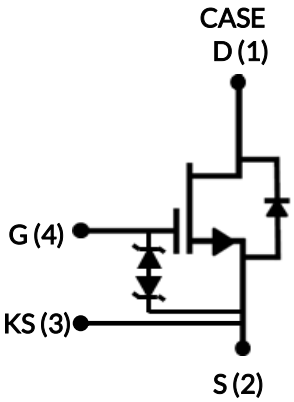
DATASHEET

UF3SC120009K4S



Part Number	Package	Marking
UF3SC120009K4S	TO-247-4L	UF3SC120009K4S

1200V-8.6mΩ SiC FET

Rev. B, December 2019

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads , and any application requiring standard gate drive.

Features

- Typical on-resistance $R_{DS(on),typ}$ of 8.6mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected, HBM class 2
- TO-247-4L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
Continuous drain current [1]	I_D	T_C < 110°C	120	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	550	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =8.6A	555	mJ
Power dissipation	P_{tot}	T_C = 25°C	789	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C

1. Limited by bondwires
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.15	0.19	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V, T_J=25°C		6	600	µA
		V_{DS}=1200V, V_{GS}=0V, T_J=175°C		65		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		5	± 20	µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=100A, T_J=25°C		8.6	11	mΩ
		V_{GS}=12V, I_D=100A, T_J=125°C		13.5		
		V_{GS}=12V, I_D=100A, T_J=175°C		18.2		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	4.7	6	V
Gate resistance	R_G	f=1MHz, open drain		0.8	1.5	Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C < 110°C			120	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			550	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=100A, T_J=25°C		1.65	2	V
		V_{GS}=0V, I_F=100A, T_J=175°C		2.4		
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=100A, V_{GS}=-5V, R_{G_EXT}=22Ω di/dt=3700A/µs, T_J=25°C		1373		nC
Reverse recovery time	t_{rr}			60		ns
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=100A, V_{GS}=-5V, R_{G_EXT}=22Ω di/dt=3700A/µs, T_J=150°C		1275		nC
Reverse recovery time	t_{rr}			60		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=0V f=100kHz		8512		pF
Output capacitance	C_{oss}			755		
Reverse transfer capacitance	C_{rss}			9		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		395		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		870		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		128		µJ
Total gate charge	Q_G	V_{DS}=800V, I_D=100A, V_{GS} = -5V to 15V		234		nC
Gate-drain charge	Q_{GD}			40		
Gate-source charge	Q_{GS}			96		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.5Ω, Turn-off $R_{G,EXT}$=5Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 5Ω, T_J=25°C		32		ns
Rise time	t_r			58		
Turn-off delay time	$t_{d(off)}$			113		
Fall time	t_f			16		
Turn-on energy	E_{ON}			3463		µJ
Turn-off energy	E_{OFF}			722		
Total switching energy	E_{TOTAL}			4185		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.5Ω, Turn-off $R_{G,EXT}$=5Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 5Ω, T_J=150°C		28		ns
Rise time	t_r			66		
Turn-off delay time	$t_{d(off)}$			126		
Fall time	t_f			16		
Turn-on energy	E_{ON}			3539		µJ
Turn-off energy	E_{OFF}			700		
Total switching energy	E_{TOTAL}			4239		

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.5Ω, Turn-off $R_{G,EXT}$=5Ω Inductive Load, FWD: UJ3D1250K, T_J=25°C		33		ns
Rise time	t_r			50		
Turn-off delay time	$t_{d(off)}$			113		
Fall time	t_f			15		
Turn-on energy	E_{ON}			1895		µJ
Turn-off energy	E_{OFF}			680		
Total switching energy	E_{TOTAL}			2575		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}$=1.5Ω, Turn-off $R_{G,EXT}$=5Ω Inductive Load, FWD: UJ3D1250K, T_J=150°C		33		ns
Rise time	t_r			52		
Turn-off delay time	$t_{d(off)}$			127		
Fall time	t_f			15		
Turn-on energy	E_{ON}			1989		µJ
Turn-off energy	E_{OFF}			595		
Total switching energy	E_{TOTAL}			2584		

Typical Performance Diagrams

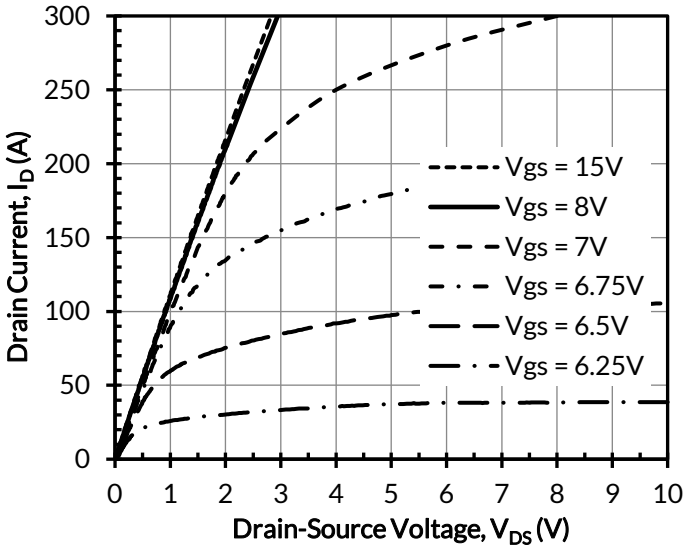


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

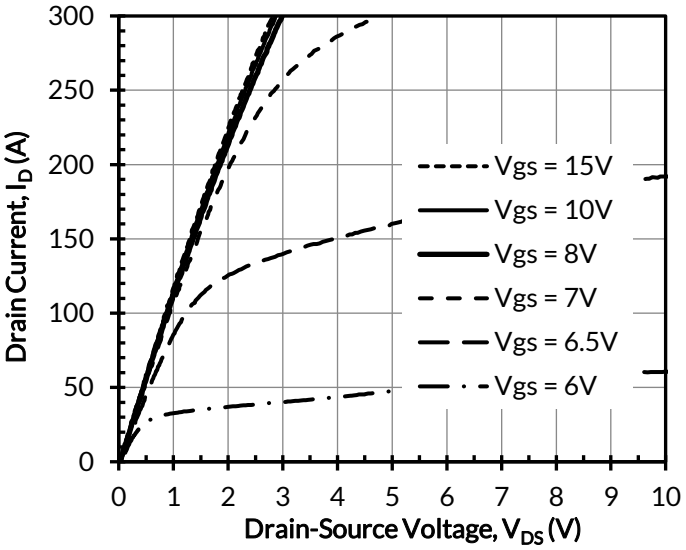


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

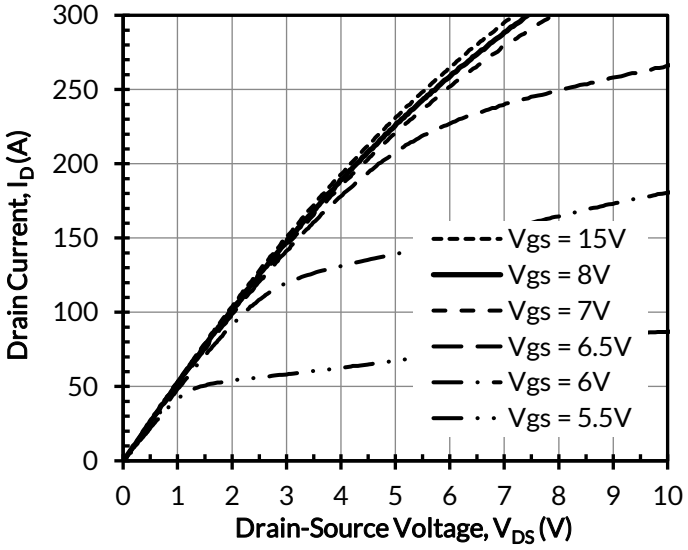


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

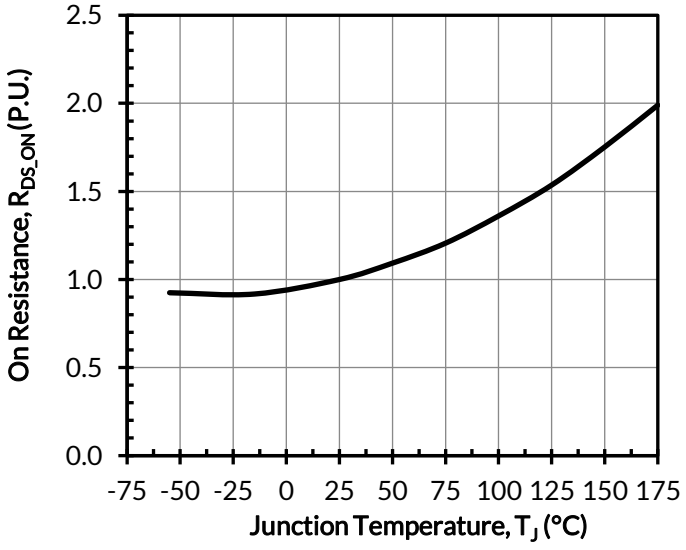


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 100A

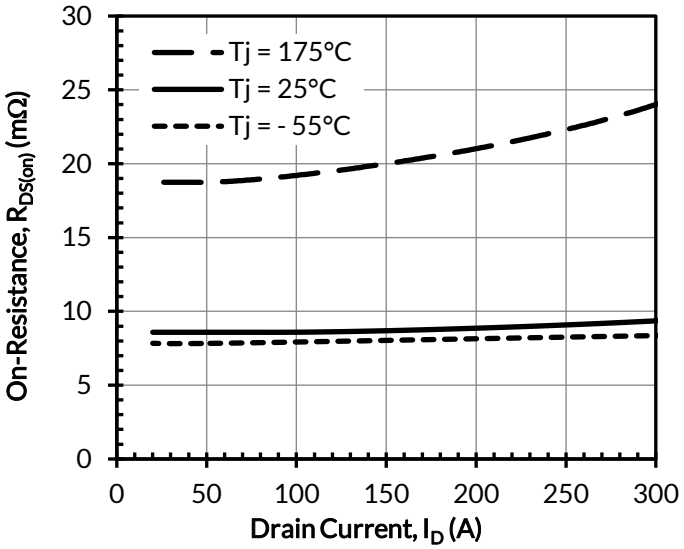


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

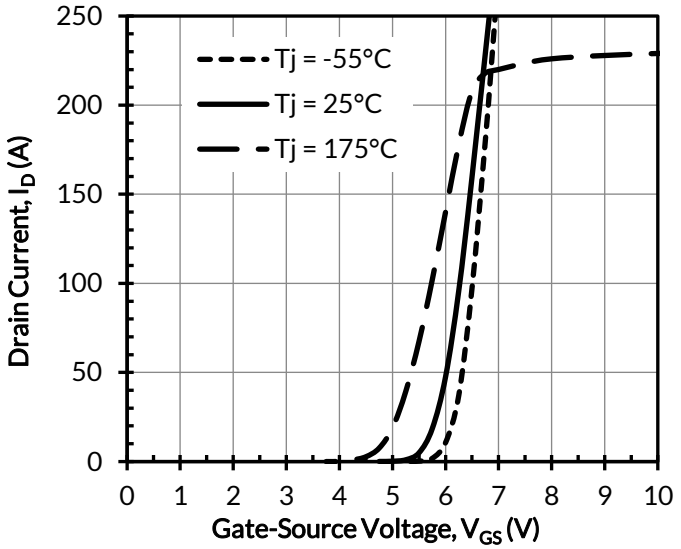


Figure 6. Typical transfer characteristics at V_{DS} = 5V

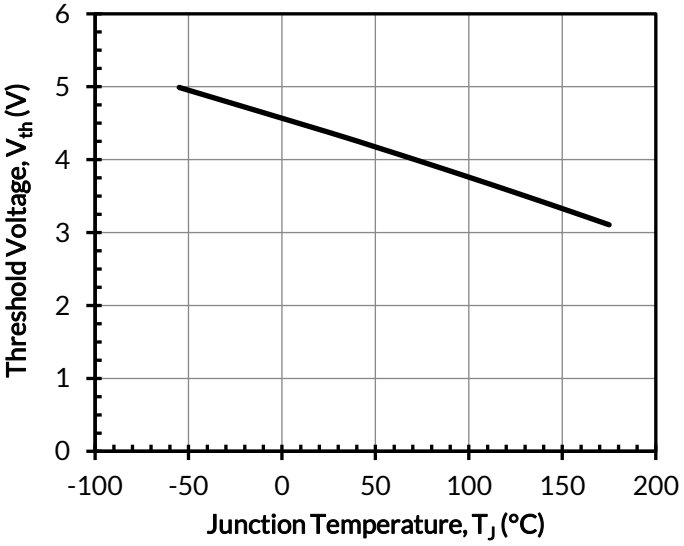


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

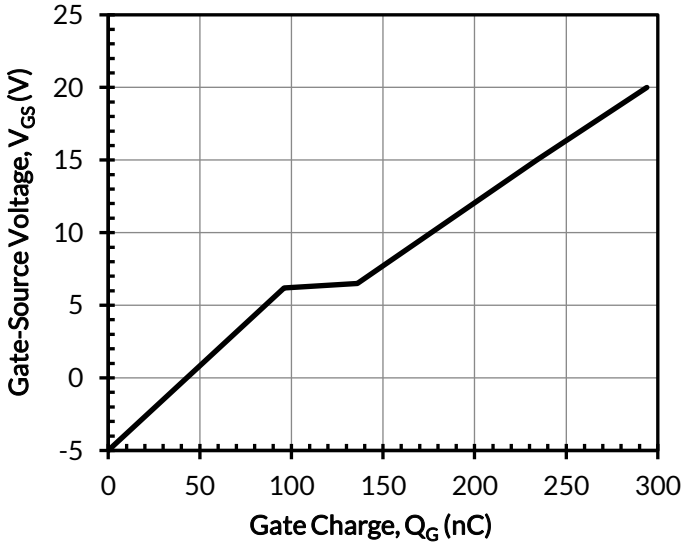


Figure 8. Typical gate charge at V_{DS} = 800V and I_D = 100A

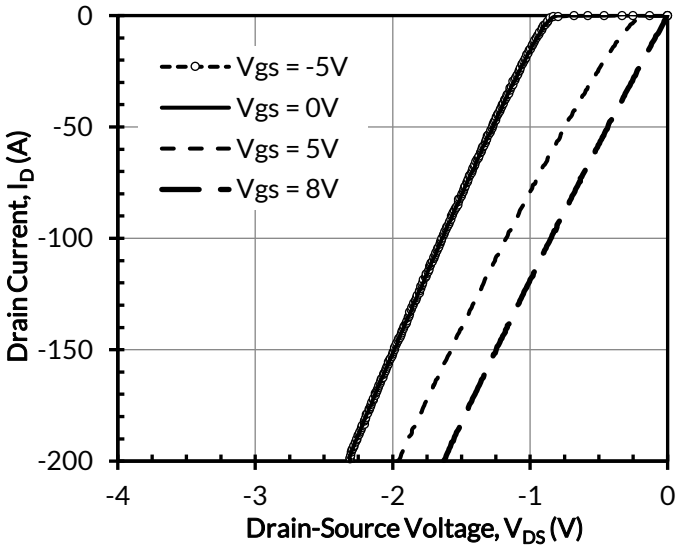


Figure 9. 3rd quadrant characteristics at T_J = -55°C

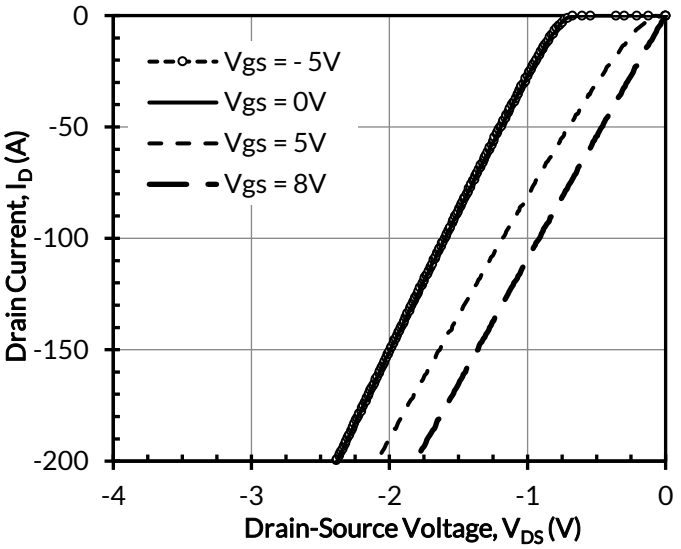


Figure 10. 3rd quadrant characteristics at T_J = 25°C

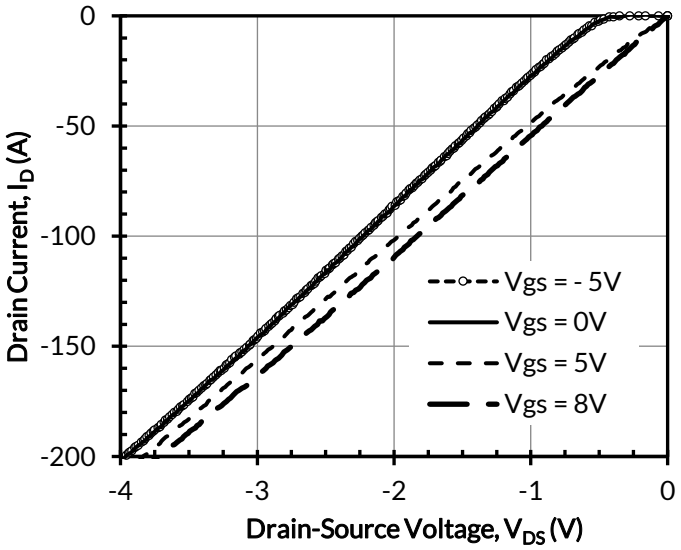


Figure 11. 3rd quadrant characteristics at T_J = 175°C

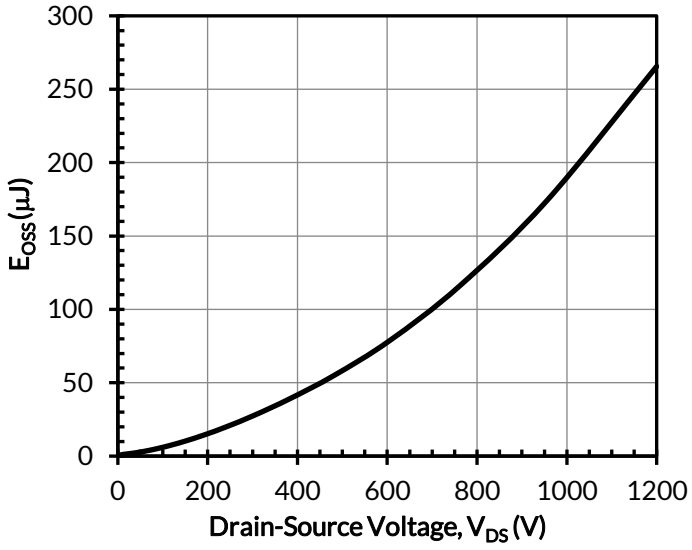


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

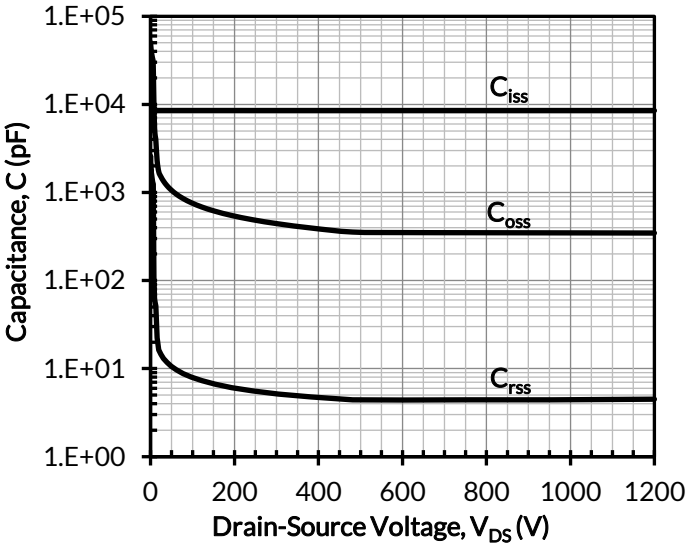


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

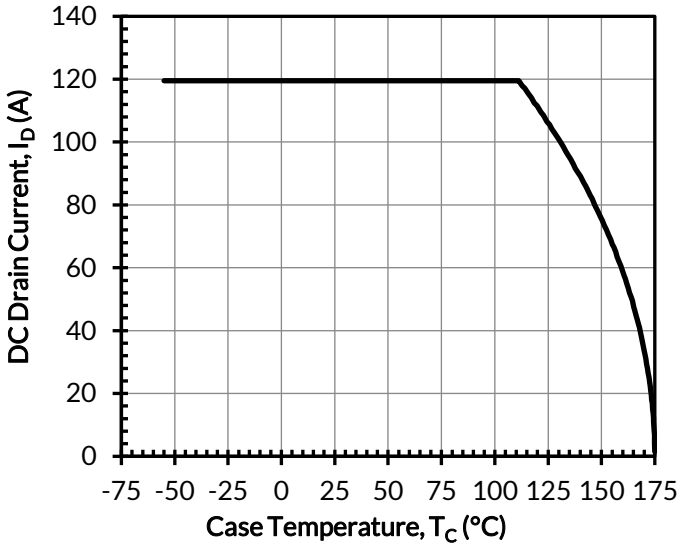


Figure 14. DC drain current derating

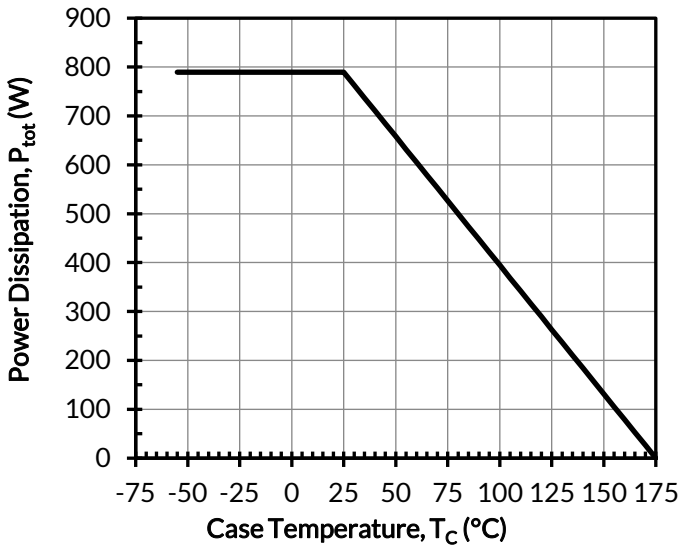


Figure 15. Total power dissipation

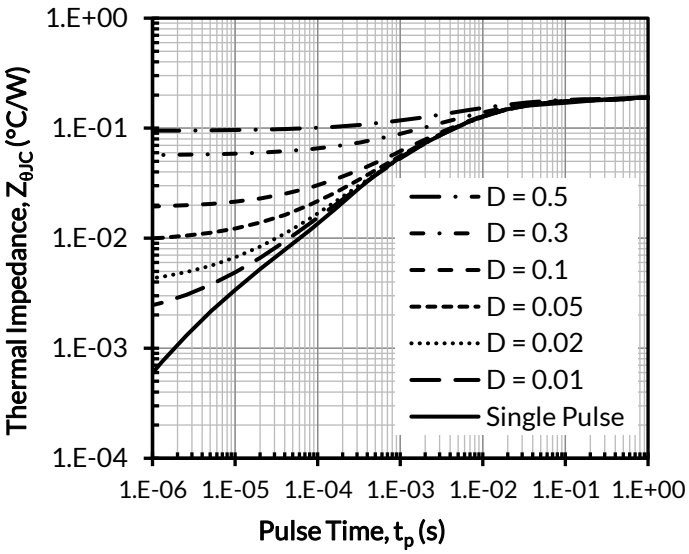


Figure 16. Maximum transient thermal impedance

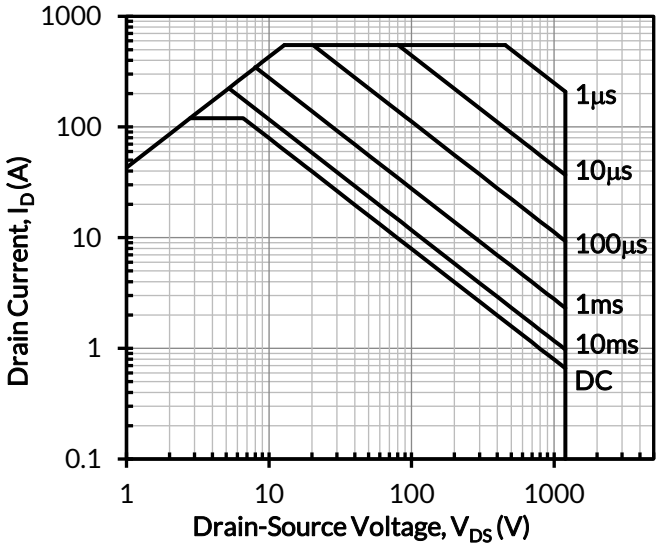


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

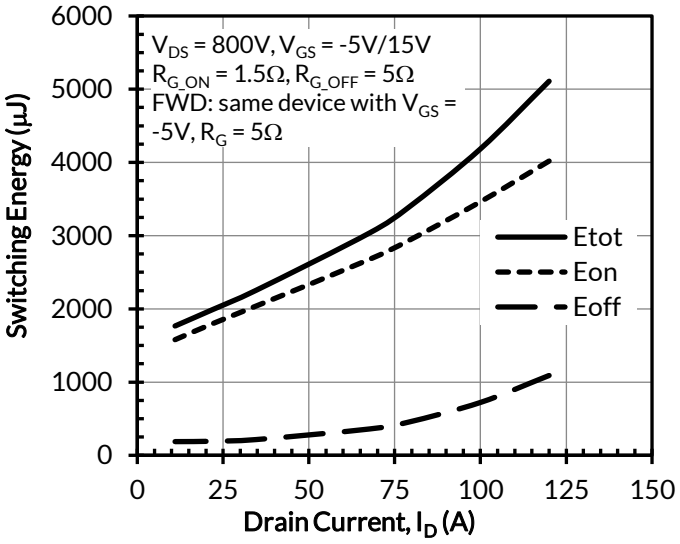


Figure 18. Clamped inductive switching energy vs. drain current at T_J = 25°C

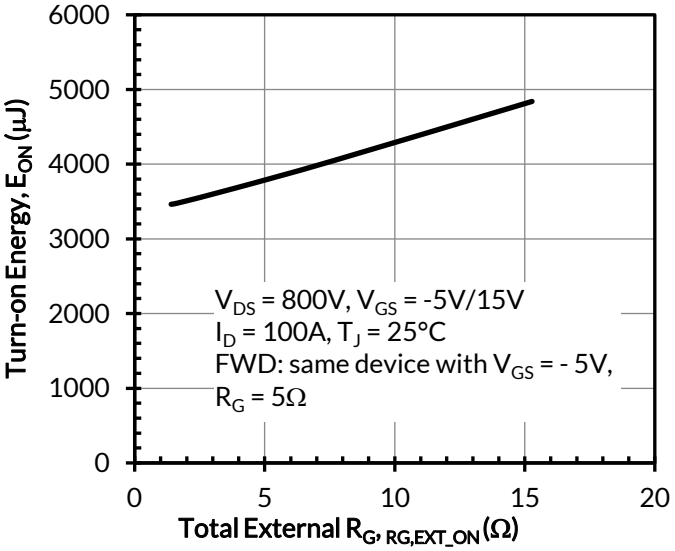


Figure 19. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

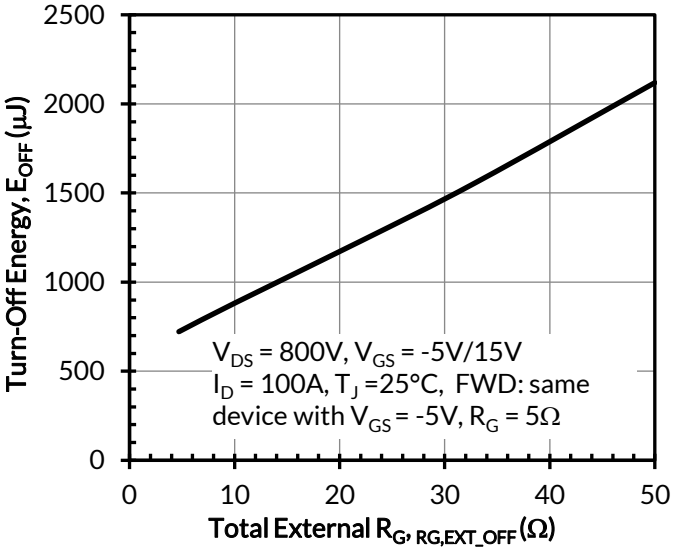


Figure 20. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

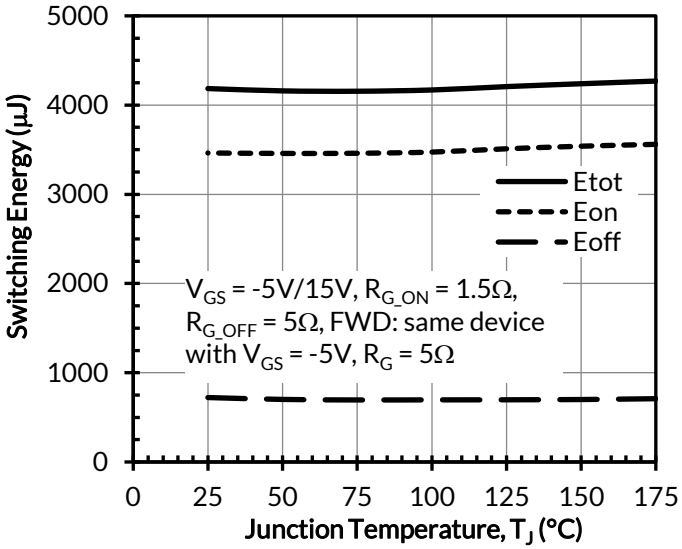


Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_D = 100A

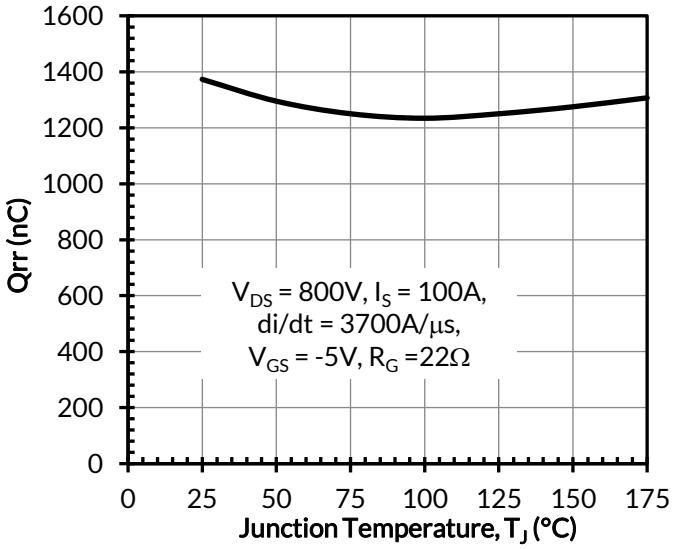


Figure 22. Reverse recovery charge Qrr vs. junction temperature

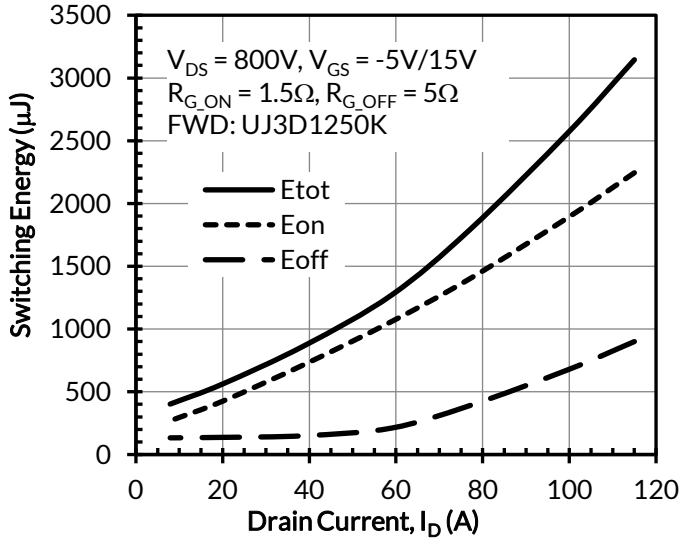


Figure 23. Clamped inductive switching energy vs. drain current at T_J = 25°C

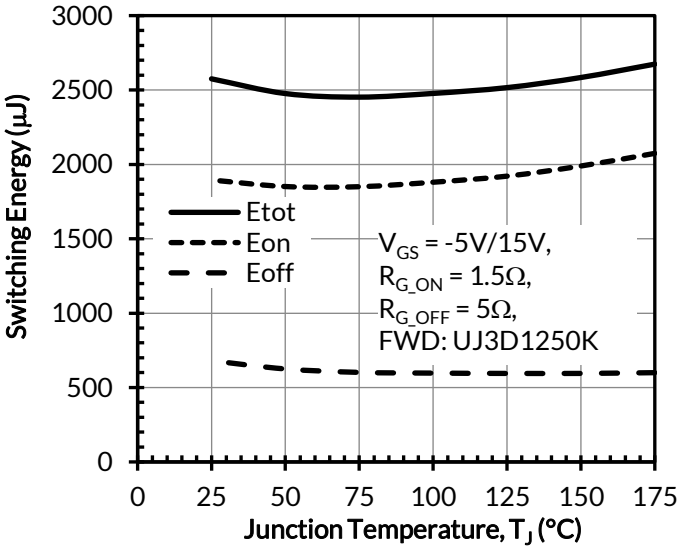


Figure 24. Clamped inductive switching energy vs. junction temperature at V_{DS} = 800V and I_D = 100A