

DATASHEET

UJ4C075023B7S

750V-23mΩ SiC FET

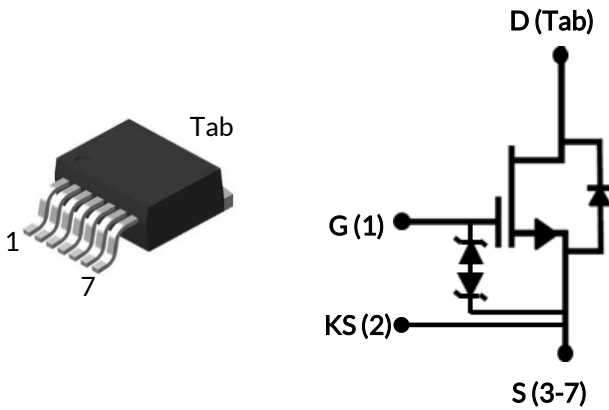
Rev. B, March 2022

Description

The UJ4C075023B7S is a 750V, 23mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- ◆ On-resistance $R_{DS(on)}$: 23mΩ (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 80nC
- ◆ Low body diode V_{FSD} : 1.23V
- ◆ Low gate charge: Q_G = 37.8nC
- ◆ Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected: HBM class 2 and CDM class C3
- ◆ D²PAK-7L package for faster switching, clean gate waveforms



Part Number	Package	Marking
UJ4C075023B7S	D ² PAK-7L	UJ4C075023B7S

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	64	A
		$T_C = 100^\circ\text{C}$	46	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	196	A
Single pulsed avalanche energy ³	E_{AS}	L=15mH, $I_{AS} = 3\text{A}$	67	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500\text{V}$	150	V/ns
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	278	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.42	0.54	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750V, V_{GS}=0V, T_J=25^\circ\text{C}$		2	30	μA
		$V_{DS}=750V, V_{GS}=0V, T_J=175^\circ\text{C}$		15		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=40A, T_J=25^\circ\text{C}$		23	29	m Ω
		$V_{GS}=12V, I_D=40A, T_J=125^\circ\text{C}$		39		
		$V_{GS}=12V, I_D=40A, T_J=175^\circ\text{C}$		50		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	4.8	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C = 25^\circ\text{C}$			64	A
Diode pulse current ²	$I_{S,pulse}$	$T_C = 25^\circ\text{C}$			196	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=20A, T_J=25^\circ\text{C}$		1.23	1.39	V
		$V_{GS}=0V, I_S=20A, T_J=175^\circ\text{C}$		1.45		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_S=40A, V_{GS}=0V, R_{G,EXT}=50\Omega$		80		nC
Reverse recovery time	t_{rr}	di/dt=1200A/ $\mu\text{s}, T_J=25^\circ\text{C}$		12		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_S=40A, V_{GS}=0V, R_{G,EXT}=50\Omega$		84		nC
Reverse recovery time	t_{rr}	di/dt=1200A/ $\mu\text{s}, T_J=150^\circ\text{C}$		12.8		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V$ $f=100kHz$		1400		pF
Output capacitance	C_{oss}			93		
Reverse transfer capacitance	C_{rss}			2.5		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		116		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		232		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		9.3		μJ
Total gate charge	Q_G	$V_{DS}=400V, I_D=40A,$ $V_{GS} = 0V$ to 15V		37.8		nC
Gate-drain charge	Q_{GD}			8		
Gate-source charge	Q_{GS}			11.8		
Turn-on delay time	$t_{d(on)}$	Notes 4, $V_{DS}=400V, I_D=40A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=50\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 50\Omega,$ $T_J=25^\circ C$		11		ns
Rise time	t_r			23		
Turn-off delay time	$t_{d(off)}$			158		
Fall time	t_f			17		
Turn-on energy	E_{ON}			219		
Turn-off energy	E_{OFF}		167		μJ	
Total switching energy	E_{TOTAL}		386			
Turn-on delay time	$t_{d(on)}$	Notes 4, $V_{DS}=400V, I_D=40A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=50\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 50\Omega,$ $T_J=150^\circ C$		11		ns
Rise time	t_r			23		
Turn-off delay time	$t_{d(off)}$			160		
Fall time	t_f			18.4		
Turn-on energy	E_{ON}			238		
Turn-off energy	E_{OFF}		189		μJ	
Total switching energy	E_{TOTAL}		427			

4. Measured with the switching test circuit in Figure 23.

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V$, $I_D=40A$, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=5\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$, RC snubber: $R_S=10\Omega$ and $C_S=200pF$, $T_J=25^\circ C$		13		ns	
Rise time	t_r			23			
Turn-off delay time	$t_{d(off)}$			44			
Fall time	t_f			9.6			
Turn-on energy including R_S energy	E_{ON}				231		μJ
Turn-off energy including R_S energy	E_{OFF}				53		
Total switching energy	E_{TOTAL}				284		
Snubber R_S energy during turn-on	E_{RS_ON}				8		
Snubber R_S energy during turn-off	E_{RS_OFF}				5		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V$, $I_D=40A$, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=5\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$, RC snubber: $R_S=10\Omega$ and $C_S=200pF$, $T_J=150^\circ C$		12		ns	
Rise time	t_r			23			
Turn-off delay time	$t_{d(off)}$			44			
Fall time	t_f			9.6			
Turn-on energy including R_S energy	E_{ON}				231		μJ
Turn-off energy including R_S energy	E_{OFF}				53		
Total switching energy	E_{TOTAL}				284		
Snubber R_S energy during turn-on	E_{RS_ON}				8.3		
Snubber R_S energy during turn-off	E_{RS_OFF}				6		

5. Measured with the switching test circuit in Figure 24.

6. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

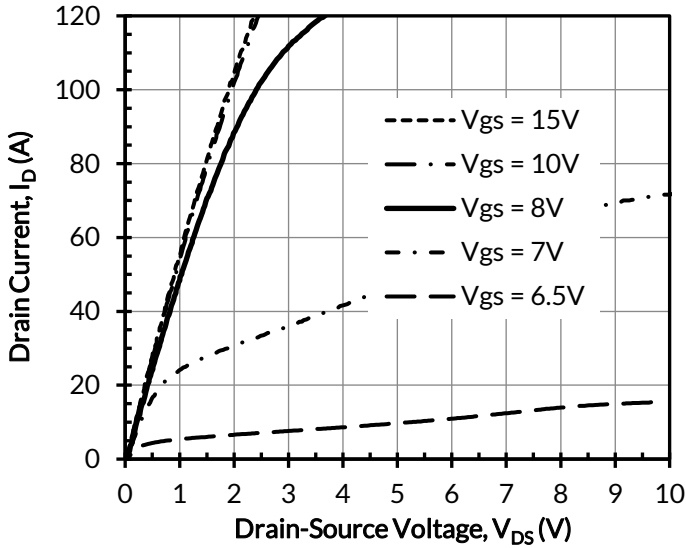


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

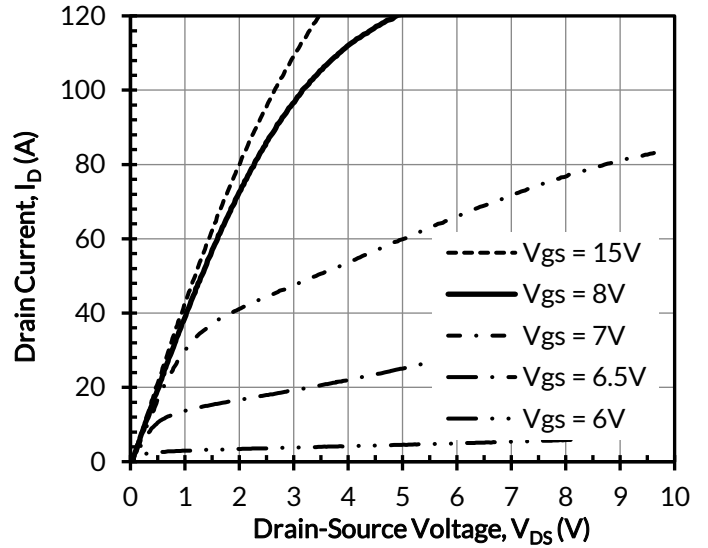


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

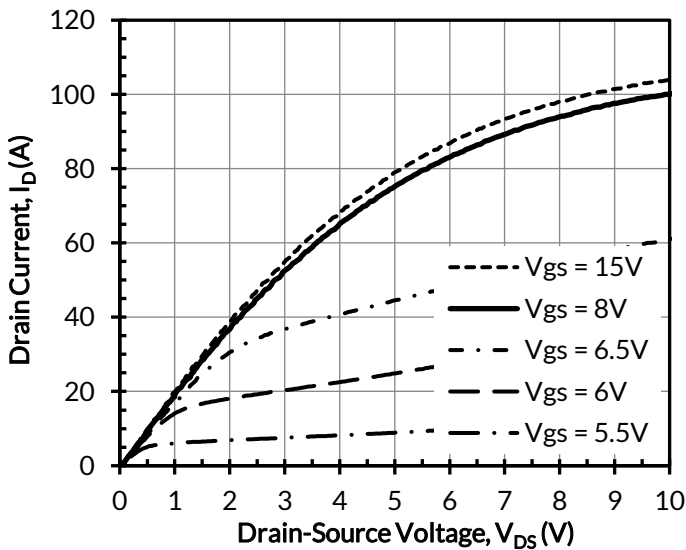


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

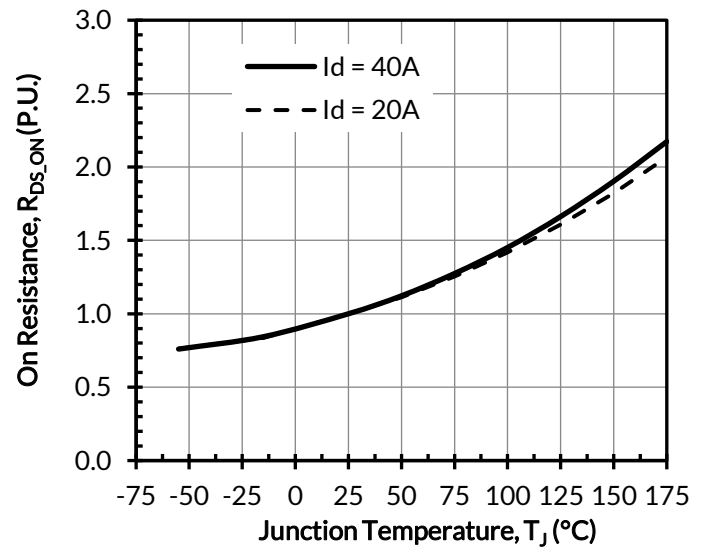


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$

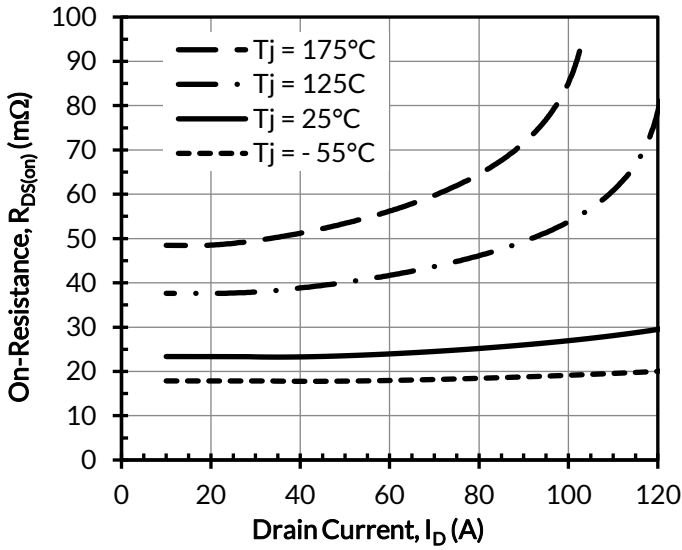


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

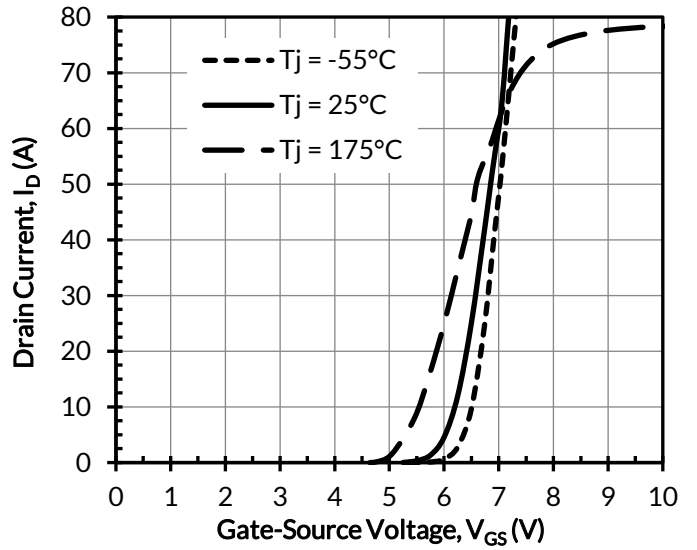


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

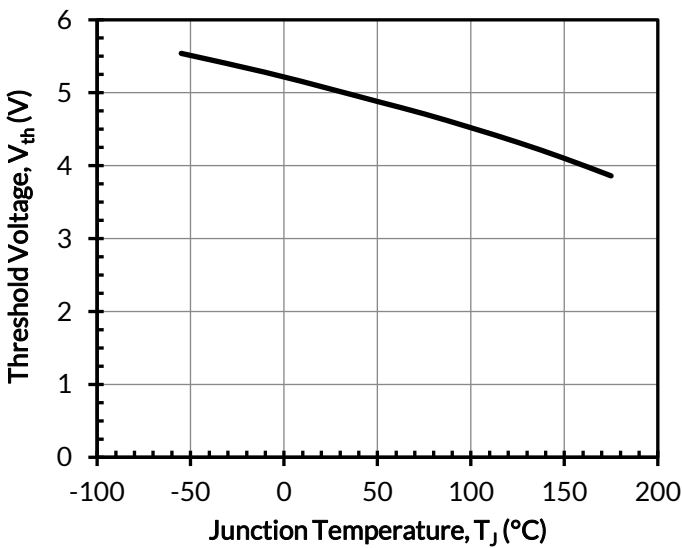


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

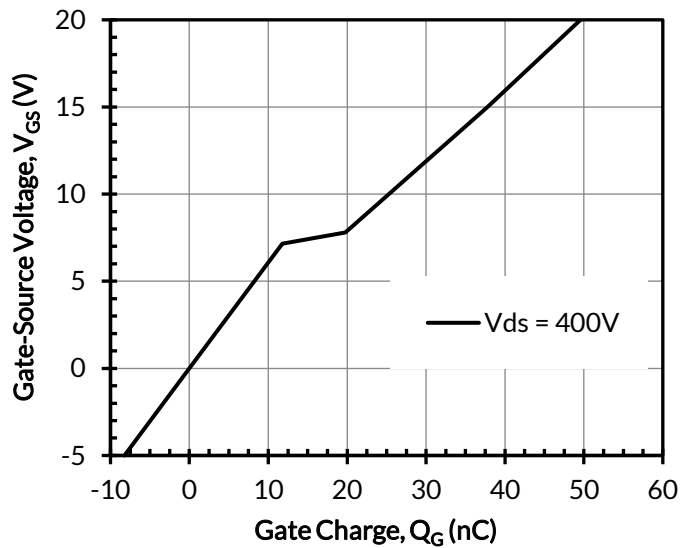


Figure 8. Typical gate charge at $I_D = 40A$

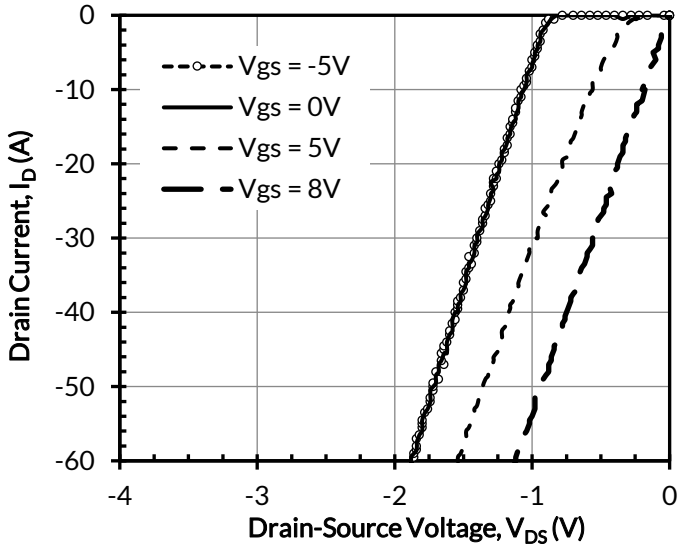


Figure 9. 3rd quadrant characteristics at $T_J = -55^\circ\text{C}$

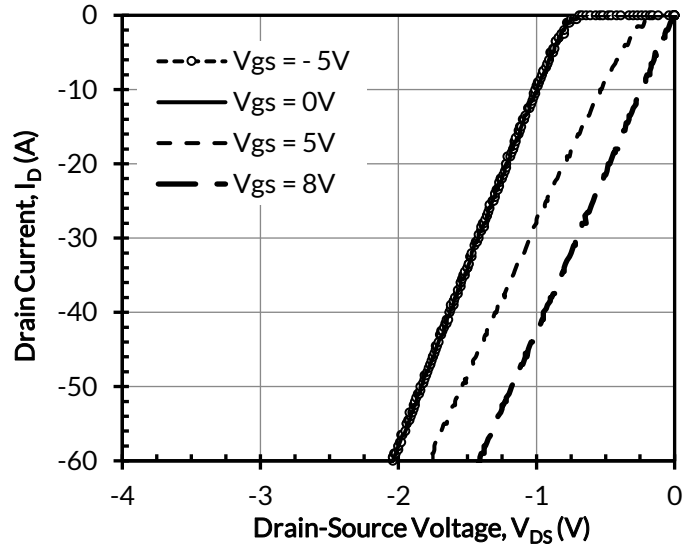


Figure 10. 3rd quadrant characteristics at $T_J = 25^\circ\text{C}$

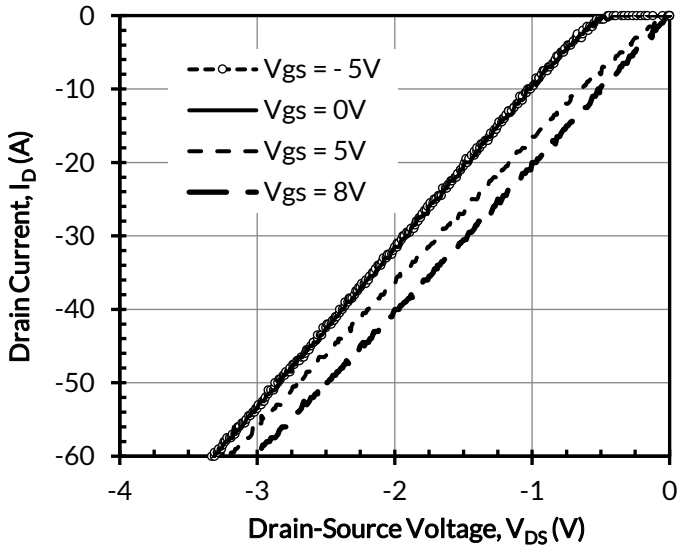


Figure 11. 3rd quadrant characteristics at $T_J = 175^\circ\text{C}$

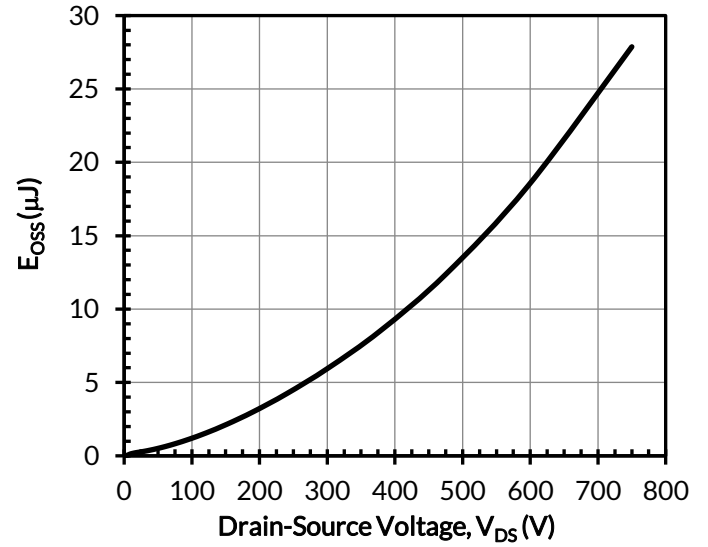


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

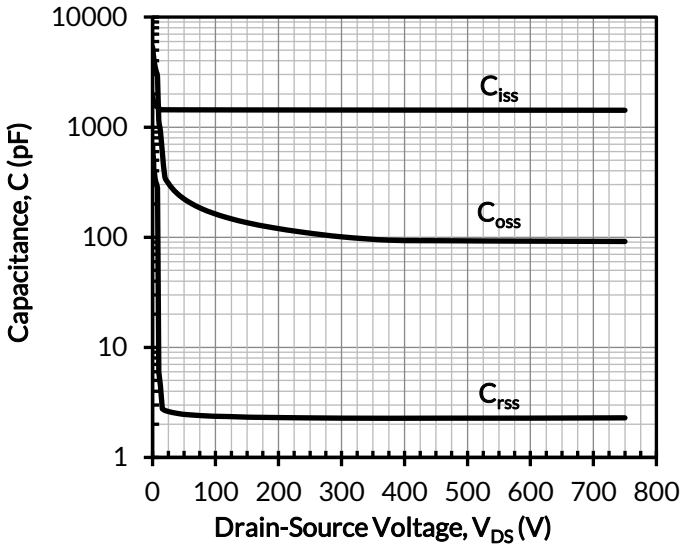


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

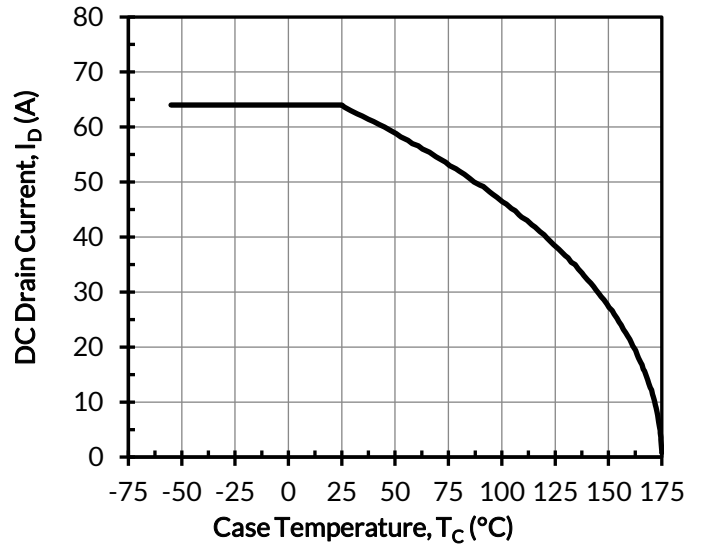


Figure 14. DC drain current derating

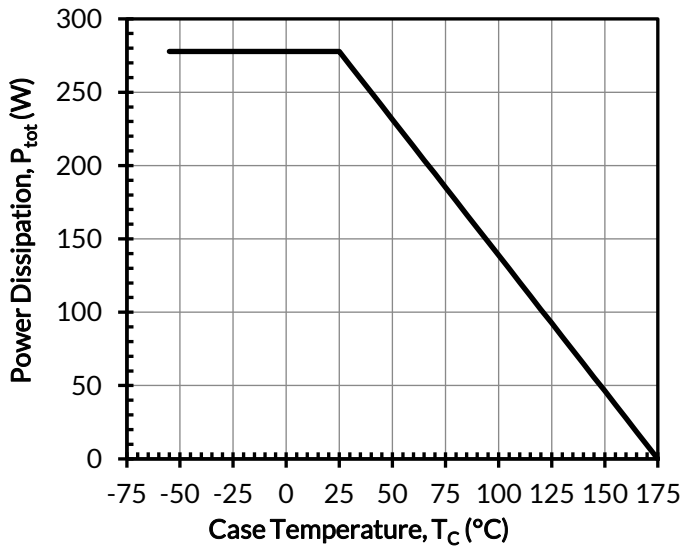


Figure 15. Total power dissipation

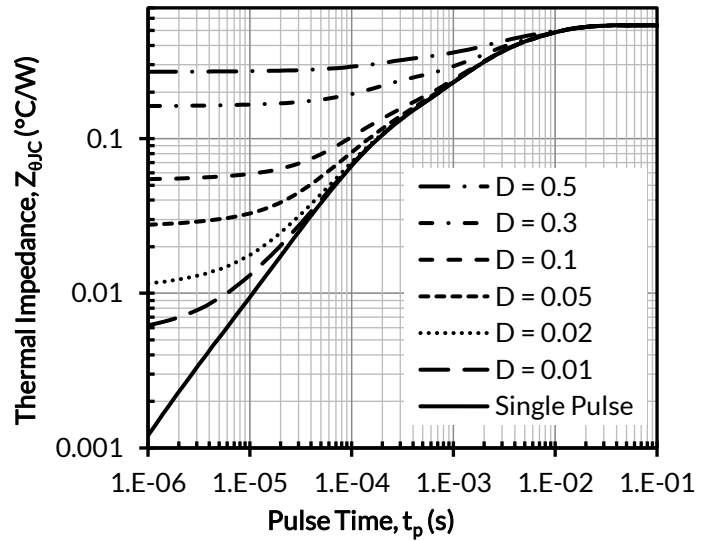


Figure 16. Maximum transient thermal impedance

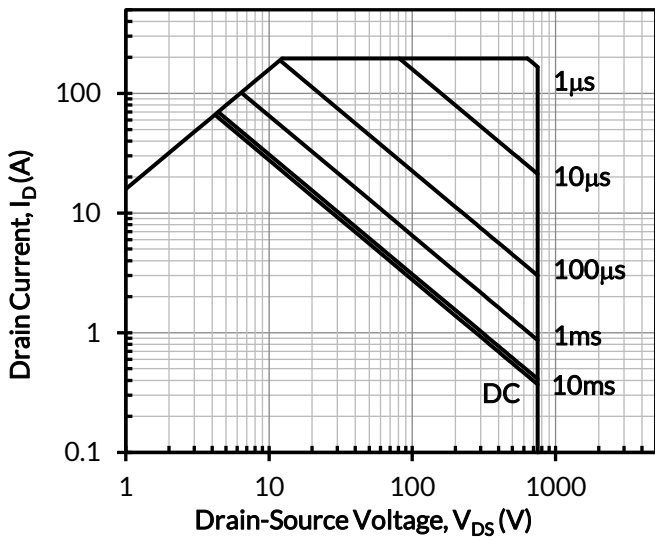


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

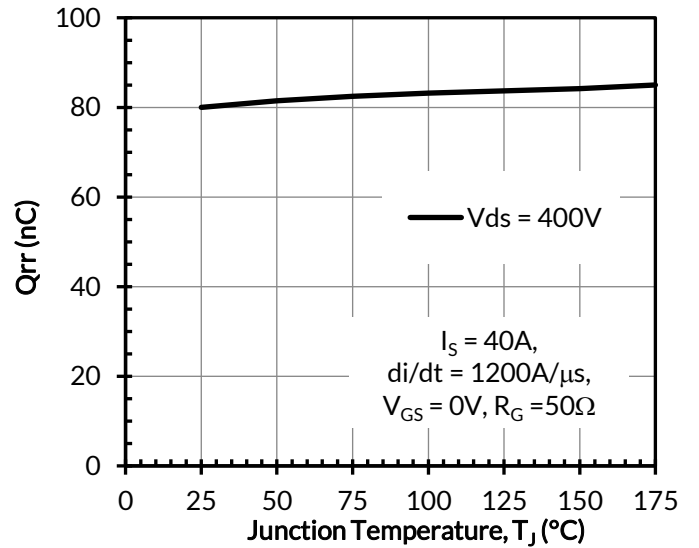


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

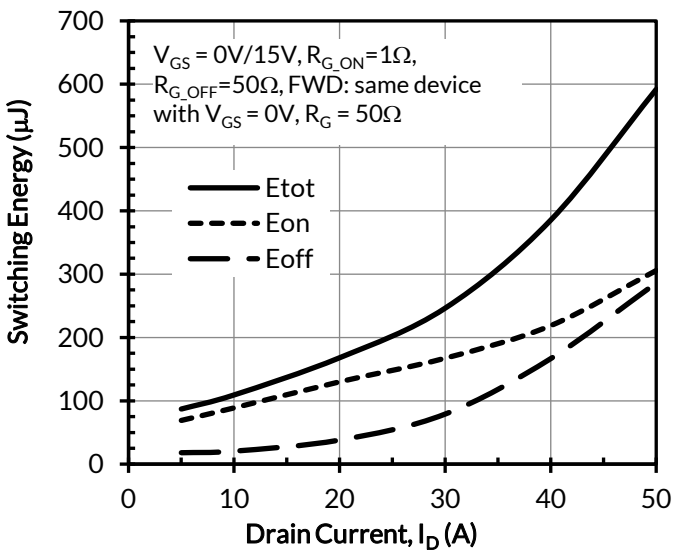


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

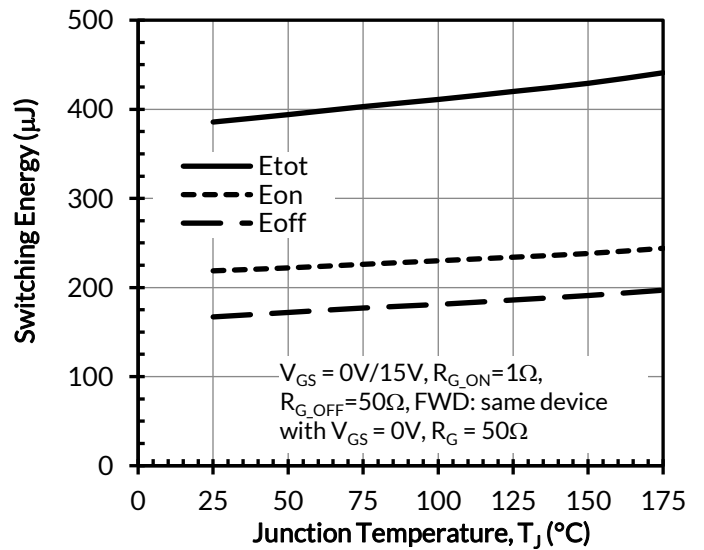


Figure 21. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 400\text{V}$ and $I_D = 40\text{A}$

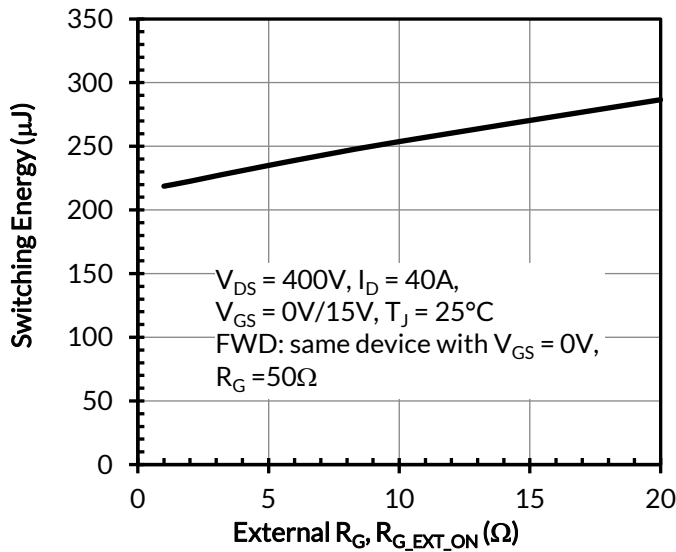


Figure 21. Clamped inductive switching turn-on energy vs. $R_{G_EXT_ON}$

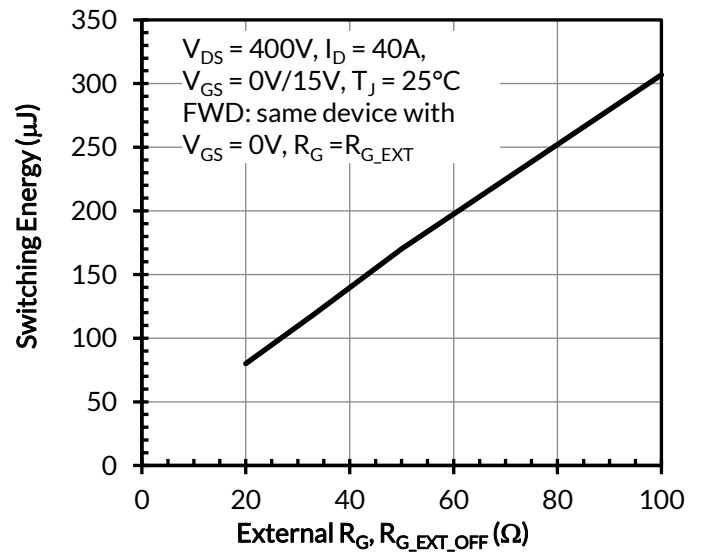


Figure 22. Clamped inductive switching turn-off energy vs. $R_{G_EXT_OFF}$

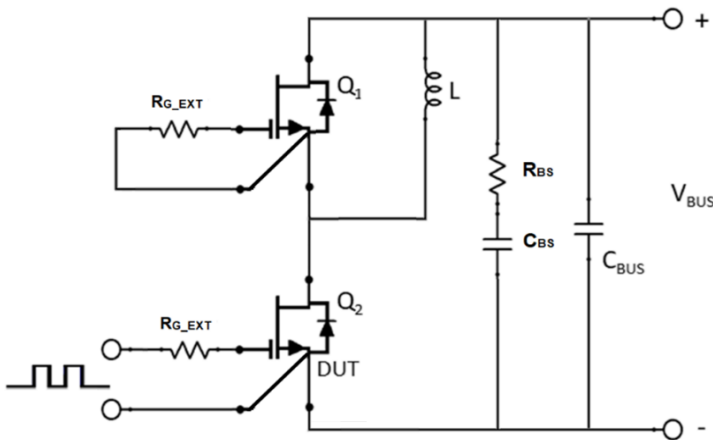


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 2.5\Omega, C_{BS} = 100\text{nF}$) is used to reduce the power loop high frequency oscillations.

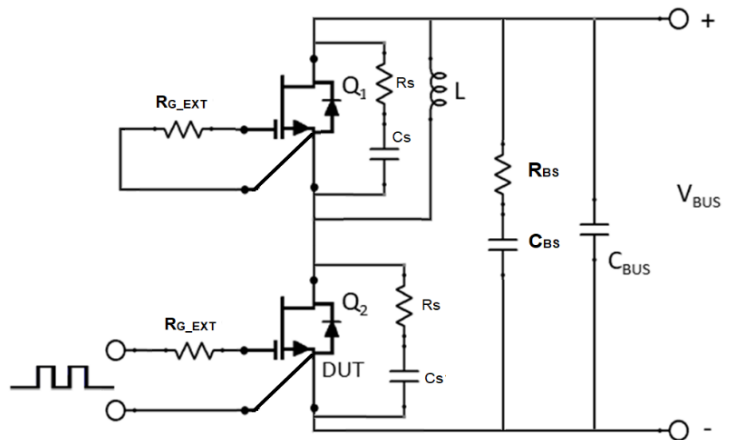


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_S = 10\Omega, C_S = 200\text{pF}$) and a bus RC snubber ($R_{BS} = 2.5\Omega, C_{BS} = 100\text{nF}$).