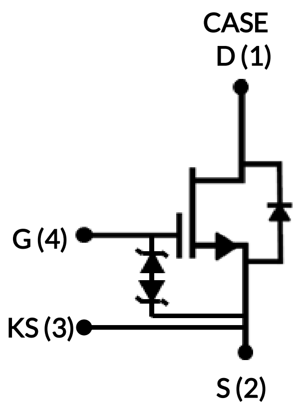
750V-23mΩ SiC FET

Rev. B, July 2021

DATASHEET

UJ4C075023K4S



Part Number	Package	Marking
UJ4C075023K4S	TO-247-4L	UJ4C075023K4S

RoHS COMPLIANT · Pb LEAD FREE · HF HALOGEN FREE

Description

The UJ4C075023K4S is a 750V, 23mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 23mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 105nC
- Low body diode V_{FSD}: 1.23V
- Low gate charge: Q_G = 37.8nC
- Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- TO-247-4L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [1]	I_D	T_C = 25°C	66	A
		T_C = 100°C	49	A
Pulsed drain current [2]	I_{DM}	T_C = 25°C	196	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =3A	67	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq$ 500V	150	V/ns
Power dissipation	P_{tot}	T_C = 25°C	306	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1. Limited by $T_{J,max}$
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.38	0.49	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=0V, T_J=25°C		2	30	μA
		V_{DS}=750V, V_{GS}=0V, T_J=175°C		15		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=40A, T_J=25°C		23	29	mΩ
		V_{GS}=12V, I_D=40A, T_J=125°C		39		
		V_{GS}=12V, I_D=40A, T_J=175°C		50		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	4.8	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C = 25°C			66	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			196	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=20A, T_J=25°C		1.23	1.39	V
		V_{GS}=0V, I_S=20A, T_J=175°C		1.45		
Reverse recovery charge	Q_{rr}	V_R=400V, I_S=40A, V_{GS}=0V, R_{G_EXT}=5Ω di/dt=3100A/μs, T_J=25°C		105		nC
Reverse recovery time	t_{rr}			12		ns
Reverse recovery charge	Q_{rr}	V_R=400V, I_S=40A, V_{GS}=0V, R_{G_EXT}=5Ω di/dt=3100A/μs, T_J=150°C		112		nC
Reverse recovery time	t_{rr}			13		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V f=100kHz		1400		pF
Output capacitance	C_{oss}			93		
Reverse transfer capacitance	C_{rss}			2.5		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V		116		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 400V, V_{GS}=0V		232		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V		9.3		μJ
Total gate charge	Q_G	V_{DS}=400V, I_D=40A, V_{GS} = 0V to 15V		37.8		nC
Gate-drain charge	Q_{GD}			8		
Gate-source charge	Q_{GS}			11.8		
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, V_{DS}=400V, I_D=40A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G = 5Ω, RC snubber: R_S=10Ω and C_S=200pF, T_J=25°C		16		ns
Rise time	t_r			27		
Turn-off delay time	$t_{d(off)}$			28		
Fall time	t_f			8		
Turn-on energy including R_S energy	E_{ON}			237		μJ
Turn-off energy including R_S energy	E_{OFF}			50		
Total switching energy	E_{TOTAL}			287		
Snubber R_S energy during turn-on	E_{RS_ON}			4.9		
Snubber R_S energy during turn-off	E_{RS_OFF}			17		
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, V_{DS}=400V, I_D=40A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G = 5Ω, RC snubber: R_S=10Ω and C_S=200pF, T_J=150°C		19		ns
Rise time	t_r			24		
Turn-off delay time	$t_{d(off)}$			29		
Fall time	t_f			10		
Turn-on energy including R_S energy	E_{ON}			288		μJ
Turn-off energy including R_S energy	E_{OFF}			60		
Total switching energy	E_{TOTAL}			348		
Snubber R_S energy during turn-on	E_{RS_ON}			4		
Snubber R_S energy during turn-off	E_{RS_OFF}			18		

4. Measured with the switching test circuit in Figure 35.
5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Turn-on delay time	$t_{d(on)}$	Note 6, V_{DS}=400V, I_D=40A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: UJ3D06520TS, RC snubber: R_S=10Ω and C_S=200pF, T_J=25°C		17		ns
Rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			22		
Fall time	t_f			7		
Turn-on energy including R_S energy	E_{ON}			167		μJ
Turn-off energy including R_S energy	E_{OFF}			40		
Total switching energy	E_{TOTAL}			207		
Snubber R_S energy during turn-on	E_{RS_ON}			4.3		
Snubber R_S energy during turn-off	E_{RS_OFF}			26		
Turn-on delay time	$t_{d(on)}$	Note 6, V_{DS}=400V, I_D=40A, Gate Driver =0V to +15V, Turn-on $R_{G,EXT}$=1Ω, Turn-off $R_{G,EXT}$=5Ω, inductive Load, FWD: UJ3D06520TS, RC snubber: R_S=10Ω and C_S=200pF, T_J=150°C		17		ns
Rise time	t_r			22		
Turn-off delay time	$t_{d(off)}$			23		
Fall time	t_f			8		
Turn-on energy including R_S energy	E_{ON}			183		μJ
Turn-off energy including R_S energy	E_{OFF}			58		
Total switching energy	E_{TOTAL}			241		
Snubber R_S energy during turn-on	E_{RS_ON}			4		
Snubber R_S energy during turn-off	E_{RS_OFF}			22		

6. Measured with the switching test circuit in Figure 35.

Typical Performance Diagrams

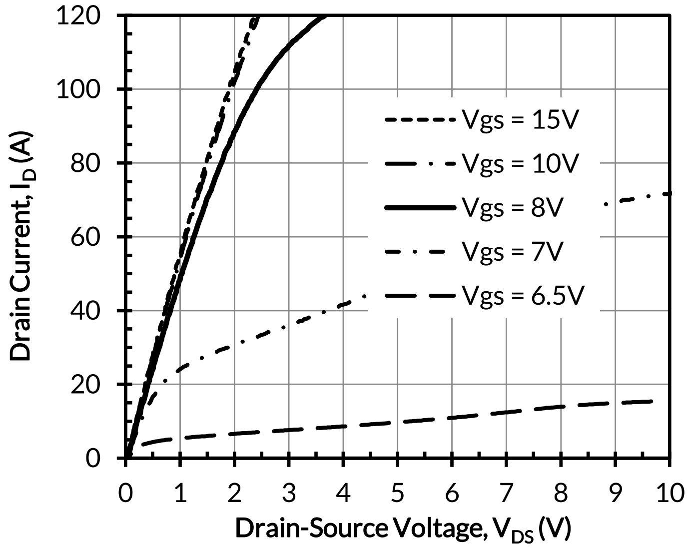


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250μs

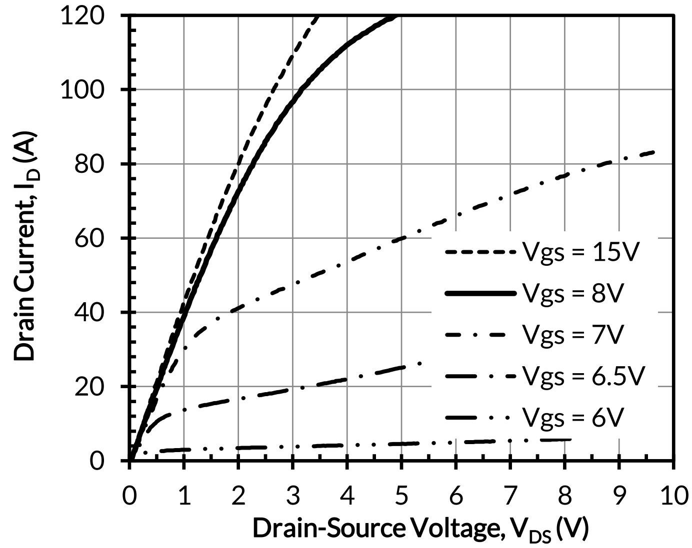


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250μs

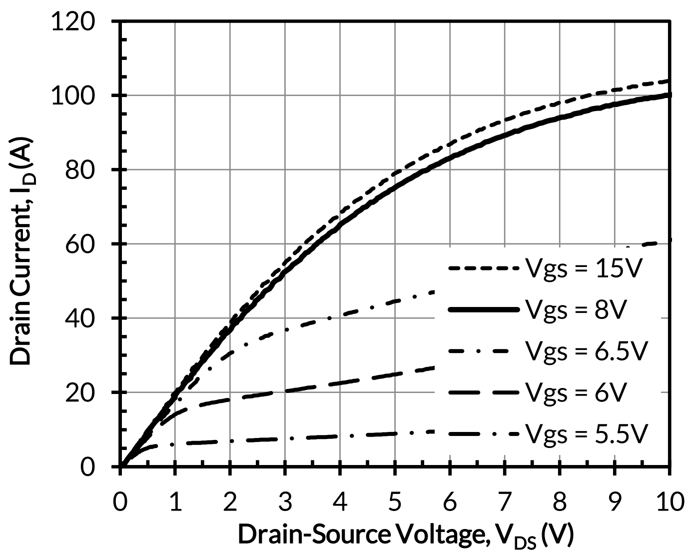


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250μs

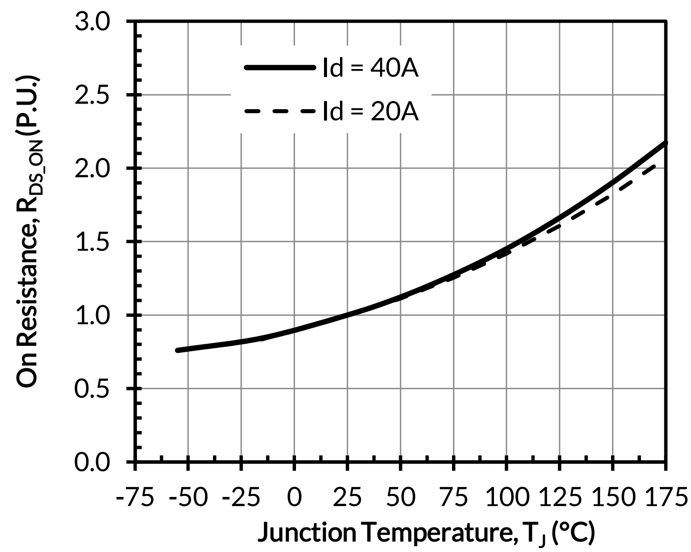


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V

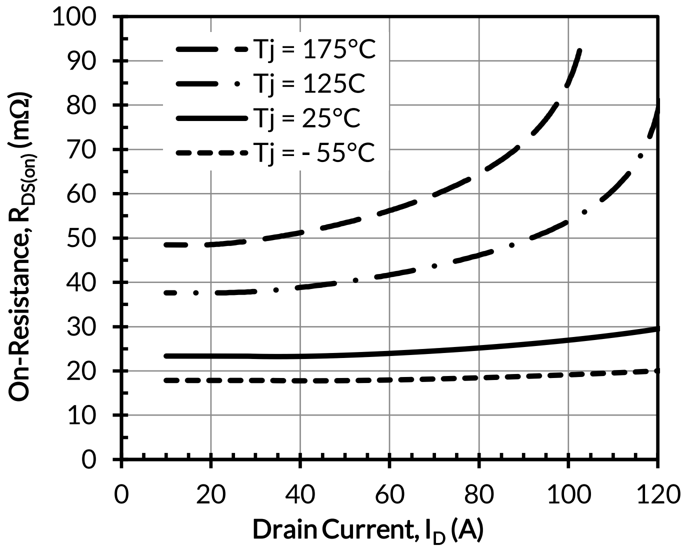


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

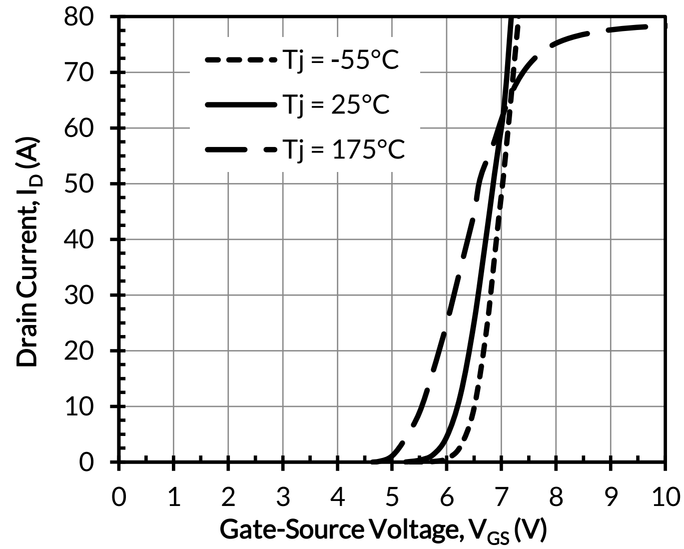


Figure 6. Typical transfer characteristics at V_{DS} = 5V

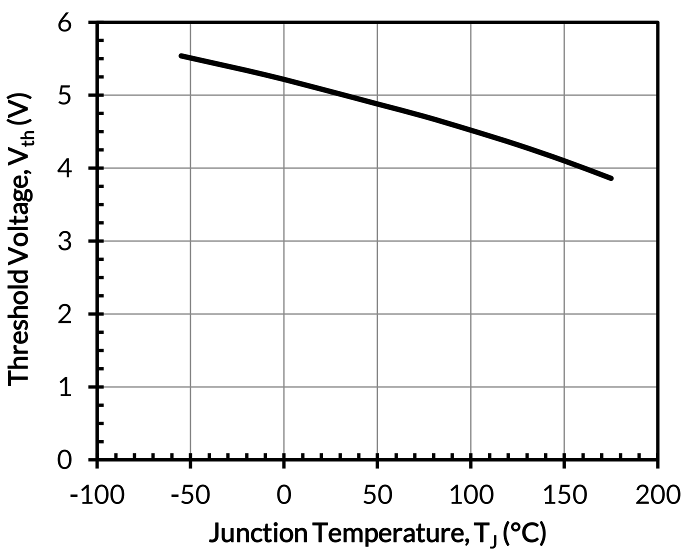


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

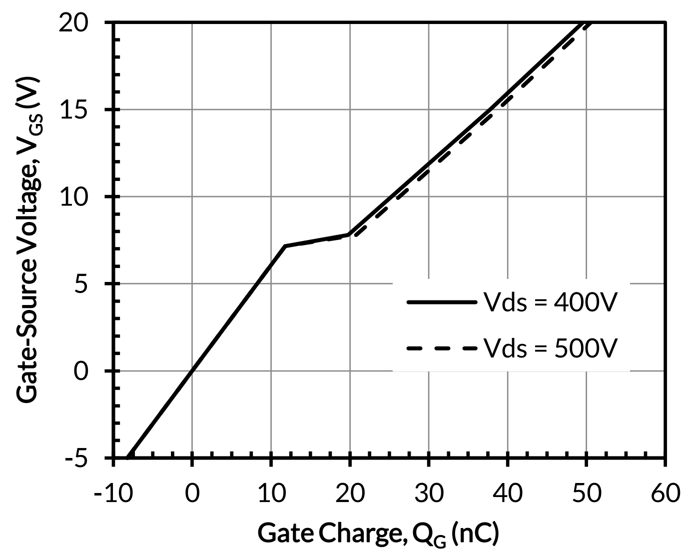


Figure 8. Typical gate charge at I_D = 40A

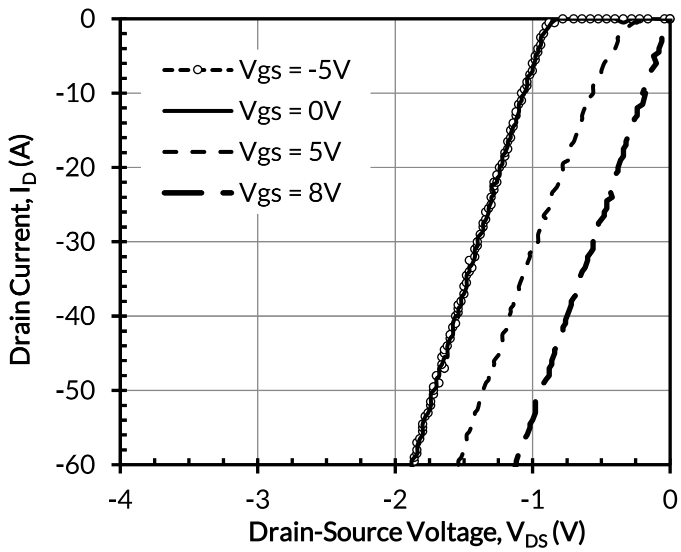


Figure 9. 3rd quadrant characteristics at T_J = -55°C

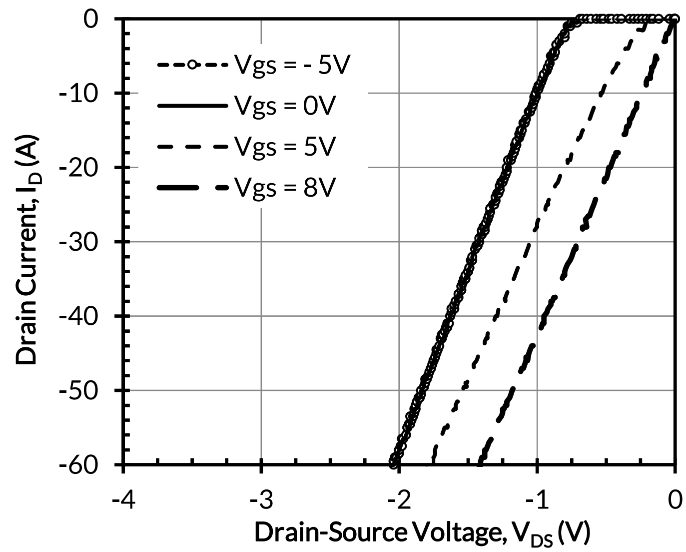


Figure 10. 3rd quadrant characteristics at T_J = 25°C

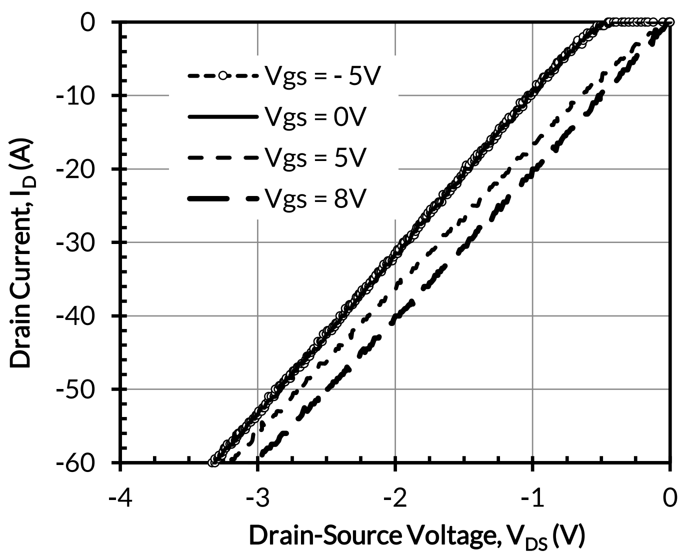


Figure 11. 3rd quadrant characteristics at T_J = 175°C

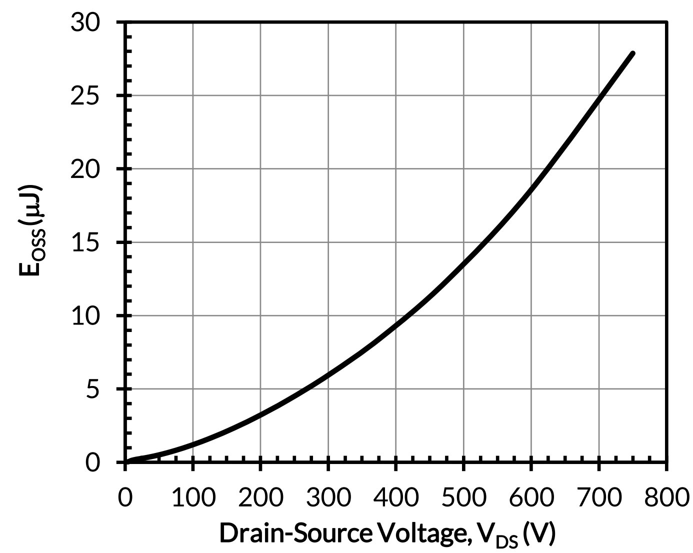


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

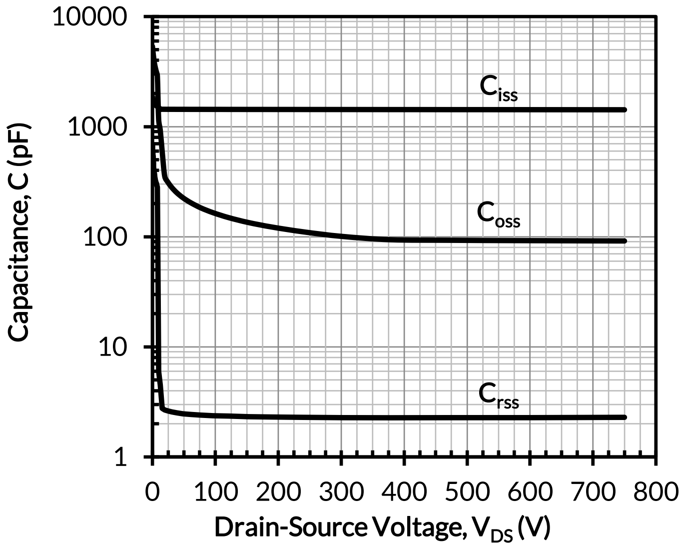


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

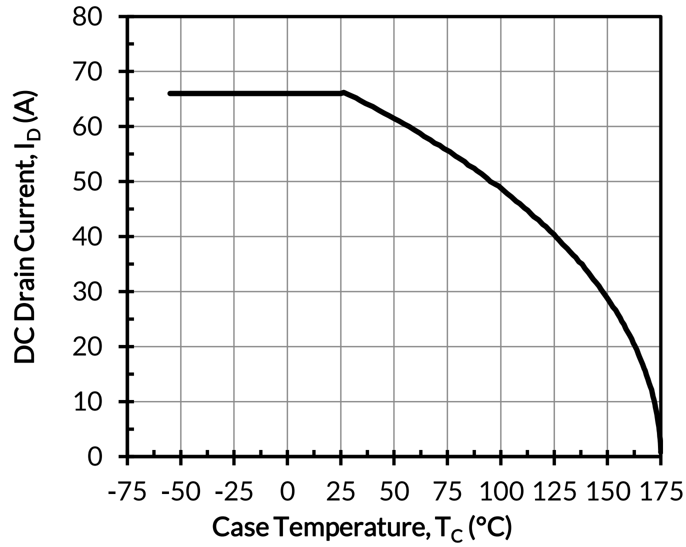


Figure 14. DC drain current derating

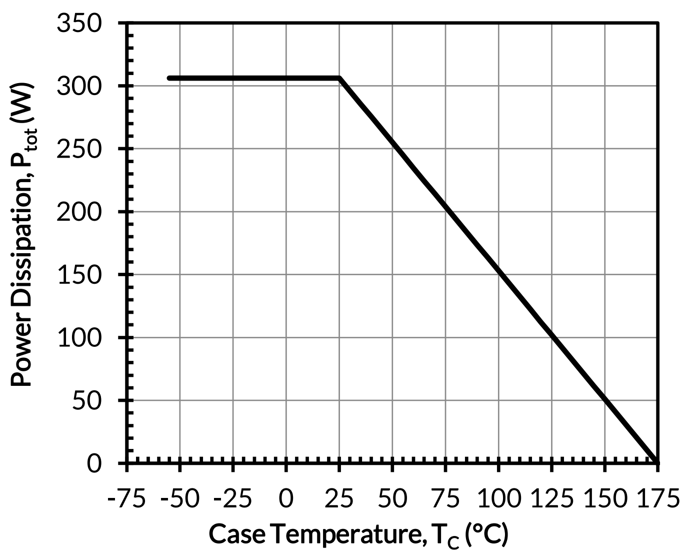


Figure 15. Total power dissipation

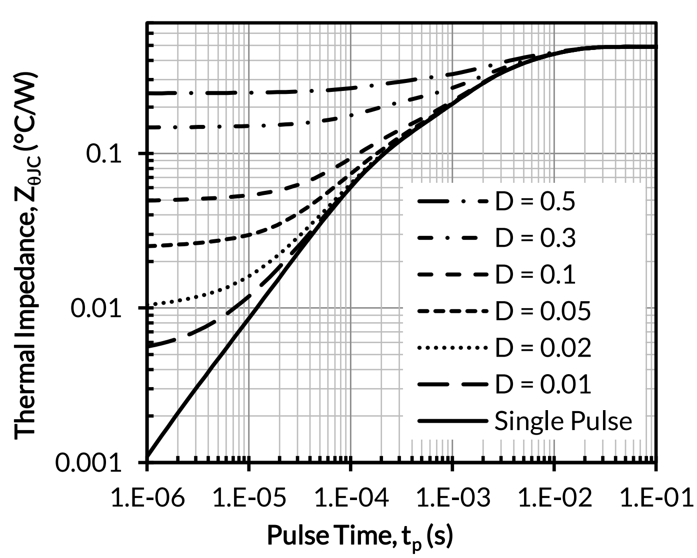


Figure 16. Maximum transient thermal impedance

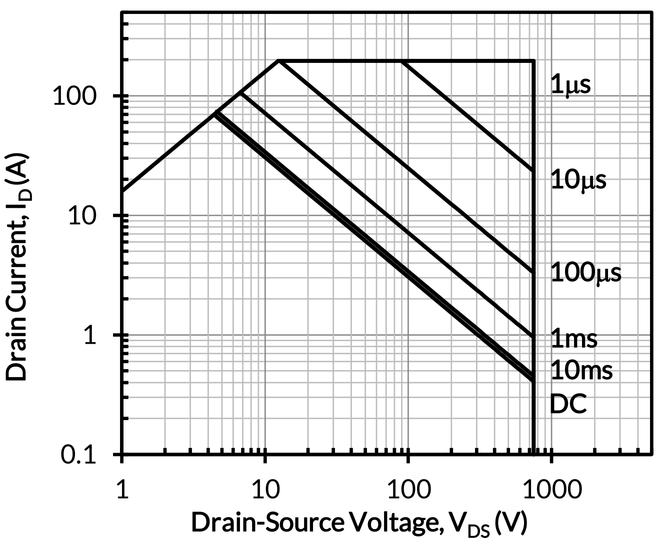


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

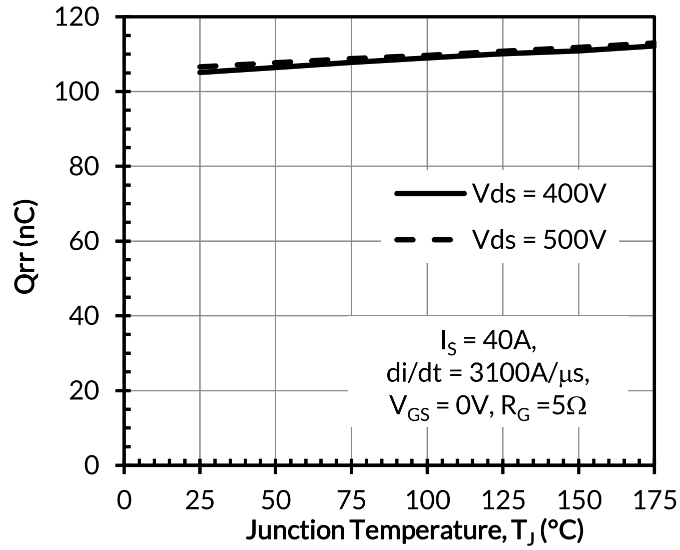


Figure 18. Reverse recovery charge Qrr vs. junction temperature

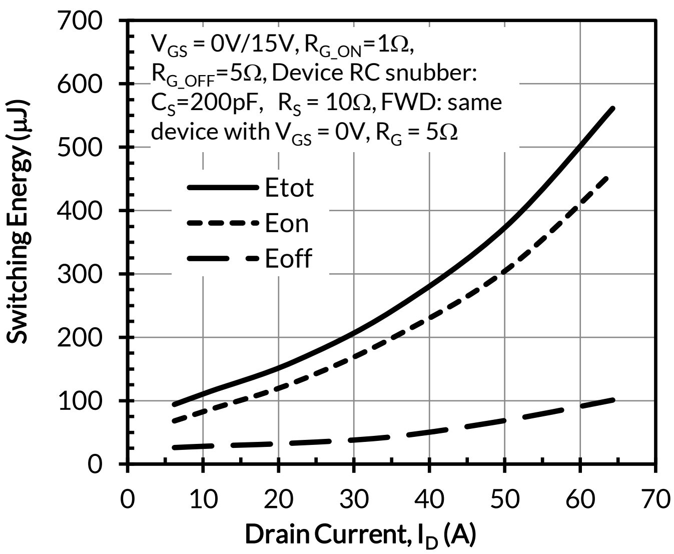


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

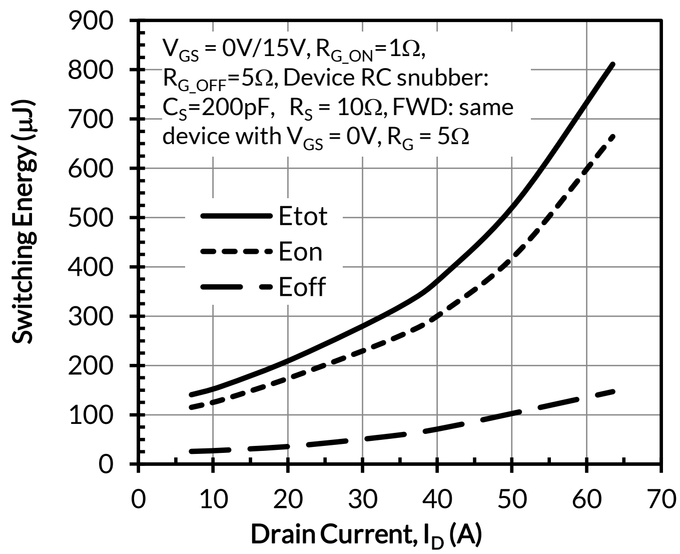


Figure 20. Clamped inductive switching energy vs. drain current at V_{DS} = 500V and T_J = 25°C

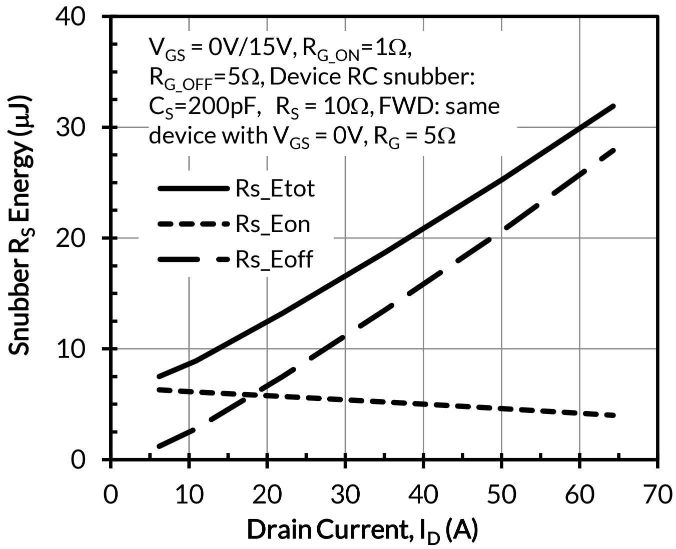


Figure 21. RC snubber energy loss vs. drain current at V_{DS} = 400V and T_J = 25°C

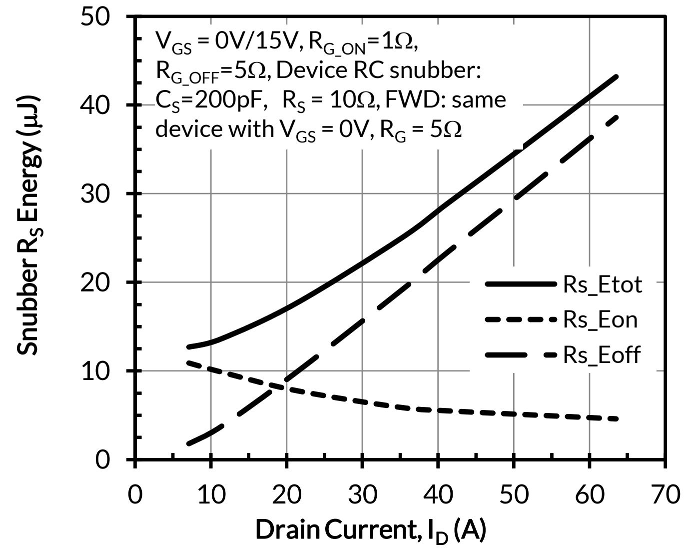


Figure 22. RC snubber energy losses vs. drain current at V_{DS} = 500V and T_J = 25°C

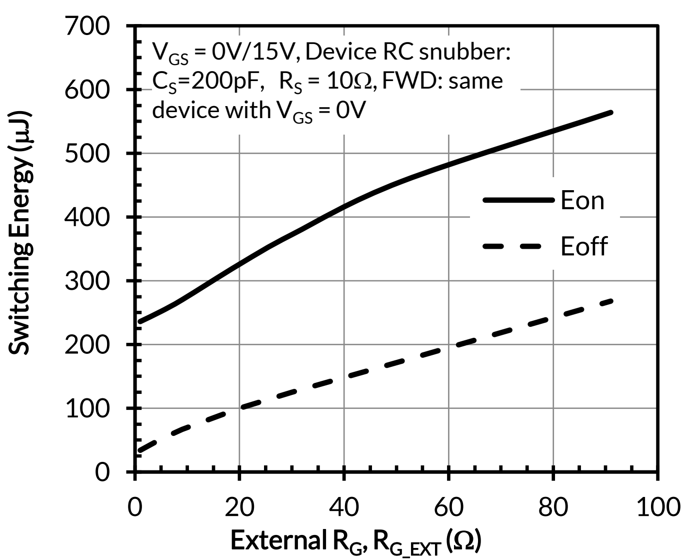


Figure 23. Clamped inductive switching energies vs. $R_{G,EXT}$ at V_{DS} = 400V, I_D = 40A, and T_J = 25°C

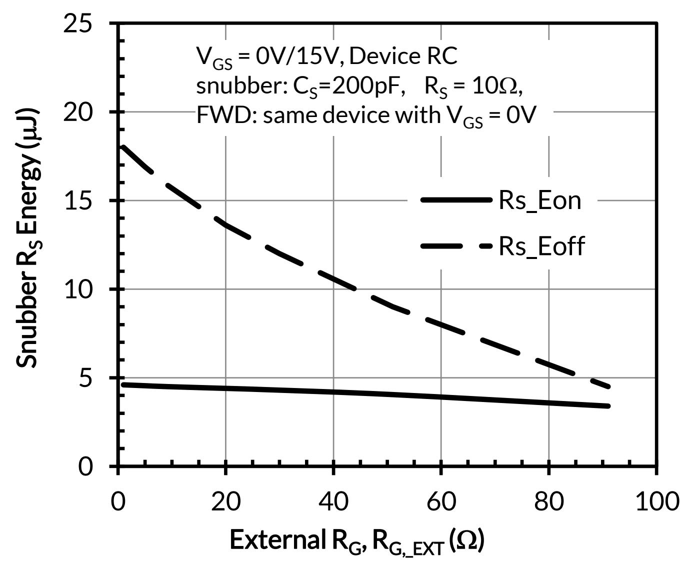


Figure 24. RC snubber energy losses vs. $R_{G,EXT}$ at V_{DS} = 400V, I_D = 40A, and T_J = 25°C

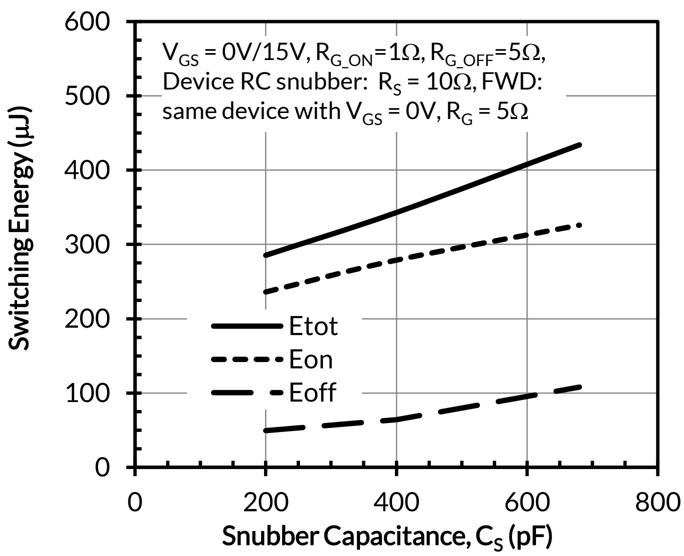


Figure 25. Clamped inductive switching energies vs. snubber capacitance C_S at V_{DS} = 400V, I_D = 40A, and T_J = 25°C

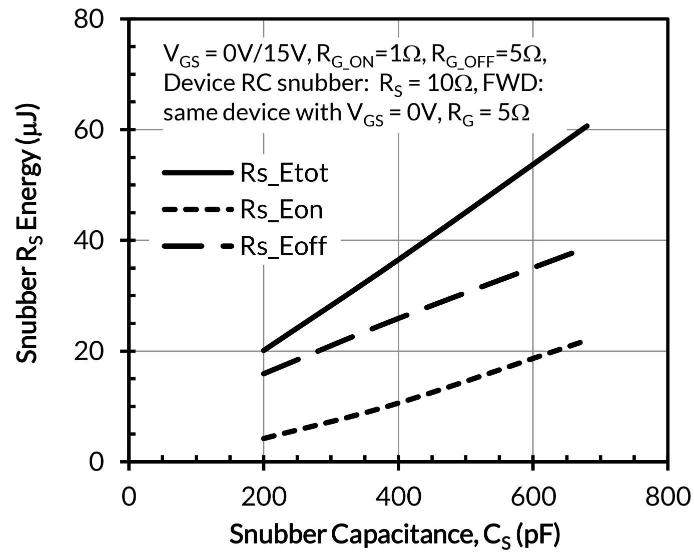


Figure 26. RC snubber energy losses vs. snubber capacitance C_S at V_{DS} = 400V, I_D = 40A, and T_J = 25°C

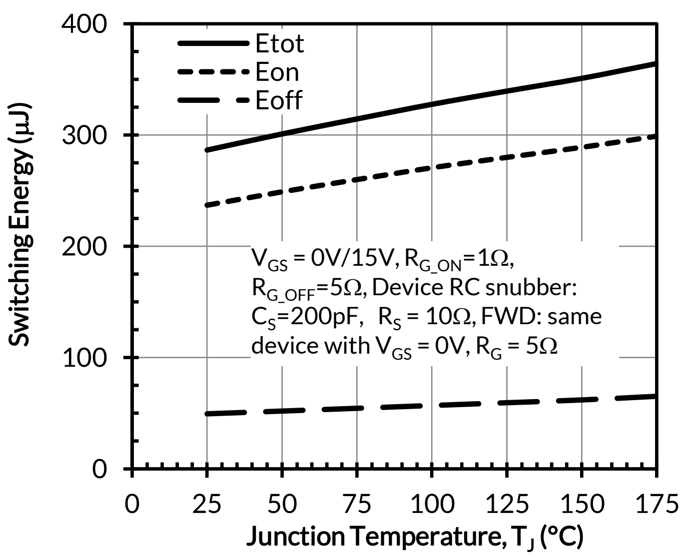


Figure 27. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D = 40A

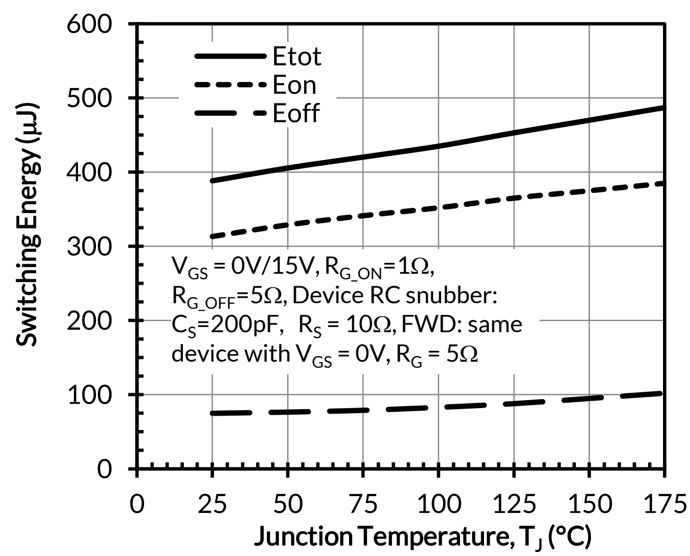


Figure 28. Clamped inductive switching energy vs. junction temperature at V_{DS} =500V and I_D = 40A

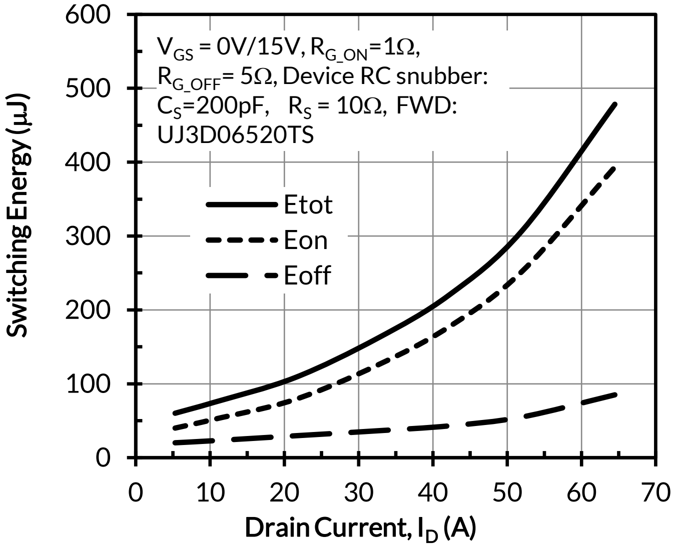


Figure 29. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

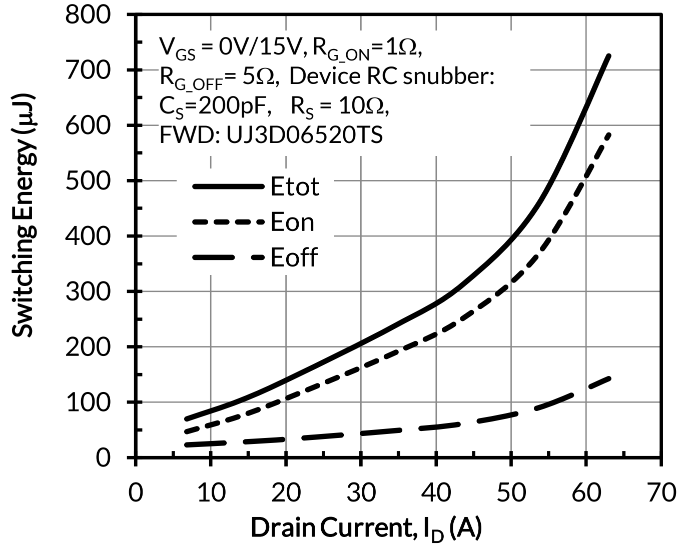


Figure 30. Clamped inductive switching energy vs. drain current at V_{DS} = 500V and T_J = 25°C

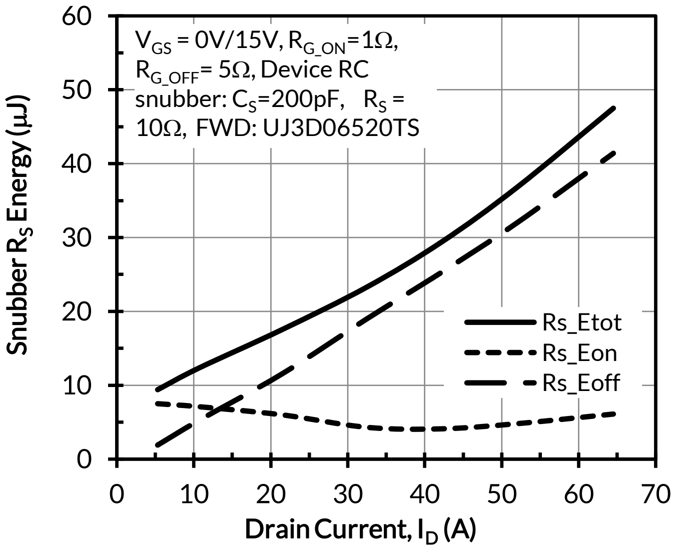


Figure 31. RC snubber energy losses vs. drain current at V_{DS} = 400V and T_J = 25°C

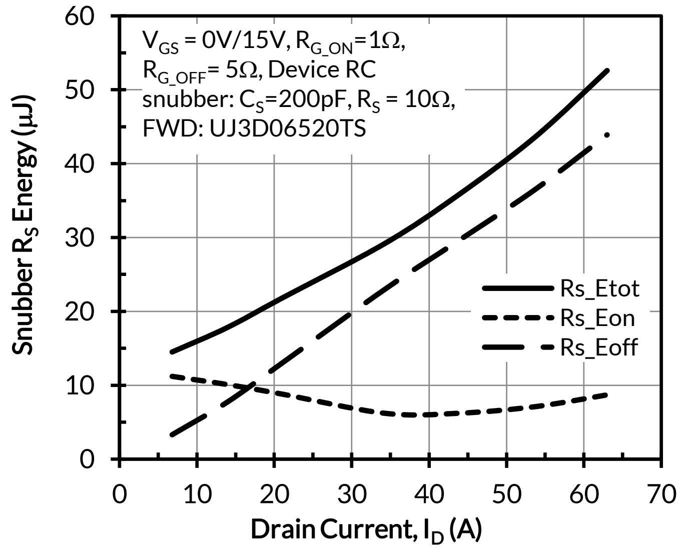


Figure 32. RC snubber energy losses vs. drain current at V_{DS} = 500V and T_J = 25°C

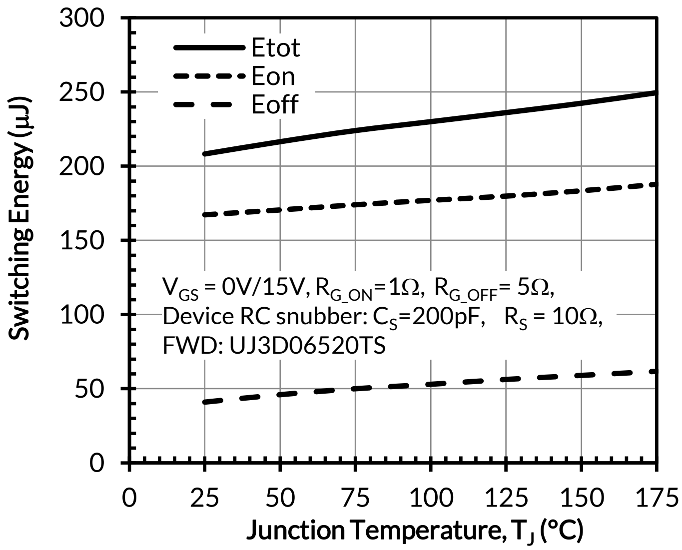


Figure 33. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D = 40A

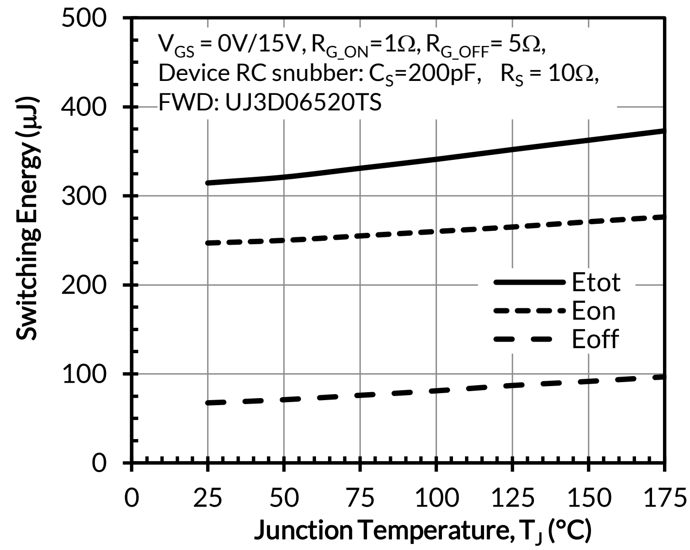


Figure 34. Clamped inductive switching energy vs. junction temperature at V_{DS} =500V and I_D = 40A

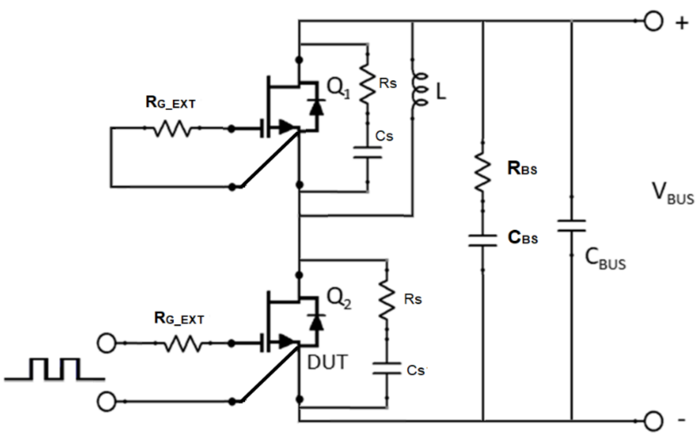


Figure 35. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF) is used to reduce the power loop high frequency oscillations.

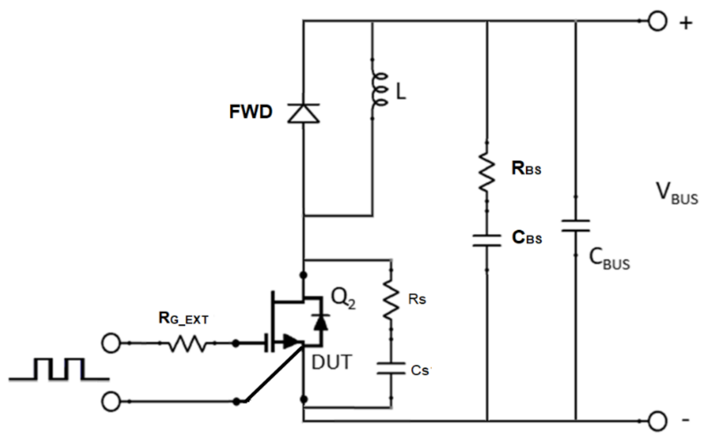


Figure 36. Schematic of the chopper mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF) is used to reduce the power loop high frequency oscillations.