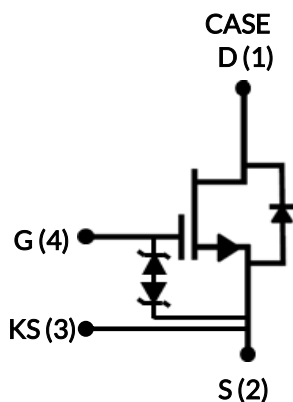


DATASHEET

UJ4C075060K4S



750V-58mΩ SiC FET

Rev. A, October 2020

Description

The UJ4C075060K4S is a 750V, 58mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- ◆ On-resistance $R_{DS(on)}$: 58mΩ (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 52nC
- ◆ Low body diode V_{FSD} : 1.31V
- ◆ Low gate charge: Q_G = 37.8nC
- ◆ Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ TO-247-4L package for faster switching, clean gate waveforms

Part Number	Package	Marking
UJ4C075060K4S	TO-247-4L	UJ4C075060K4S



Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
Continuous drain current ¹	I_D	$T_C = 25^\circ\text{C}$	28	A
		$T_C = 100^\circ\text{C}$	20.6	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	62	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}, I_{AS}=1.8\text{A}$	24.3	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	155	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	$^\circ\text{C}$

1. Limited by $T_{J,max}$

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.75	0.97	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750V, V_{GS}=0V, T_J=25^\circ\text{C}$		0.7	40	μA
		$V_{DS}=750V, V_{GS}=0V, T_J=175^\circ\text{C}$		15		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		4.7	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=20A, T_J=25^\circ\text{C}$		58	74	m Ω
		$V_{GS}=12V, I_D=20A, T_J=125^\circ\text{C}$		106		
		$V_{GS}=12V, I_D=20A, T_J=175^\circ\text{C}$		147		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	4.8	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			28	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			62	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_F=10A, T_J=25^\circ\text{C}$		1.31	1.75	V
		$V_{GS}=0V, I_F=10A, T_J=175^\circ\text{C}$		1.8		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=20A, V_{GS}=0V, R_{G,EXT}=20\Omega$		52		nC
Reverse recovery time	t_{rr}	di/dt=1060A/ $\mu\text{s}, T_J=25^\circ\text{C}$		16		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=20A, V_{GS}=0V, R_{G,EXT}=20\Omega$		58		nC
Reverse recovery time	t_{rr}	di/dt=1060A/ $\mu\text{s}, T_J=150^\circ\text{C}$		19		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1422		pF	
Output capacitance	C_{oss}			68			
Reverse transfer capacitance	C_{rss}			2.7			
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		50		pF	
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		94		pF	
C_{oss} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		4		μJ	
Total gate charge	Q_G	$V_{DS}=400V, I_D=20A,$ $V_{GS} = 0V$ to 15V		37.8		nC	
Gate-drain charge	Q_{GD}			8			
Gate-source charge	Q_{GS}			11.8			
Turn-on delay time	$t_{d(on)}$	Note 4, $V_{DS}=400V, I_D=20A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: same device with $V_{GS} = 0V, R_G = 20\Omega,$ $T_J=25^\circ C$		12		ns	
Rise time	t_r			19			
Turn-off delay time	$t_{d(off)}$			78			
Fall time	t_f			12			
Turn-on energy	E_{ON}			126			
Turn-off energy	E_{OFF}		37		μJ		
Total switching energy	E_{TOTAL}		163				
Turn-on delay time	$t_{d(on)}$	Note 4, $V_{DS}=400V, I_D=20A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1\Omega,$ Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: same device with $V_{GS} = 0V, R_G = 20\Omega,$ $T_J=150^\circ C$		12		ns	
Rise time	t_r			21			
Turn-off delay time	$t_{d(off)}$			83			
Fall time	t_f			14			
Turn-on energy	E_{ON}			151			
Turn-off energy	E_{OFF}			50			μJ
Total switching energy	E_{TOTAL}			201			

4. Measured with the half-bridge mode switching test circuit in Figure 28.

Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Turn-on delay time	$t_{d(on)}$	Note 5, $V_{DS}=400V$, $I_D=20A$, Gate Driver = 0V to +15V, $R_{G,EXT}=1\Omega$, inductive Load, FWD: same device with $V_{GS}=0V$ and $R_G=1\Omega$, RC snubber: $R_{S1}=10\Omega$ and $C_{S1}=95pF$, $T_J=25^\circ C$		12		ns	
Rise time	t_r			22			
Turn-off delay time	$t_{d(off)}$			31			
Fall time	t_f			9			
Turn-on energy including R_S energy	E_{ON}		FWD: same device with $V_{GS}=0V$ and $R_G=1\Omega$, RC snubber: $R_{S1}=10\Omega$ and $C_{S1}=95pF$, $T_J=25^\circ C$		142		μJ
Turn-off energy including R_S energy	E_{OFF}				17		
Total switching energy	E_{TOTAL}				159		
Snubber R_S energy during turn-on	E_{RS_ON}				0.7		
Snubber R_S energy during turn-off	E_{RS_OFF}				1		
Turn-on delay time	$t_{d(on)}$	Note 5, $V_{DS}=400V$, $I_D=20A$, Gate Driver = 0V to +15V, $R_{G,EXT}=1\Omega$, inductive Load, FWD: same device with $V_{GS}=0V$ and $R_G=1\Omega$, RC snubber: $R_{S1}=10\Omega$ and $C_{S1}=95pF$, $T_J=150^\circ C$		12		ns	
Rise time	t_r			25			
Turn-off delay time	$t_{d(off)}$			35			
Fall time	t_f			9			
Turn-on energy including R_S energy	E_{ON}		FWD: same device with $V_{GS}=0V$ and $R_G=1\Omega$, RC snubber: $R_{S1}=10\Omega$ and $C_{S1}=95pF$, $T_J=150^\circ C$		153		μJ
Turn-off energy including R_S energy	E_{OFF}				18		
Total switching energy	E_{TOTAL}				171		
Snubber R_S energy during turn-on	E_{RS_ON}				0.7		
Snubber R_S energy during turn-off	E_{RS_OFF}				1		
Turn-on delay time	$t_{d(on)}$	Note 6, $V_{DS}=400V$, $I_D=20A$, Gate Driver = 0V to +15V, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: UJ3D06510TS $T_J=25^\circ C$		12		ns	
Rise time	t_r			18			
Turn-off delay time	$t_{d(off)}$			78			
Fall time	t_f			12		μJ	
Turn-on energy	E_{ON}			90			
Turn-off energy	E_{OFF}			37			
Total switching energy	E_{TOTAL}			127			
Turn-on delay time	$t_{d(on)}$	Note 6, $V_{DS}=400V$, $I_D=20A$, Gate Driver = 0V to +15V, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: UJ3D06510TS $T_J=150^\circ C$		12		ns	
Rise time	t_r			19			
Turn-off delay time	$t_{d(off)}$			84			
Fall time	t_f			15			
Turn-on energy	E_{ON}			104		μJ	
Turn-off energy	E_{OFF}			49			
Total switching energy	E_{TOTAL}			153			

5. Measured with the chopper mode switching test circuit in Figure 30.

6. Measured with the chopper mode switching test circuit in Figure 29.

Typical Performance Diagrams

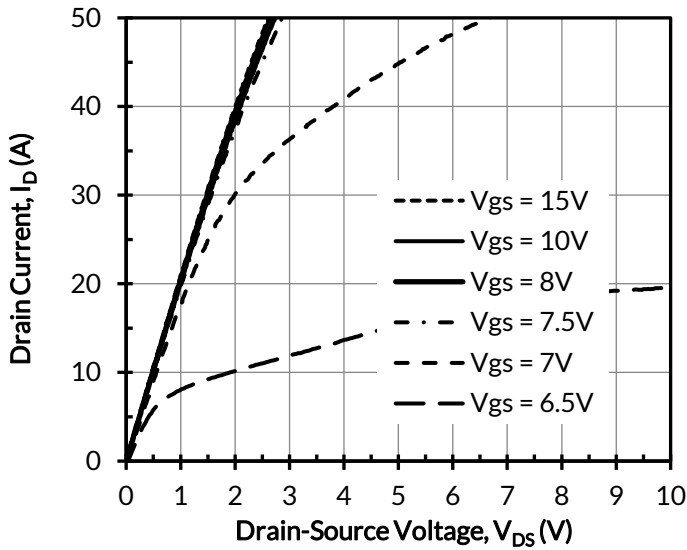


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

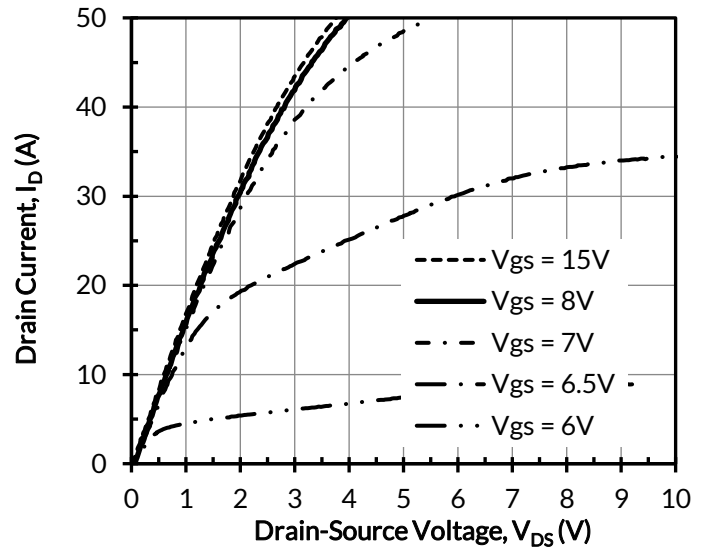


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

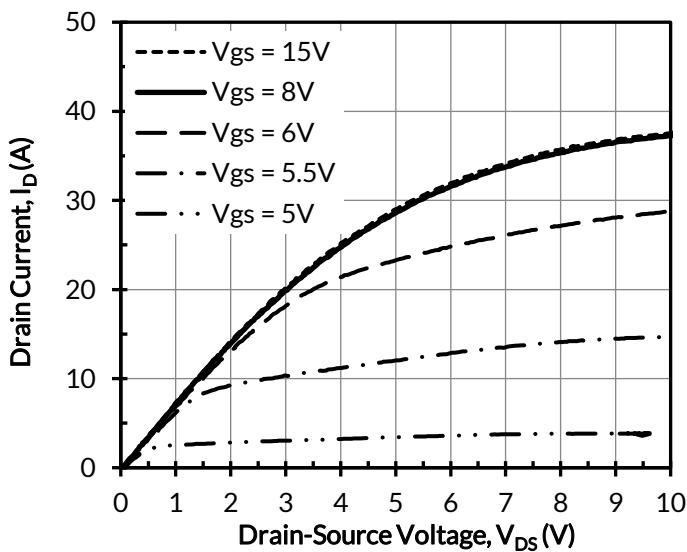


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

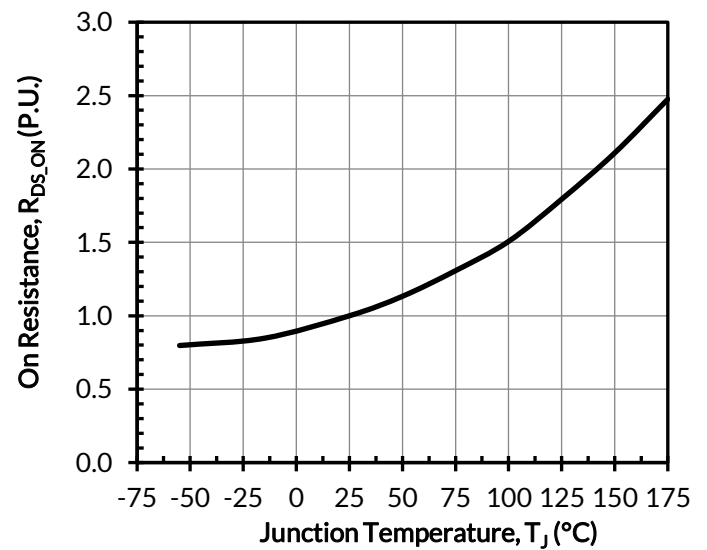


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 20\text{A}$

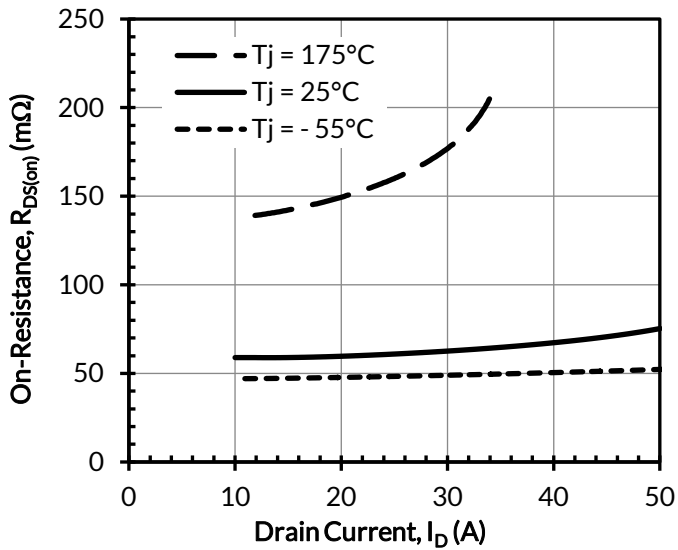


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12\text{V}$

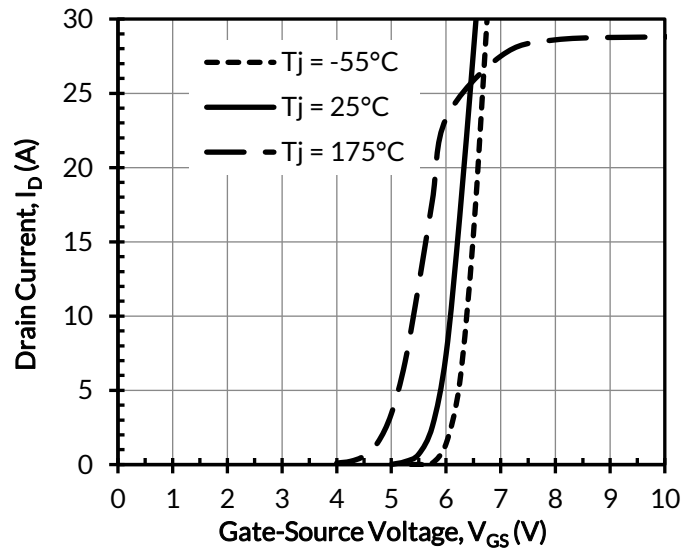


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

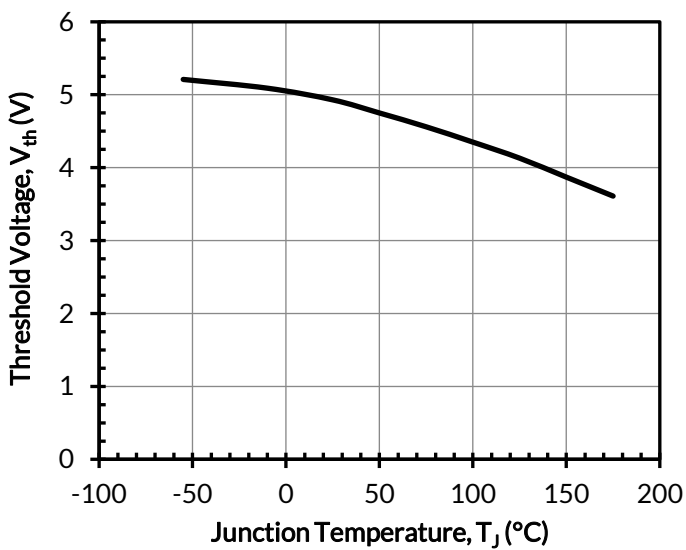


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5\text{V}$ and $I_D = 10\text{mA}$

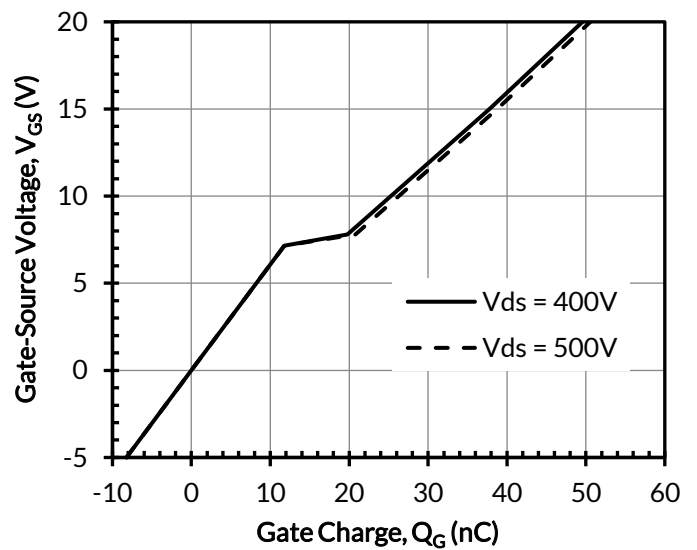


Figure 8. Typical gate charge at $I_D = 20\text{A}$

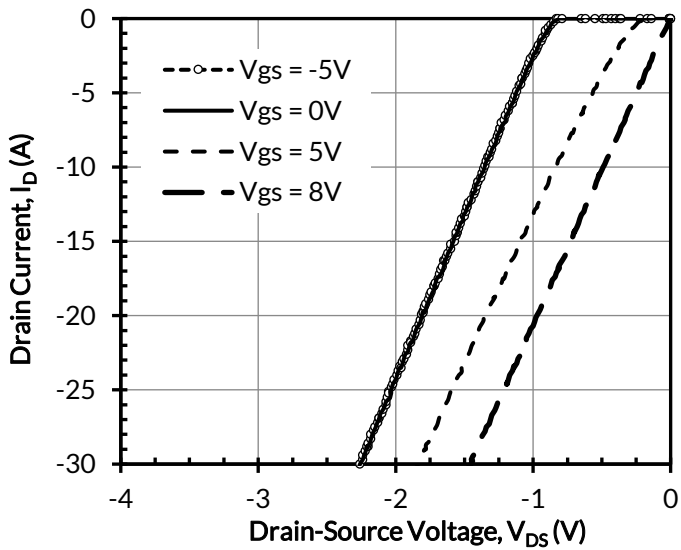


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

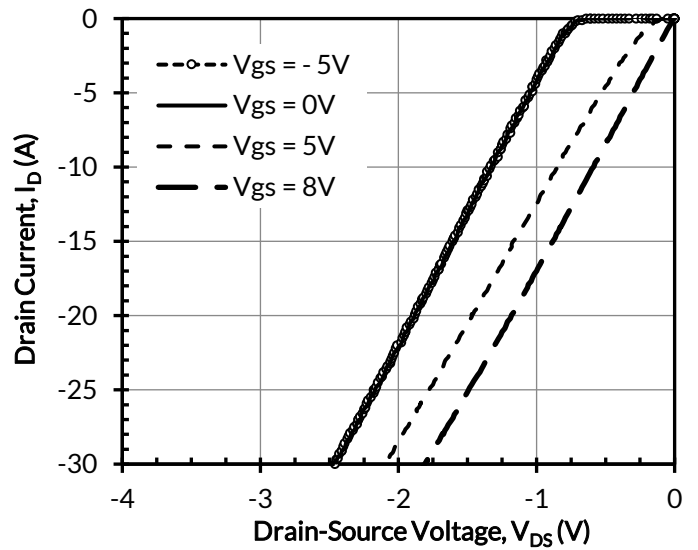


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

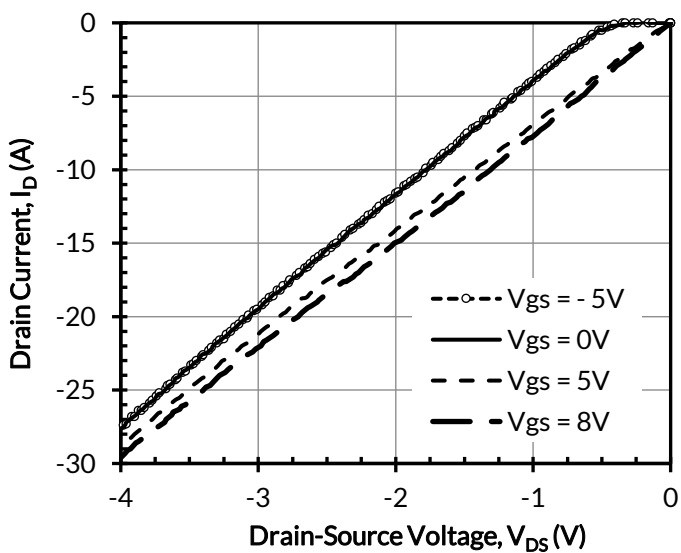


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

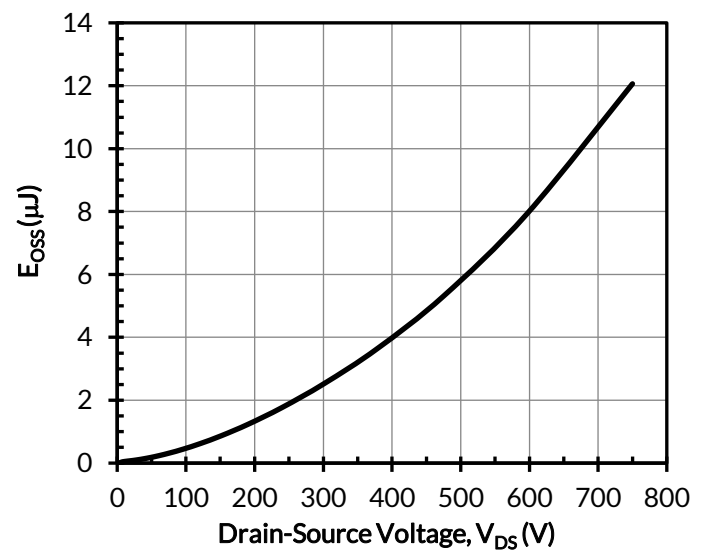


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

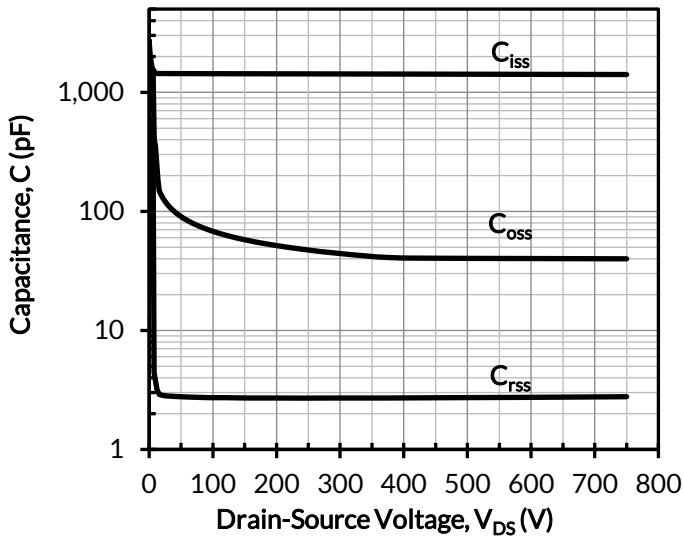


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

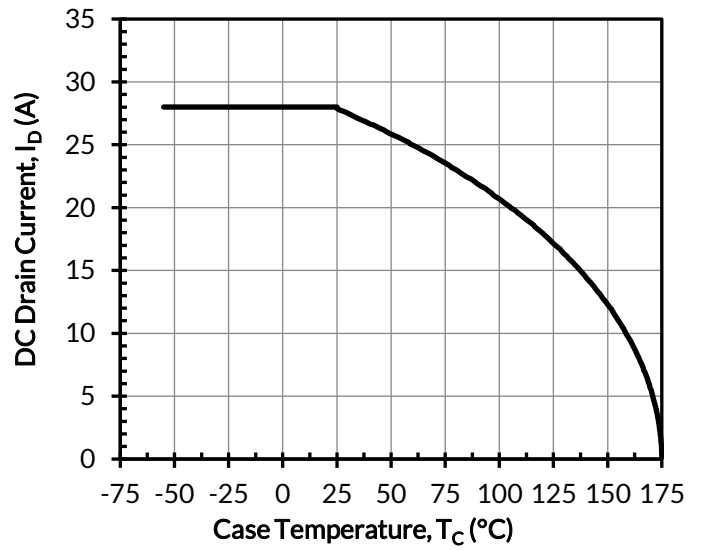


Figure 14. DC drain current derating

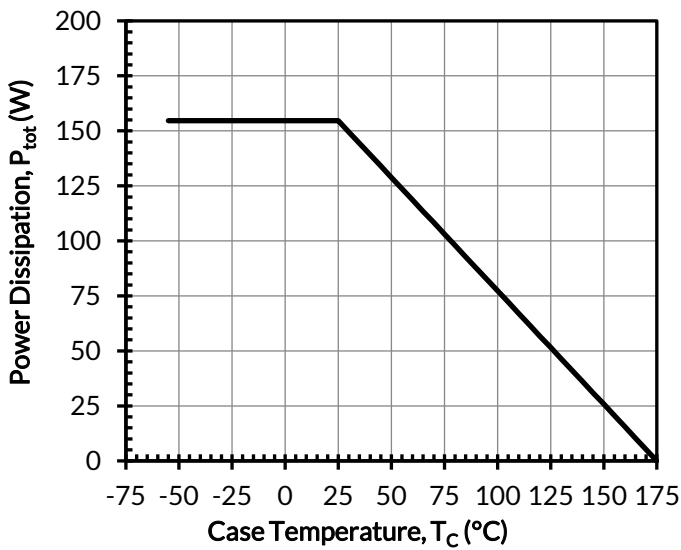


Figure 15. Total power dissipation

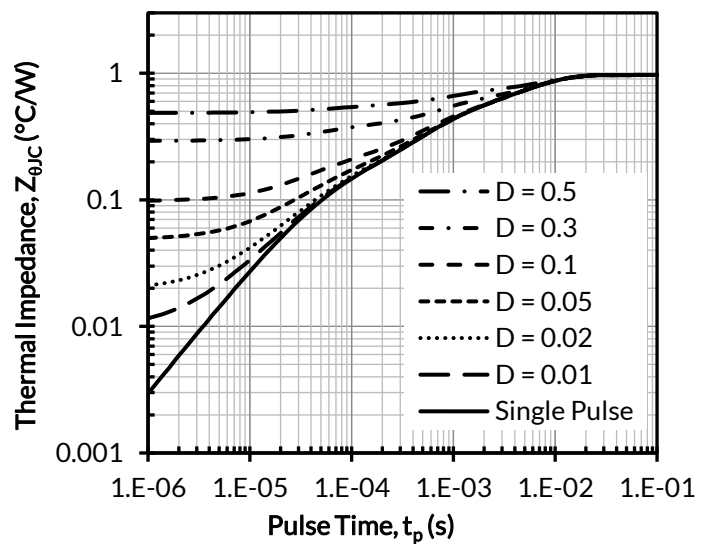


Figure 16. Maximum transient thermal impedance

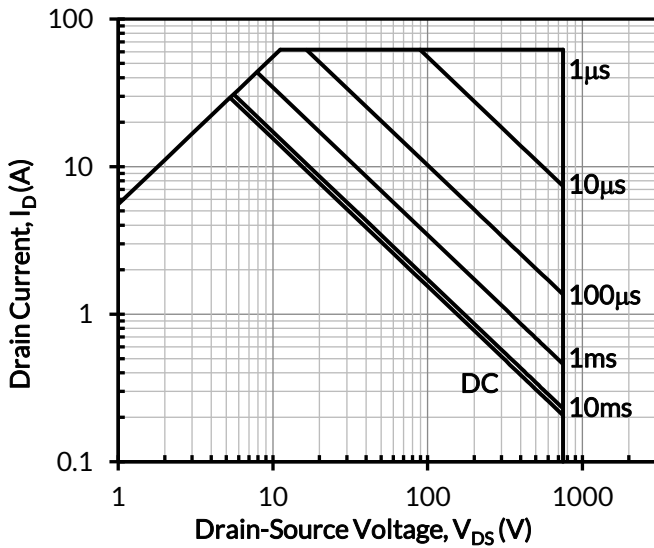


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

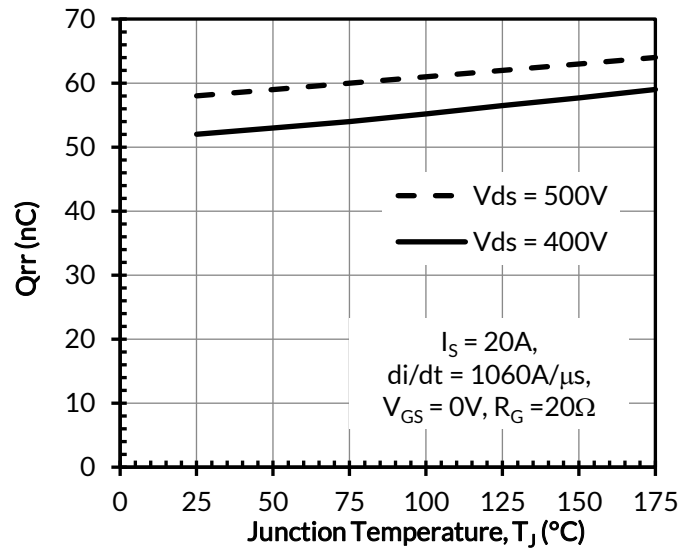


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

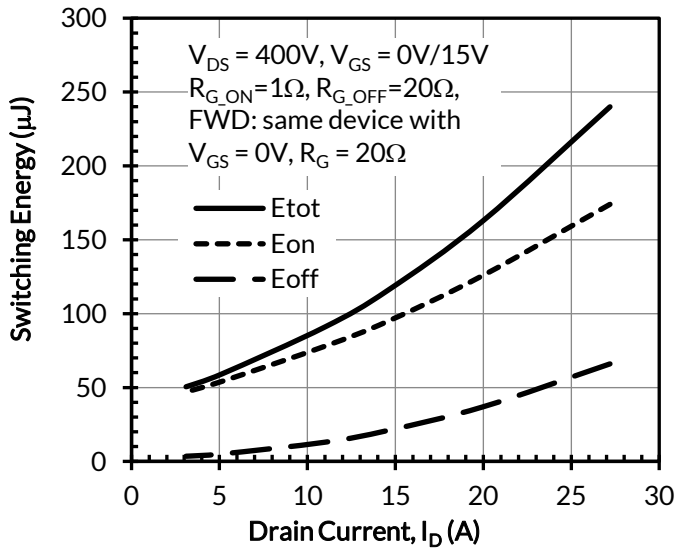


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

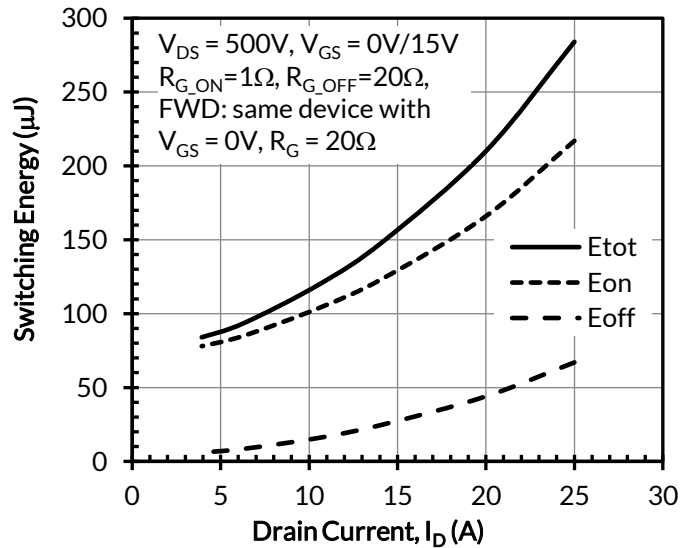


Figure 20. Clamped inductive switching energy vs. drain current at $V_{DS} = 500\text{V}$ and $T_J = 25^\circ\text{C}$

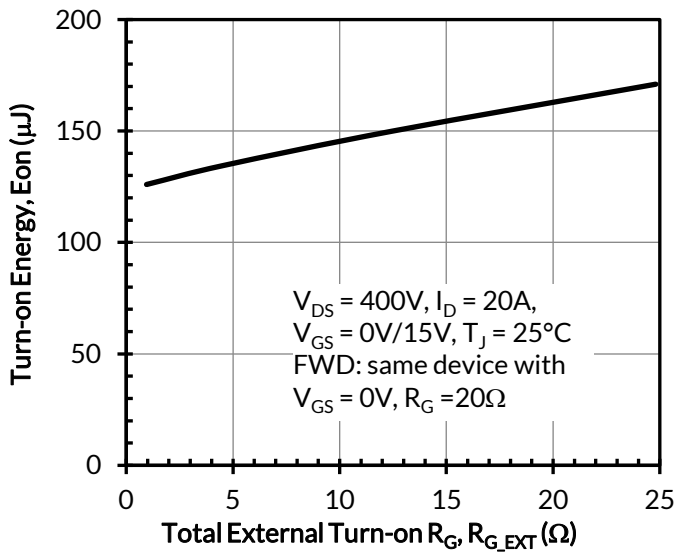


Figure 21. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

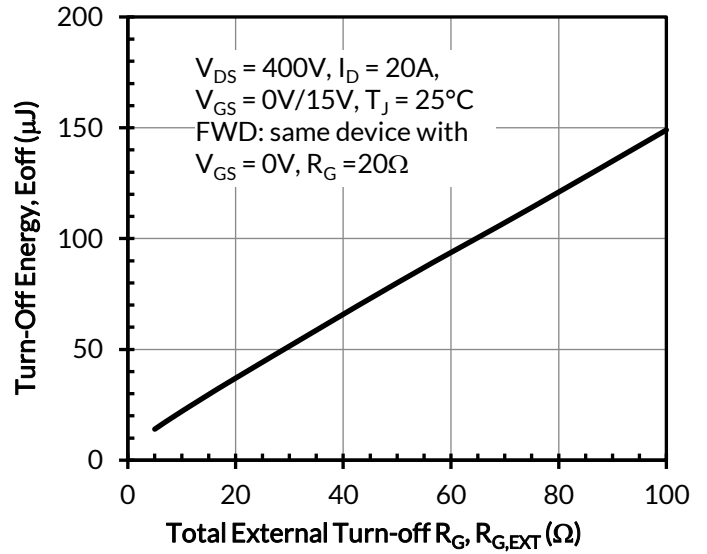


Figure 22. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

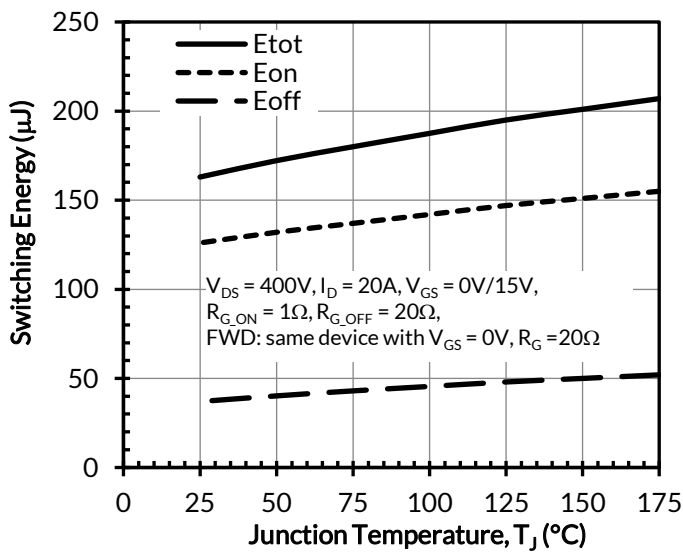


Figure 23. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 400V$ and $I_D = 20A$

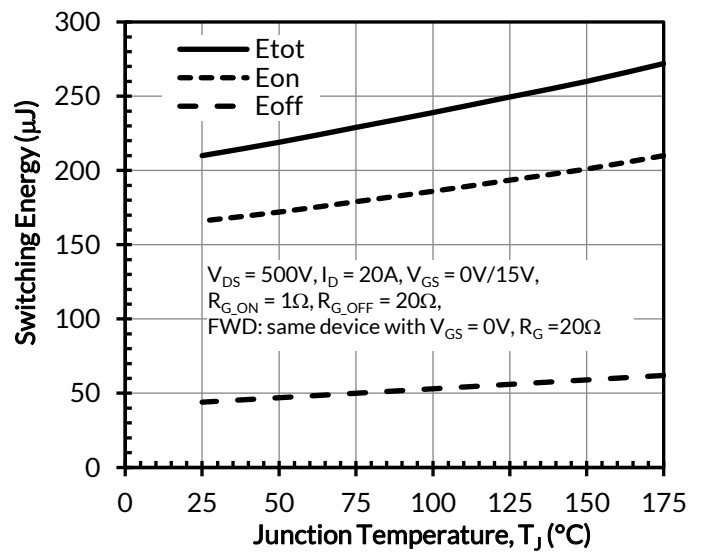


Figure 24. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 500V$ and $I_D = 20A$

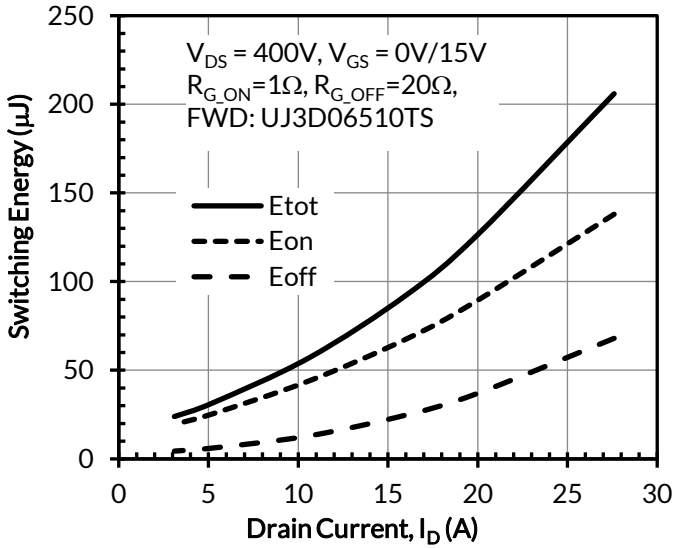


Figure 24. Clamped inductive switching energy vs. drain current at $V_{DS} = 400V$ and $T_J = 25^\circ C$

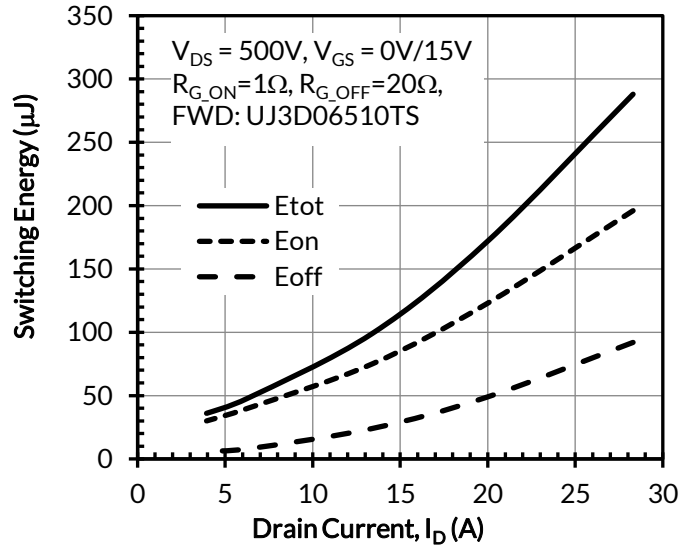


Figure 25. Clamped inductive switching energy vs. drain current at $V_{DS} = 500V$ and $T_J = 25^\circ C$

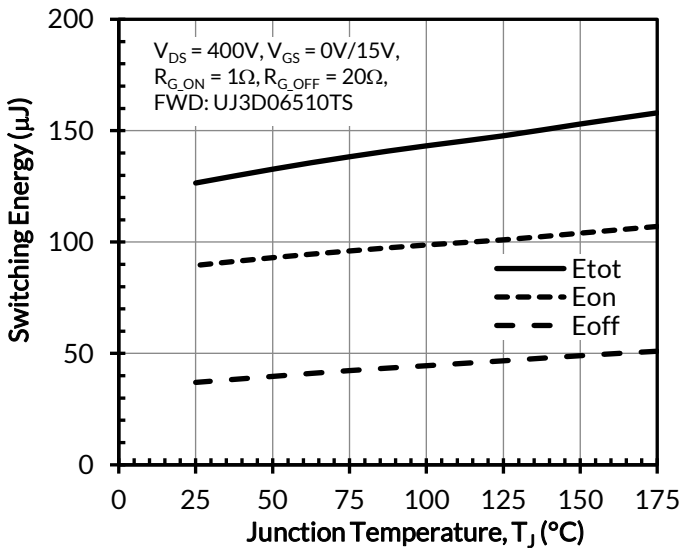


Figure 26. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 400V$ and $I_D = 20A$

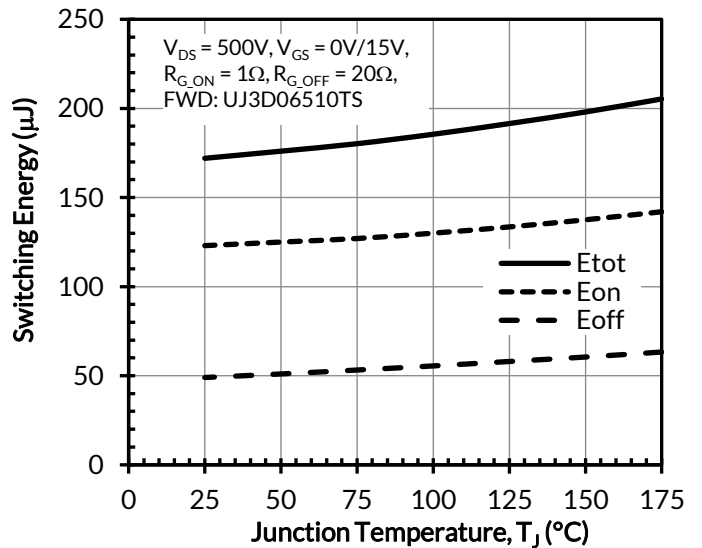


Figure 27. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 500V$ and $I_D = 20A$

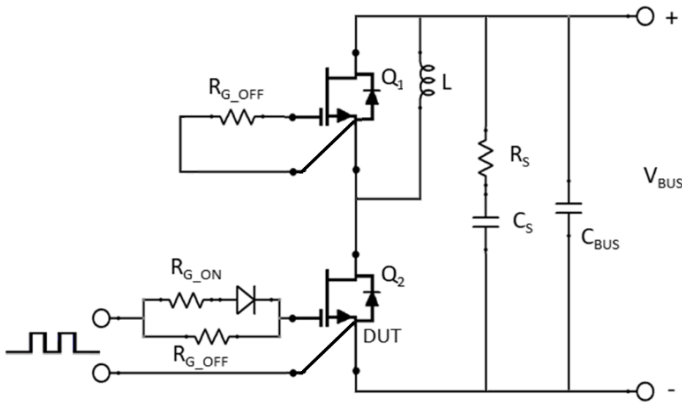


Figure 28. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_S = 2.5\Omega$, $C_S = 100\text{nF}$) is used to reduce the power loop high frequency oscillations.

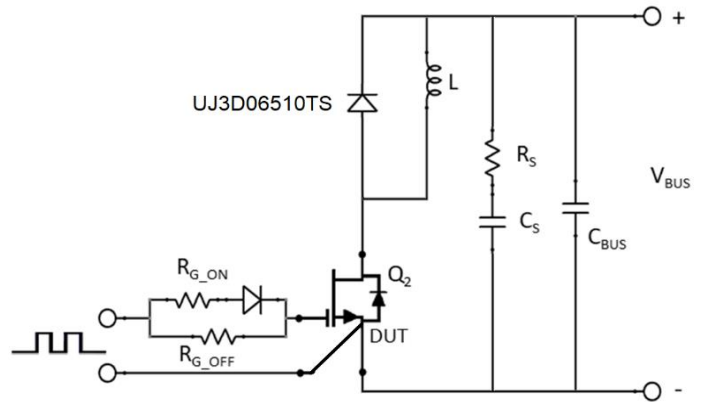


Figure 29. Schematic of the chopper mode switching test circuit. Note, a bus RC snubber ($R_S = 2.5\Omega$, $C_S = 100\text{nF}$) is used to reduce the power loop high frequency oscillations.

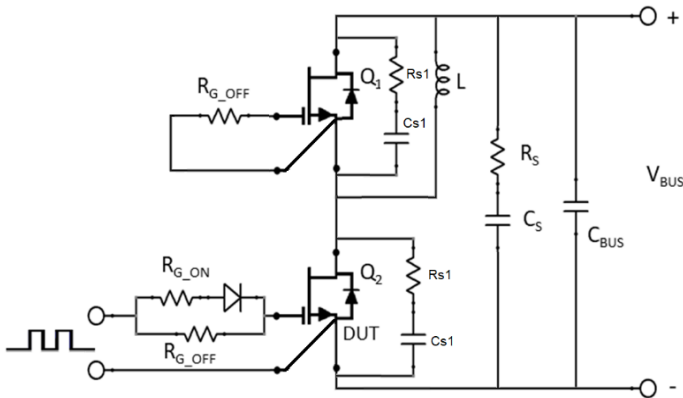


Figure 30. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_{S1} = 10\Omega$, $C_{S1} = 95\text{pF}$) and a bus RC snubber ($R_S = 2.5\Omega$, $C_S = 100\text{nF}$).