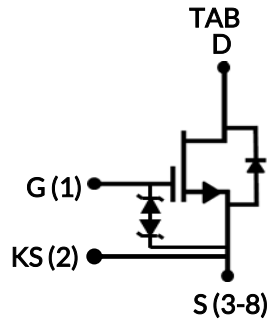
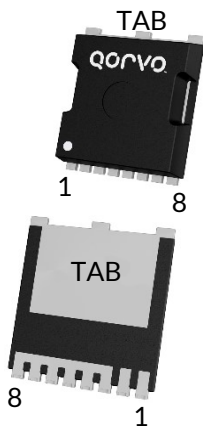


DATASHEET

UJ4SC075008L8S



750V-8.6mΩ SiC FET

Rev. A, February 2023

Description

The UJ4SC075008L8S is a 750V, 8.6mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving MO-229 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- ◆ On-resistance $R_{DS(on)}$: 8.6mΩ (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 338nC
- ◆ Low body diode V_{FSD} : 1.1V
- ◆ Low gate charge: Q_G = 75nC
- ◆ Threshold voltage $V_{G(th)}$: 4.5V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ MO-229 package for faster switching, clean gate waveforms

Typical applications

- ◆ Solid state relays and circuit-breakers
- ◆ Line rectification and active-bridge rectification circuits in AC/DC front-ends
- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

Part Number	Package	Marking
UJ4SC075008L8S	MO-229	UJ4SC075008



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C < 104^\circ\text{C}$	106	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	344	A
Single pulsed avalanche energy ³	E_{AS}	L=15mH, $I_{AS} = 5.2\text{A}$	202	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500\text{V}$	100	V/ns
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	600	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	$^\circ\text{C}$

- Limited by bondwires
- Pulse width t_p limited by $T_{J,max}$
- Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.19	0.25	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750V, V_{GS}=0V, T_J=25^\circ\text{C}$		4	84	μA
		$V_{DS}=750V, V_{GS}=0V, T_J=175^\circ\text{C}$		35		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		2	20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=70A, T_J=25^\circ\text{C}$		8.6	11.4	m Ω
		$V_{GS}=12V, I_D=70A, T_J=125^\circ\text{C}$		14.4		
		$V_{GS}=12V, I_D=70A, T_J=175^\circ\text{C}$		19		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	3.5	4.5	5.5	V
Gate resistance	R_G	$f=1\text{MHz}, \text{open drain}$		2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C < 104^\circ\text{C}$			106	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			344	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_S=35A, T_J=25^\circ\text{C}$		1.10	1.24	V
		$V_{GS}=0V, I_S=35A, T_J=175^\circ\text{C}$		1.14		
Reverse recovery charge	Q_{rr}	$V_{DS}=400V, I_S=70A, V_{GS}=0V, R_G=33\Omega$		338		nC
Reverse recovery time	t_{rr}	$di/dt=2500A/\mu\text{s}, T_J=25^\circ\text{C}$		29		ns
Reverse recovery charge	Q_{rr}	$V_{DS}=400V, I_S=70A, V_{GS}=0V, R_G=33\Omega$		375		nC
Reverse recovery time	t_{rr}	$di/dt=2500A/\mu\text{s}, T_J=150^\circ\text{C}$		32		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units	
			Min	Typ	Max		
Input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V$ $f=100kHz$		3340		pF	
Output capacitance	C_{oss}			230			
Reverse transfer capacitance	C_{rss}			1.4			
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to $400V$, $V_{GS}=0V$		286		pF	
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to $400V$, $V_{GS}=0V$		605		pF	
C_{OSS} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		23		μJ	
Total gate charge	Q_G	$V_{DS}=400V, I_D=70A$, $V_{GS} = 0V$ to $15V$		75		nC	
Gate-drain charge	Q_{GD}			13			
Gate-source charge	Q_{GS}			22			
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, $V_{DS}=400V, I_D=70A$, Gate Driver = $0V$ to $+15V$, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=5\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$, RC snubber: $R_S=5\Omega$ and $C_S=560pF$, $T_J=25^\circ C$		17		ns	
Rise time	t_r			25			
Turn-off delay time	$t_{d(off)}$			65			
Fall time	t_f			14			
Turn-on energy including R_S energy	E_{ON}			220			
Turn-off energy including R_S energy	E_{OFF}		181		μJ		
Total switching energy	E_{TOTAL}		401				
Snubber R_S energy during turn-on	E_{RS_ON}		13				
Snubber R_S energy during turn-off	E_{RS_OFF}		50				
Turn-on delay time	$t_{d(on)}$	Notes 4 and 5, $V_{DS}=400V, I_D=70A$, Gate Driver = $0V$ to $+15V$, Turn-on $R_{G,EXT}=1\Omega$, Turn-off $R_{G,EXT}=5\Omega$, inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega$, RC snubber: $R_S=5\Omega$ and $C_S=560pF$, $T_J=150^\circ C$		18		ns	
Rise time	t_r			28			
Turn-off delay time	$t_{d(off)}$			68			
Fall time	t_f			13			
Turn-on energy including R_S energy	E_{ON}			245			
Turn-off energy including R_S energy	E_{OFF}			211			
Total switching energy	E_{TOTAL}			456			μJ
Snubber R_S energy during turn-on	E_{RS_ON}			13			
Snubber R_S energy during turn-off	E_{RS_OFF}			50			

4. Measured with the switching test circuit in Figure 26.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

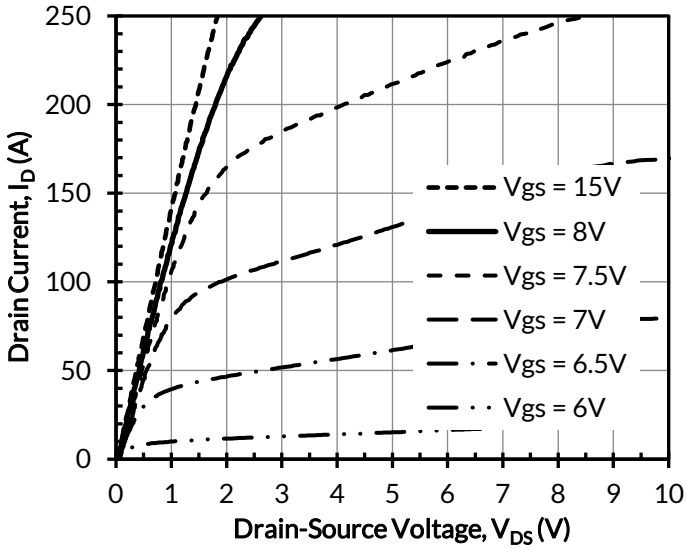


Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

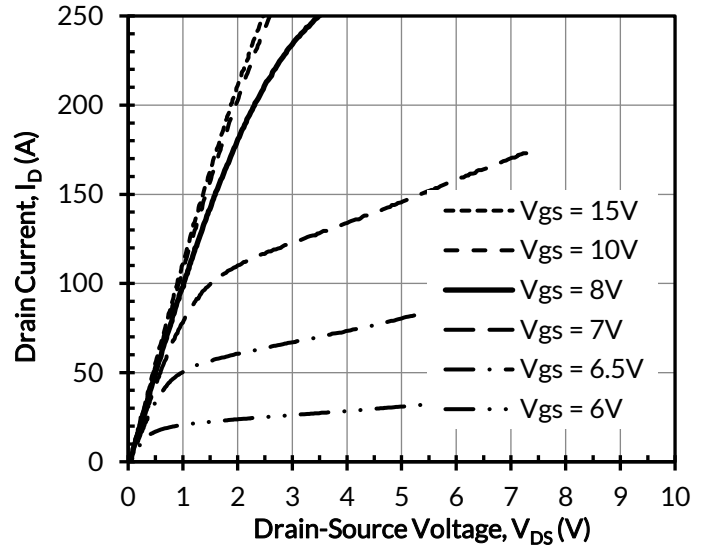


Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

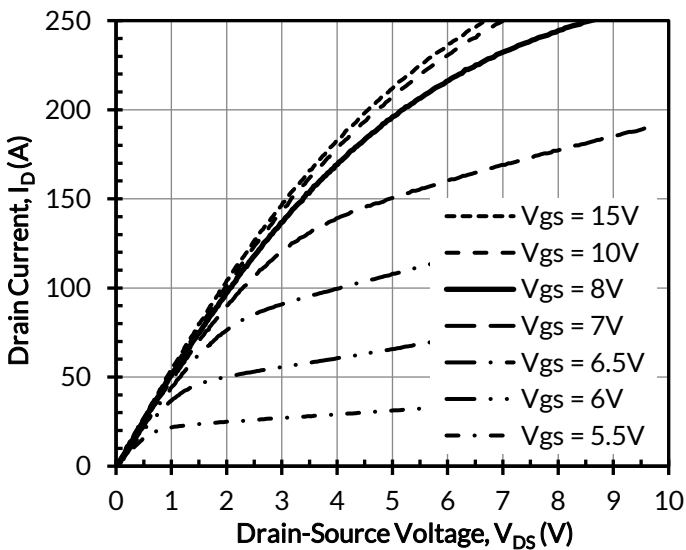


Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

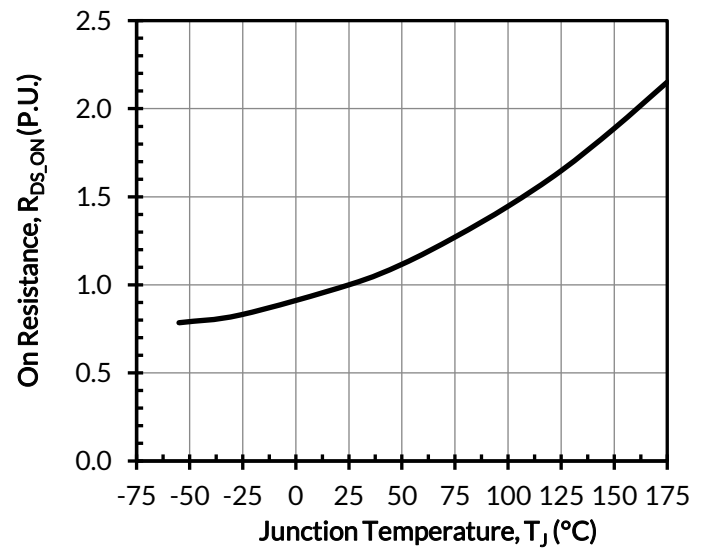


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 70\text{A}$

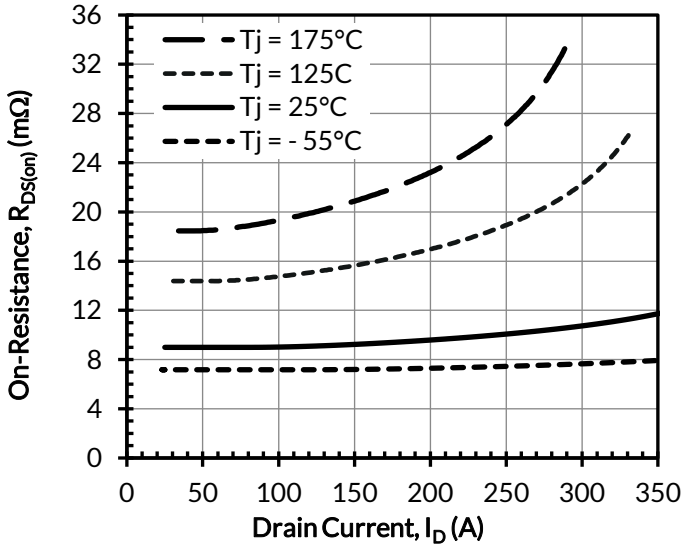


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

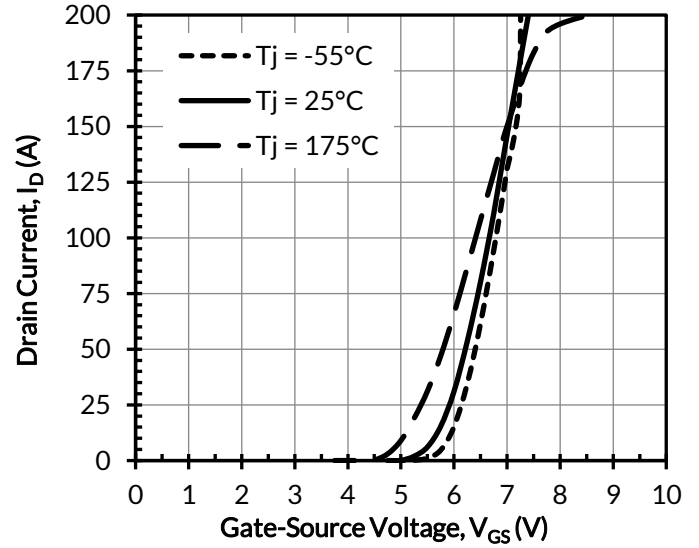


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

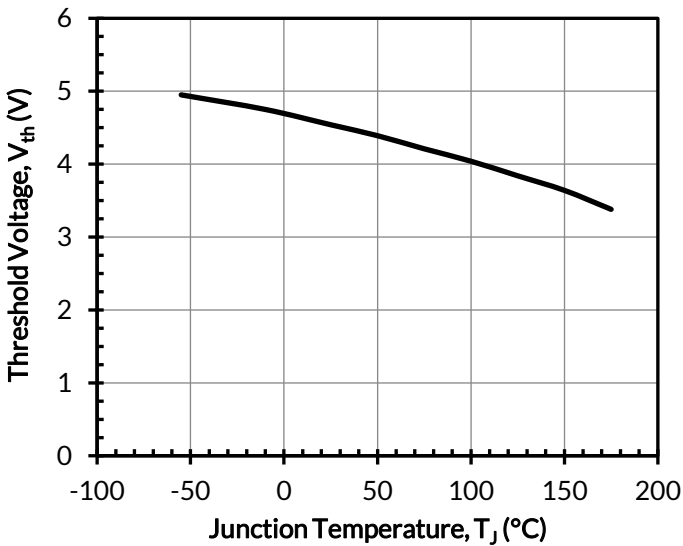


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

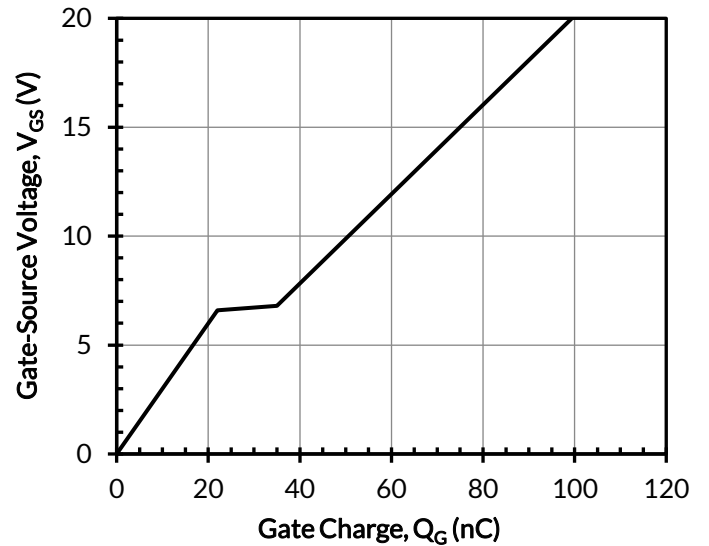


Figure 8. Typical gate charge at $V_{DS} = 400V$ and $I_D = 70A$

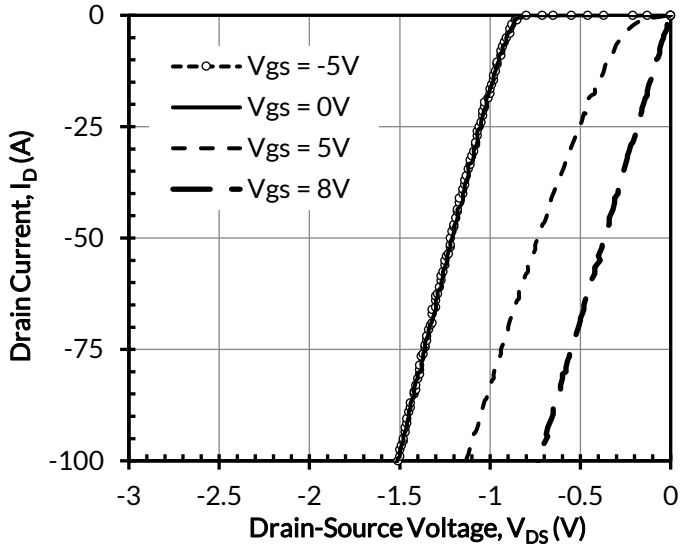


Figure 9. 3rd quadrant characteristics at $T_J = -55^\circ\text{C}$

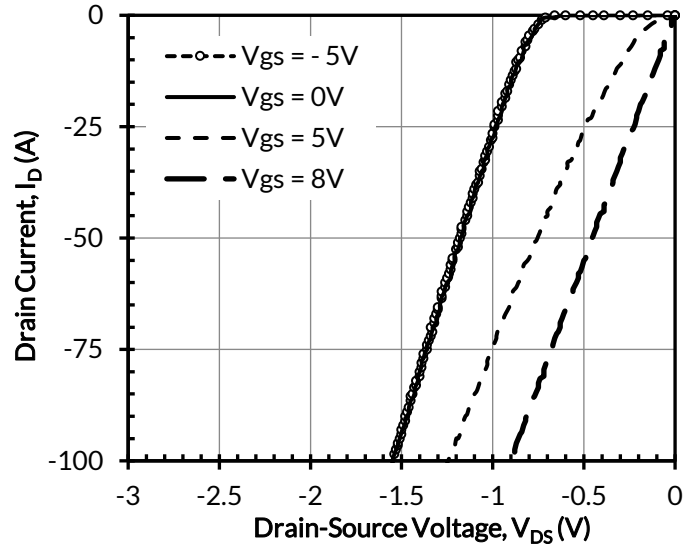


Figure 10. 3rd quadrant characteristics at $T_J = 25^\circ\text{C}$

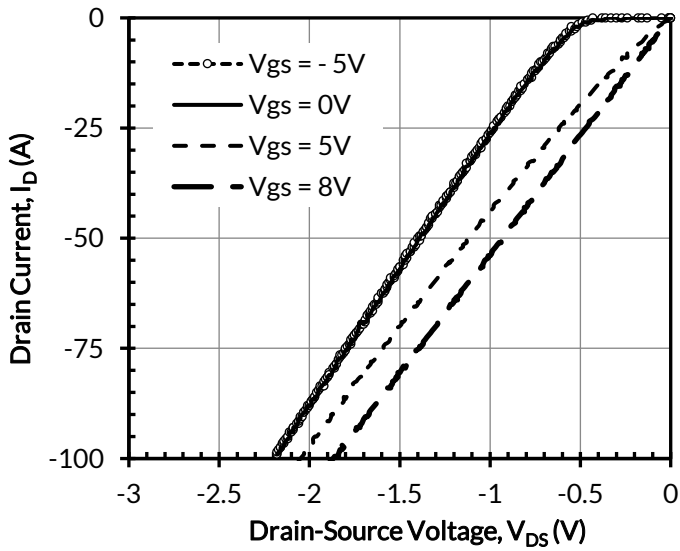


Figure 11. 3rd quadrant characteristics at $T_J = 175^\circ\text{C}$

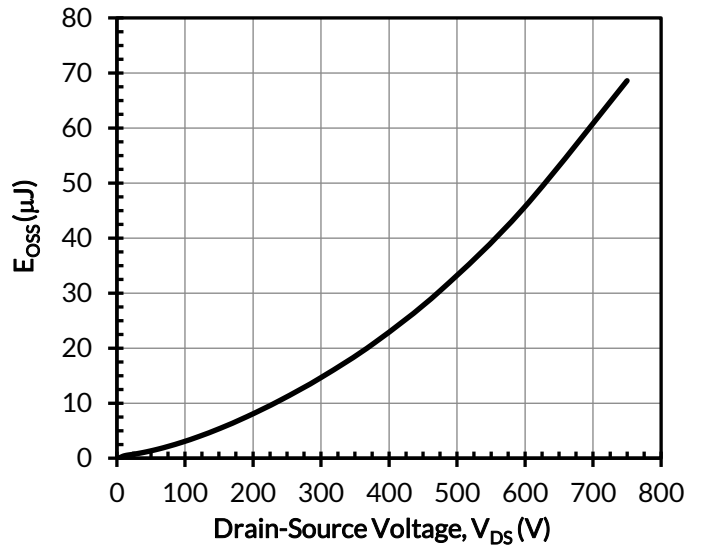


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

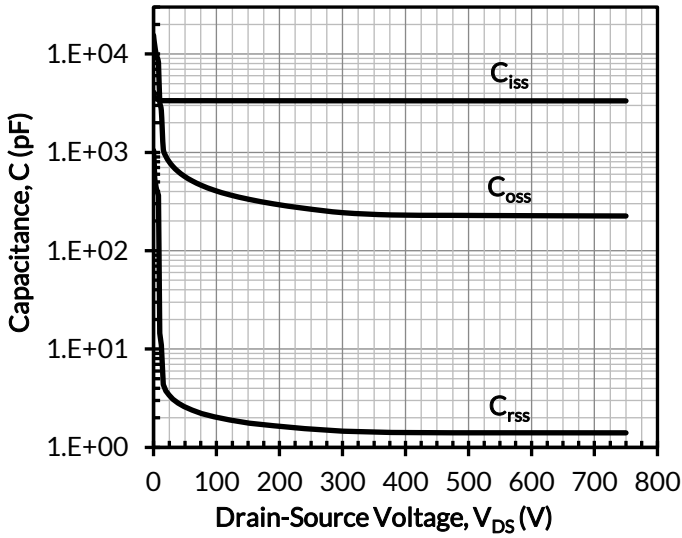


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

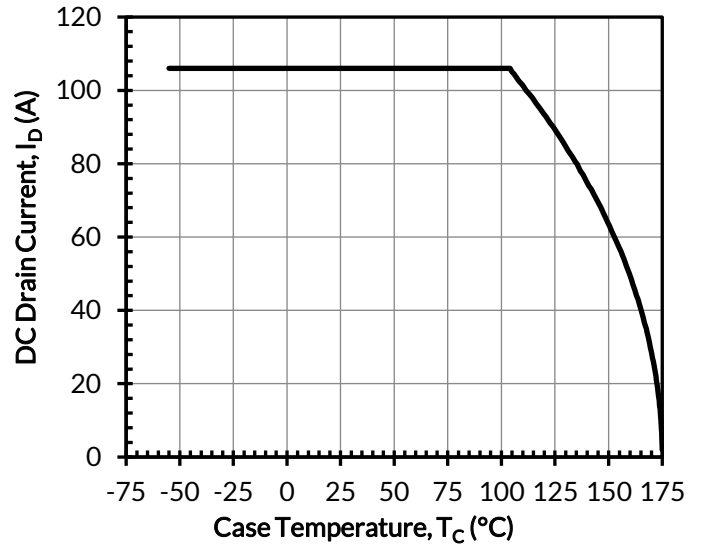


Figure 14. DC drain current derating

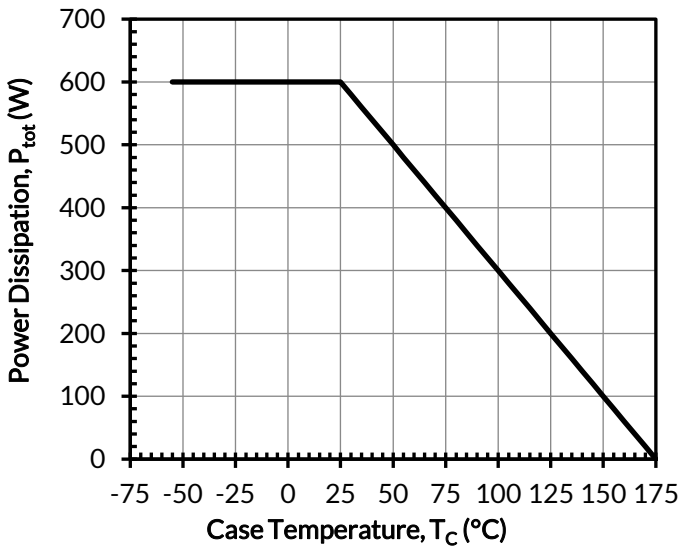


Figure 15. Total power dissipation

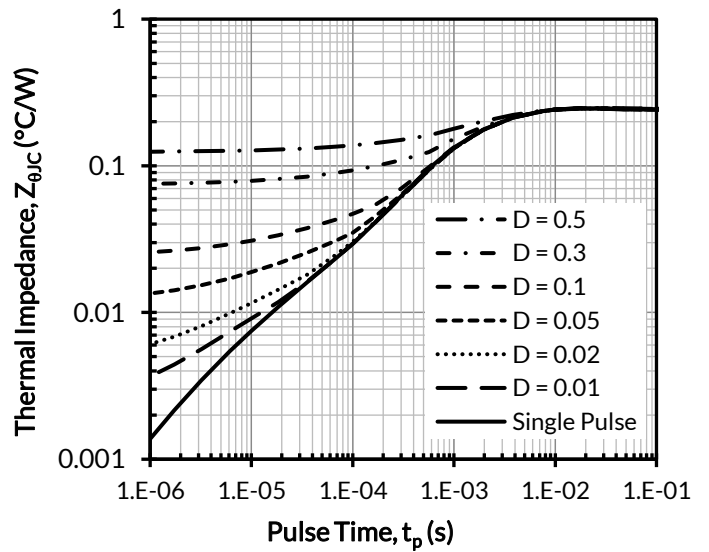


Figure 16. Maximum transient thermal impedance

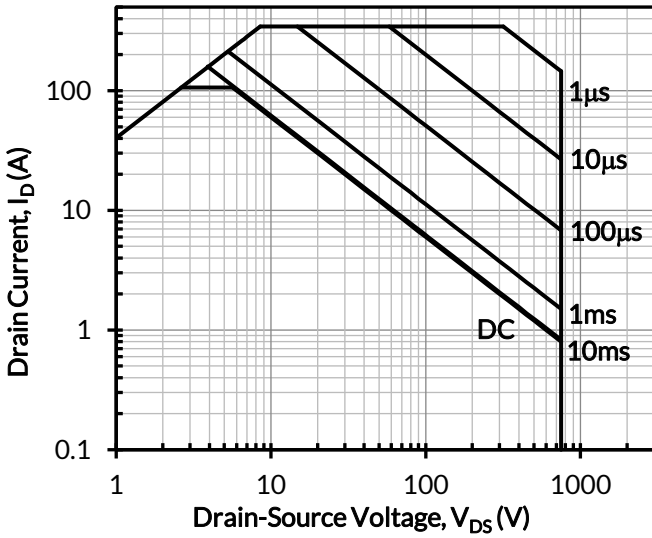


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

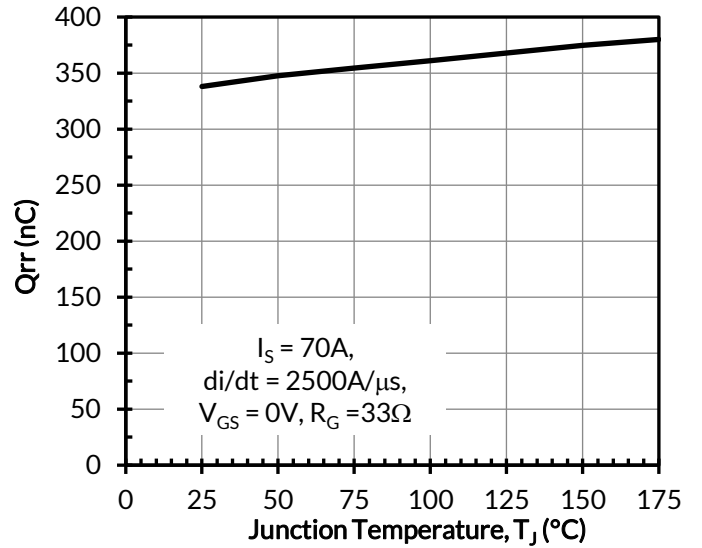


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature at $V_{DS} = 400\text{V}$

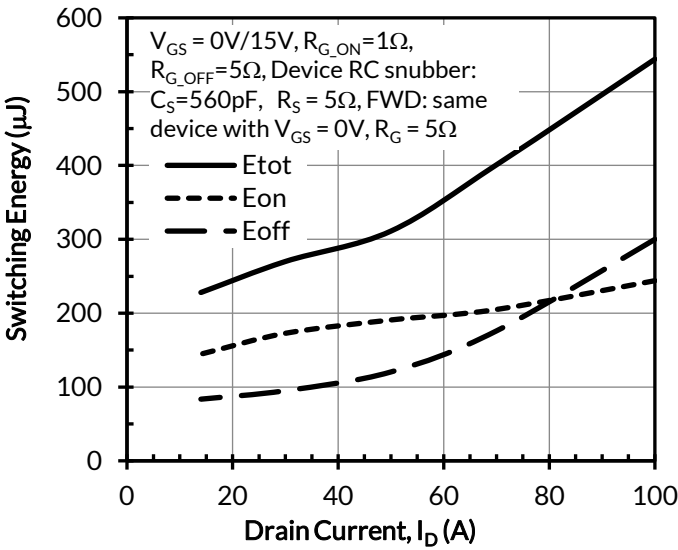


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

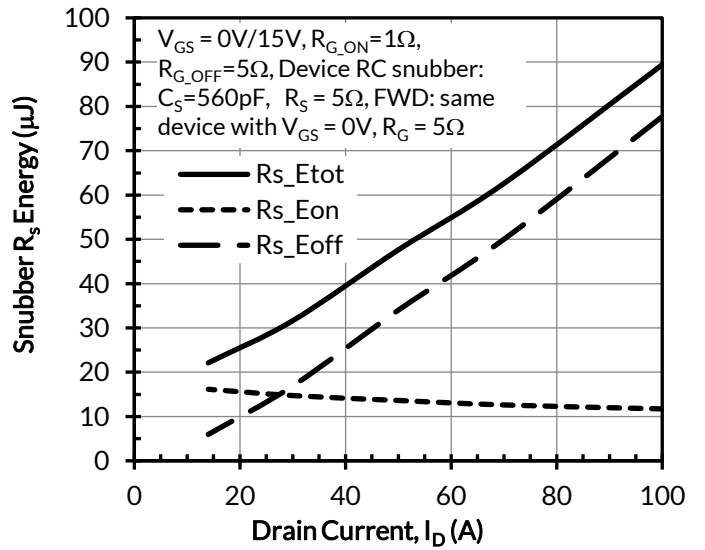


Figure 20. RC snubber energy loss vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

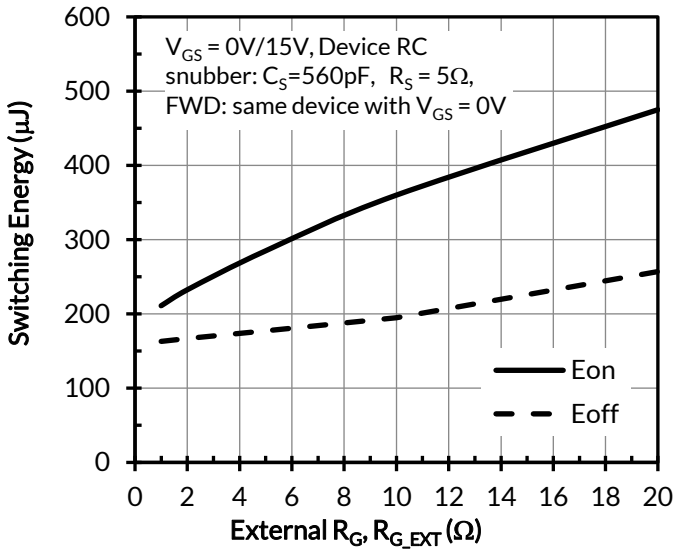


Figure 21. Clamped inductive switching energy vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

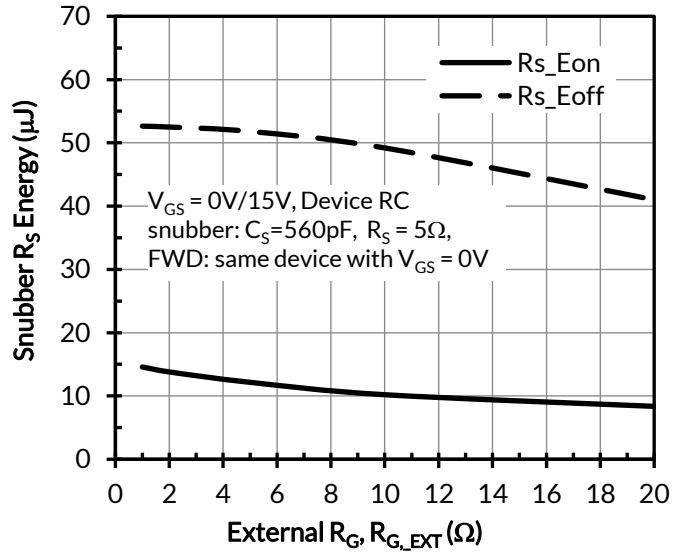


Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

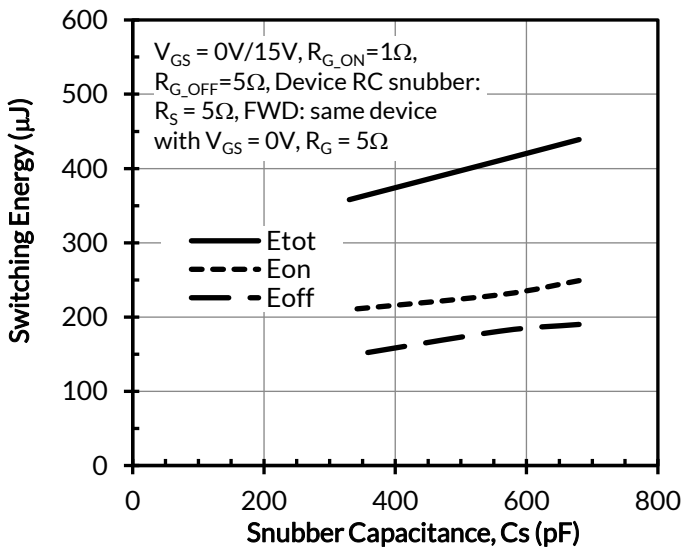


Figure 23. Clamped inductive switching energy vs. Snubber Capacitance C_S at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

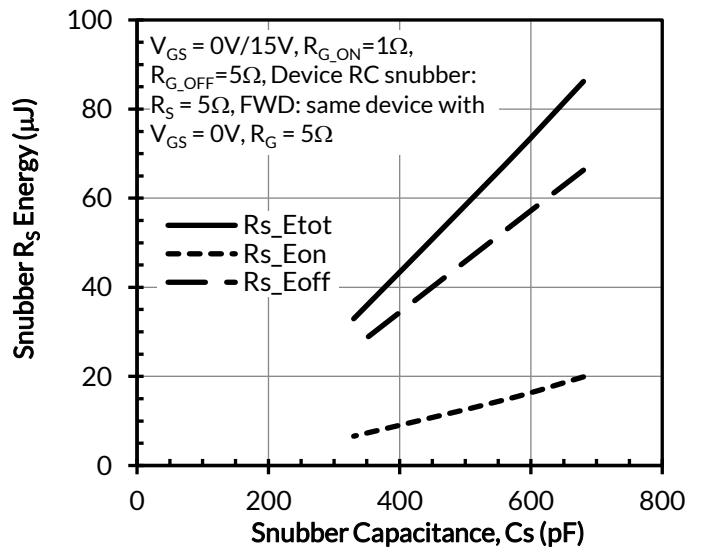


Figure 24. RC snubber energy loss vs. Snubber Capacitance C_S at $V_{DS} = 400V$, $I_D = 70A$, and $T_J = 25^\circ C$

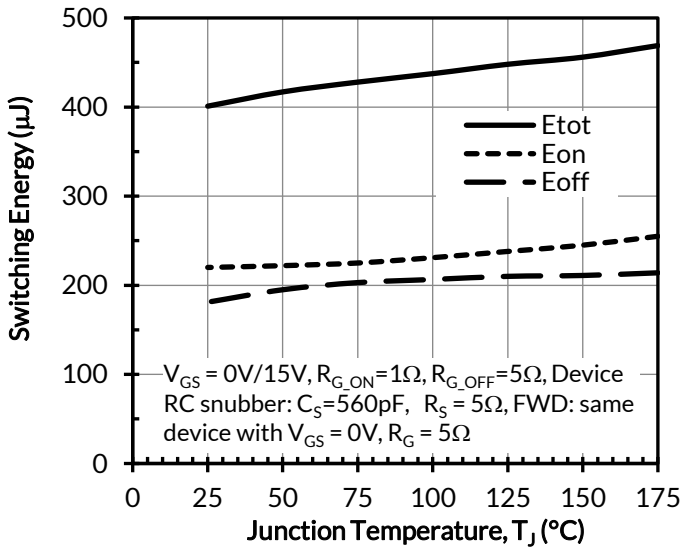


Figure 25. Clamped inductive switching energies vs. junction temperature T_j at $V_{DS} = 400V$, and $I_D = 70A$

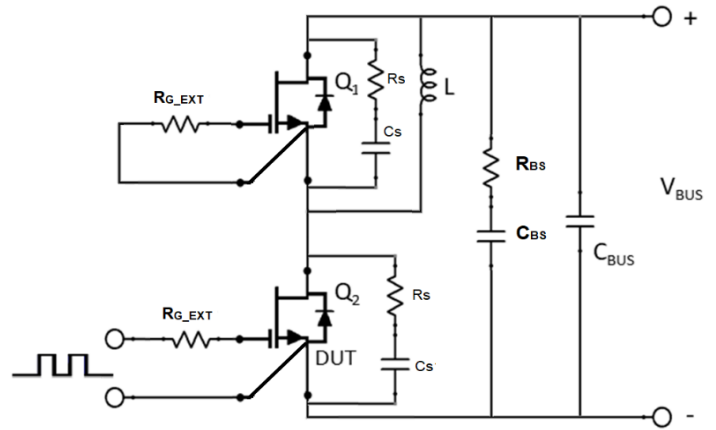


Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a device snubber ($R_s = 5\Omega$, $C_s = 560pF$) and bus RC snubber ($R_{BS} = 1\Omega$, $C_{BS} = 100nF$) is used to reduce the power loop high frequency oscillations.