



VIPer22A-E VIPer22ADIP-E, VIPer22AS-E

Low power OFF-line SMPS primary switcher

Features

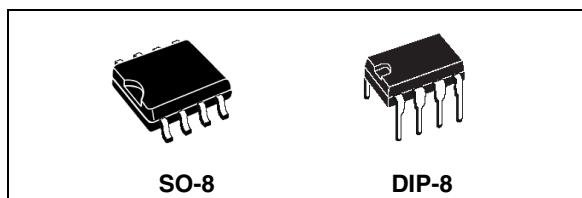
- Fixed 60 kHz switching frequency
- 9 V to 38 V wide range V_{DD} voltage
- Current mode control
- Auxiliary undervoltage lockout with hysteresis
- High voltage start-up current source
- Overtemperature, overcurrent and overvoltage protection with auto-restart

Table 1. Typical power capability

Mains type	SO-8	DIP-8
European (195 - 265 Vac)	12 W	20 W
US / wide range (85 - 265 Vac)	7 W	12 W

Description

The VIPer22A-E combines a dedicated current mode PWM controller with a high voltage power MOSFET on the same silicon chip.



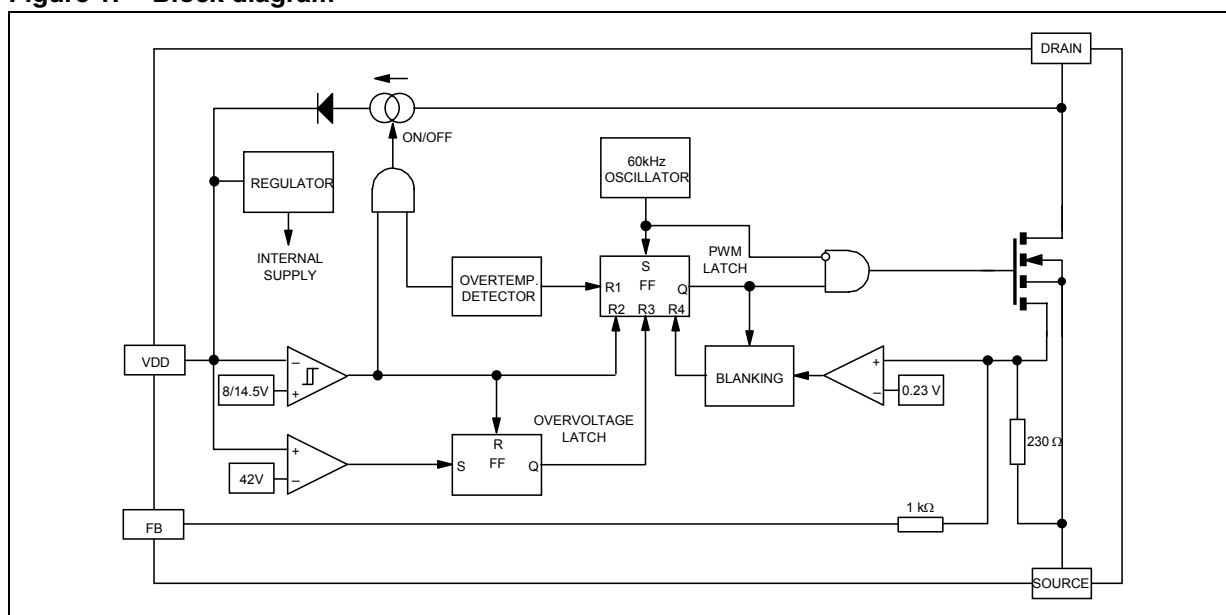
Typical applications cover off line power supplies for battery charger adapters, standby power supplies for TV or monitors, auxiliary supplies for motor control, etc. The internal control circuit offers the following benefits:

Large input voltage range on the V_{DD} pin accommodates changes in auxiliary supply voltage. This feature is well adapted to battery charger adapter configurations.

Automatic burst mode in low load condition.

Overvoltage protection in HICCUP mode.

Figure 1. Block diagram



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1 Electrical data

1.1 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
$V_{DS(sw)}$	Switching drain source voltage ($T_J = 25 \dots 125 \text{ }^\circ\text{C}$) ⁽¹⁾	-0.3 ... 730	V
$V_{DS(st)}$	Start-up drain source voltage ($T_J = 25 \dots 125 \text{ }^\circ\text{C}$) ⁽²⁾	-0.3 ... 400	V
I_D	Continuous drain current	Internally limited	A
V_{DD}	Supply voltage	0 ... 50	V
I_{FB}	Feedback current	3	mA
V_{ESD}	Electrostatic discharge: Machine model ($R = 0 \text{ } \Omega$; $C = 200 \text{ pF}$) Charged device model	200 1.5	V kV
T_J	Junction operating temperature	Internally limited	$^\circ\text{C}$
T_C	Case operating temperature	-40 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

1. This parameter applies when the start-up current source is OFF. This is the case when the VDD voltage has reached V_{DDon} and remains above V_{DDoff} .
2. This parameter applies when the start up current source is on. This is the case when the VDD voltage has not yet reached V_{DDon} or has fallen below V_{DDoff} .

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		SO-8	DIP-8	Unit
R_{thJC}	Thermal resistance junction - case	Max	25	15	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction - ambient ⁽¹⁾	Max	55	45	$^\circ\text{C}/\text{W}$

1. When mounted on a standard single-sided FR4 board with 200 mm² of Cu (at least 35 μm thick) connected to all DRAIN pins.

2 Electrical characteristics

$T_J = 25\text{ °C}$, $V_{DD} = 18\text{ V}$, unless otherwise specified

Table 4. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-source voltage	$I_D = 1\text{ mA}$; $V_{FB} = 2\text{ V}$	730			V
I_{DSS}	OFF state drain current	$V_{DS} = 500\text{ V}$; $V_{FB} = 2\text{ V}$; $T_J = 125\text{ °C}$			0.1	mA
$r_{DS(on)}$	Static drain-source ON state resistance	$I_D = 0.4\text{ A}$ $I_D = 0.4\text{ A}$; $T_J = 100\text{ °C}$		15	17 31	Ω
t_f	Fall time	$I_D = 0.2\text{ A}$; $V_{IN} = 300\text{ V}$ ⁽¹⁾ (See Figure 9 on page 13)		100		ns
t_r	Rise time	$I_D = 0.4\text{ A}$; $V_{IN} = 300\text{ V}$ ⁽¹⁾ (See Figure 9 on page 13)		50		ns
C_{OSS}	Drain capacitance	$V_{DS} = 25\text{ V}$		40		pF

1. On clamped inductive load

Table 5. Supply section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{DDch}	Start-up charging current	$100\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{DD} = 0\text{ V} \dots V_{DDon}$ (See Figure 10 on page 13)		-1		mA
I_{DDoff}	Start-up charging current in thermal shutdown	$V_{DD} = 5\text{ V}$; $V_{DS} = 100\text{ V}$ $T_J > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating supply current not switching	$I_{FB} = 2\text{ mA}$		3	5	mA
I_{DD1}	Operating supply current switching	$I_{FB} = 0.5\text{ mA}$; $I_D = 50\text{ mA}$ ⁽¹⁾		4.5		mA
D_{RST}	Restart duty-cycle	(See Figure 11 on page 13)		16		%
V_{DDoff}	V_{DD} undervoltage shutdown threshold	(See Figure 10 , Figure 11 on page 13)	7	8	9	V
V_{DDon}	V_{DD} start-up threshold	(See Figure 10 , Figure 11 on page 13)	13	14.5	16	V
V_{DDhyst}	V_{DD} threshold hysteresis	(See Figure 10 on page 13)	5.8	6.5	7.2	V
V_{DDovp}	V_{DD} overvoltage threshold		38	42	46	V

1. These test conditions obtained with a resistive load are leading to the maximum conduction time of the device.

Table 6. Oscillation section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{OSC}	Oscillator frequency total variation	$V_{DD} = V_{DDoff} \dots 35 \text{ V};$ $T_J = 0 \dots 100 \text{ }^\circ\text{C}$	54	60	66	kHz

Table 7. PWM comparator section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
G_{ID}	I_{FB} to I_D current gain	(See Figure 12 on page 14)		560		
I_{Dim}	Peak current limitation	$V_{FB} = 0 \text{ V}$ (See Figure 12 on page 14)	0.56	0.7	0.84	A
I_{FBsd}	I_{FB} shutdown current	(See Figure 12 on page 14)		0.9		mA
R_{FB}	FB pin input impedance	$I_D = 0 \text{ mA}$ (See Figure 12 on page 14)		1.2		k Ω
t_d	Current sense delay to turn-OFF	$I_D = 0.4 \text{ A}$		200		ns
t_b	Blanking time			500		ns
t_{ONmin}	Minimum turn-ON time			700		ns

Table 8. Overtemperature section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{SD}	Thermal shutdown temperature	(See Figure 13 on page 14)	140	170		$^\circ\text{C}$
T_{HYST}	Thermal shutdown hysteresis	(See Figure 13 on page 14)		40		$^\circ\text{C}$

Table 9. Typical power capability ⁽¹⁾

Mains type	SO-8	DIP-8
European (195 - 265 Vac)	12 W	20 W
US / Wide range (85 - 265 Vac)	7 W	12 W

1. Above power capabilities are given under adequate thermal conditions

3 Pin connections and function

Figure 2. Pin connection

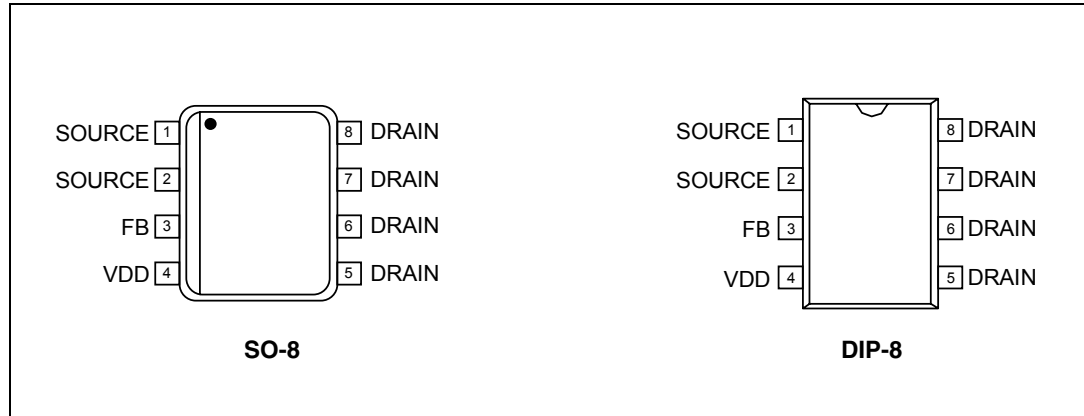


Figure 3. Current and voltage conventions

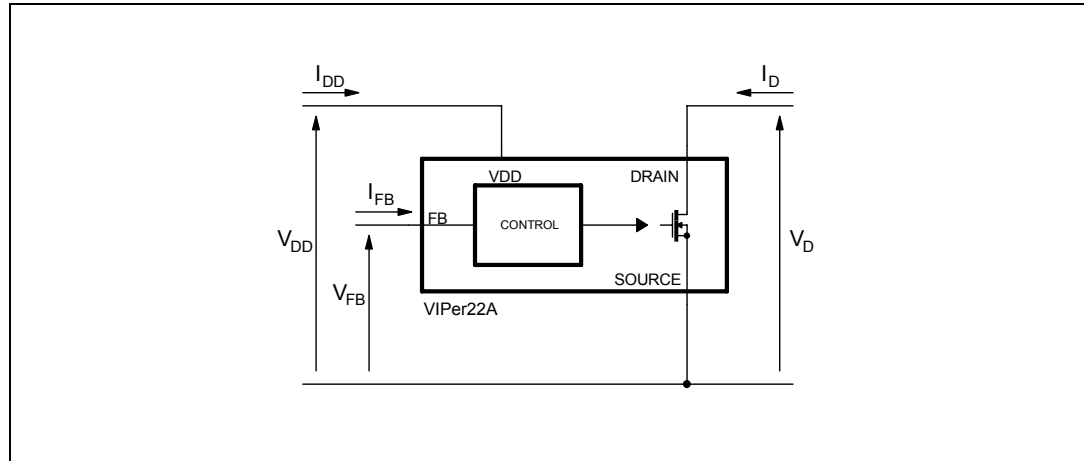


Table 10. Pin function

Pin Name	Pin function
V _{DD}	Power supply of the control circuits. Also provides a charging current during start up thanks to a high voltage current source connected to the drain. For this purpose, an hysteresis comparator monitors the V _{DD} voltage and provides two thresholds: - V _{DDon} : Voltage value (typically 14.5 V) at which the device starts switching and turns off the start up current source. - V _{DDoff} : Voltage value (typically 8 V) at which the device stops switching and turns on the start up current source.
SOURCE	Power MOSFET source and circuit ground reference.
DRAIN	Power MOSFET drain. Also used by the internal high voltage current source during start up phase for charging the external V _{DD} capacitor.
FB	Feedback input. The useful voltage range extends from 0 V to 1 V, and defines the peak drain MOSFET current. The current limitation, which corresponds to the maximum drain current, is obtained for a FB pin shorted to the SOURCE pin.

4.2 Wide range of V_{DD} voltage

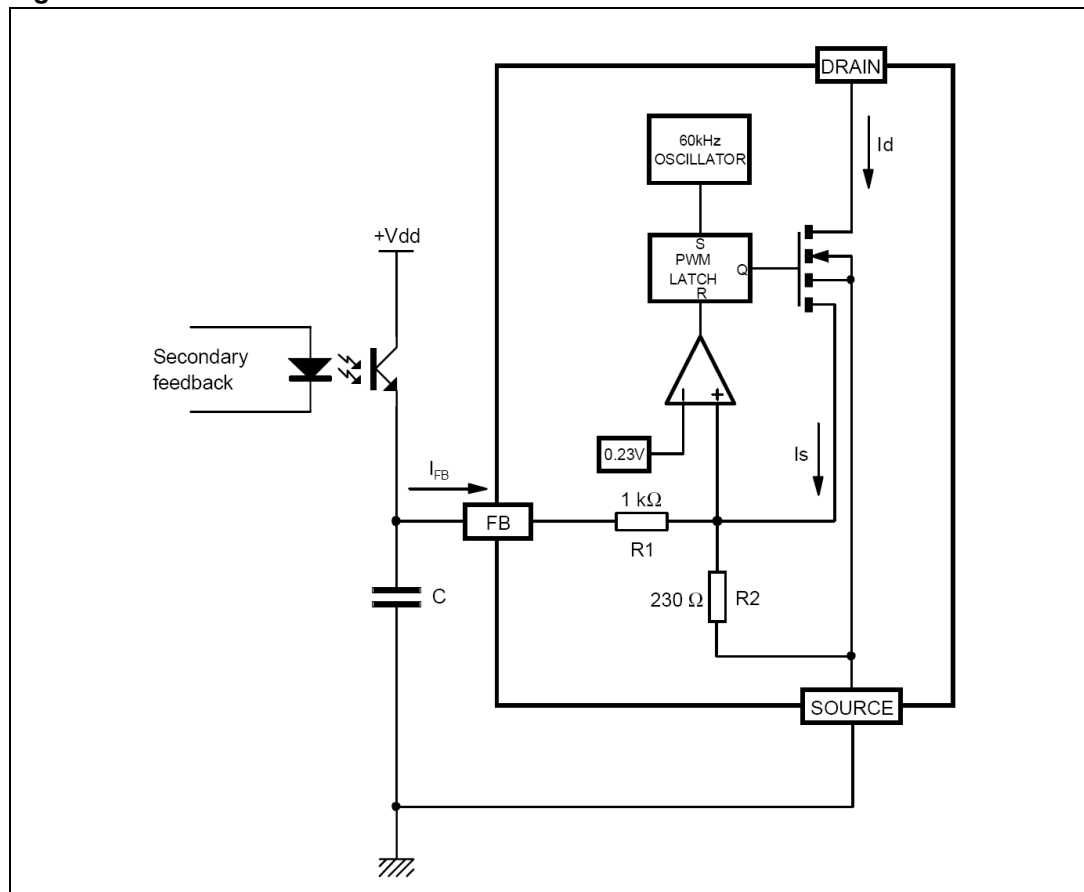
The V_{DD} pin voltage range extends from 9 V to 38 V. This feature offers a great flexibility in design to achieve various behaviors. In [Figure 4 on page 7](#) a forward configuration has been chosen to supply the device with two benefits:

- As soon as the device starts switching, it immediately receives some energy from the auxiliary winding. C5 can be therefore reduced and a small ceramic chip (100 nF) is sufficient to insure the filtering function. The total start up time from the switch on of input voltage to output voltage presence is dramatically decreased.
- The output current characteristic can be maintained even with very low or zero output voltage. Since the TSM101 is also supplied in forward mode, it keeps the current regulation up whatever the output voltage is. The V_{DD} pin voltage may vary as much as the input voltage, that is to say with a ratio of about 4 for a wide range application.

4.3 Feedback pin principle of operation

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input (the inverted input of an operational amplifier), the FB pin is sensitive to current. [Figure 5](#). presents the internal current mode structure.

Figure 5. Internal current control structure



The Power MOSFET delivers a sense current I_S which is proportional to the main current I_D . R2 receives this current and the current coming from the FB pin. The voltage across R2 is then compared to a fixed reference voltage of about 0.23 V. The MOSFET is switched off when the following equation is reached:

$$R_2 \cdot (I_S + I_{FB}) = 0.23V$$

By extracting I_S :

$$I_S = \frac{0.23V}{R_2} - I_{FB}$$

Using the current sense ratio of the MOSFET G_{ID} :

$$I_D = G_{ID} \cdot I_S = G_{ID} \cdot \left(\frac{0.23V}{R_2} - I_{FB} \right)$$

The current limitation is obtained with the FB pin shorted to ground ($V_{FB} = 0 V$). This leads to a negative current sourced by this pin, and expressed by:

$$I_{FB} = -\frac{0.23V}{R_1}$$

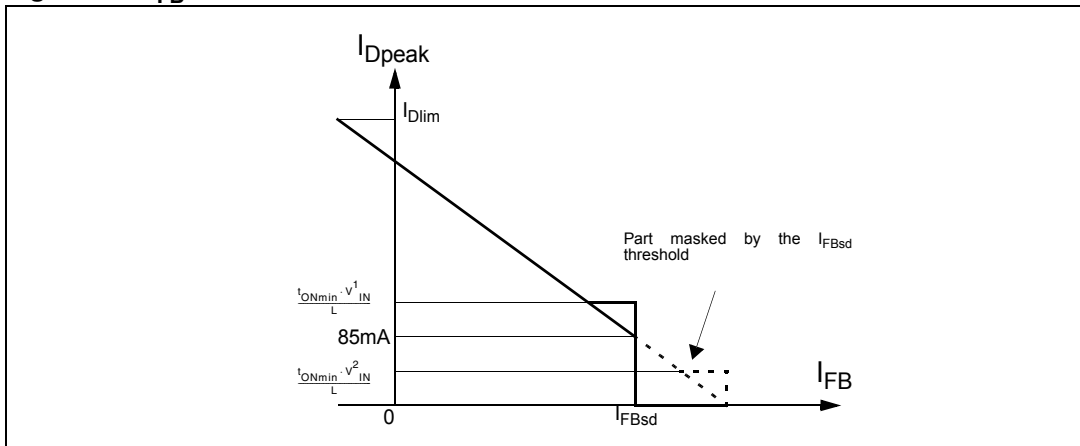
By reporting this expression in the previous one, it is possible to obtain the drain current limitation I_{Dlim} :

$$I_{Dlim} = G_{ID} \cdot 0.23V \cdot \left(\frac{1}{R_2} + \frac{1}{R_1} \right)$$

In a real application, the FB pin is driven with an optocoupler as shown on [Figure 5](#), which acts as a pull up. So, it is not possible to really short this pin to ground and the above drain current value is not achievable. Nevertheless, the capacitor C is averaging the voltage on the FB pin, and when the optocoupler is off (start up or short circuit), it can be assumed that the corresponding voltage is very close to 0 V.

For low drain currents, the formula (1) is valid as long as I_{FB} satisfies $I_{FB} < I_{FBsd}$, where I_{FBsd} is an internal threshold of the VIPer22A. If I_{FB} exceeds this threshold the device will stop switching. This is represented on [Figure 12 on page 14](#), and I_{FBsd} value is specified in the PWM COMPARATOR SECTION. Actually, as soon as the drain current is about 12 % of I_{Dlim} , that is to say 85 mA, the device will enter a burst mode operation by missing switching cycles. This is especially important when the converter is lightly loaded.

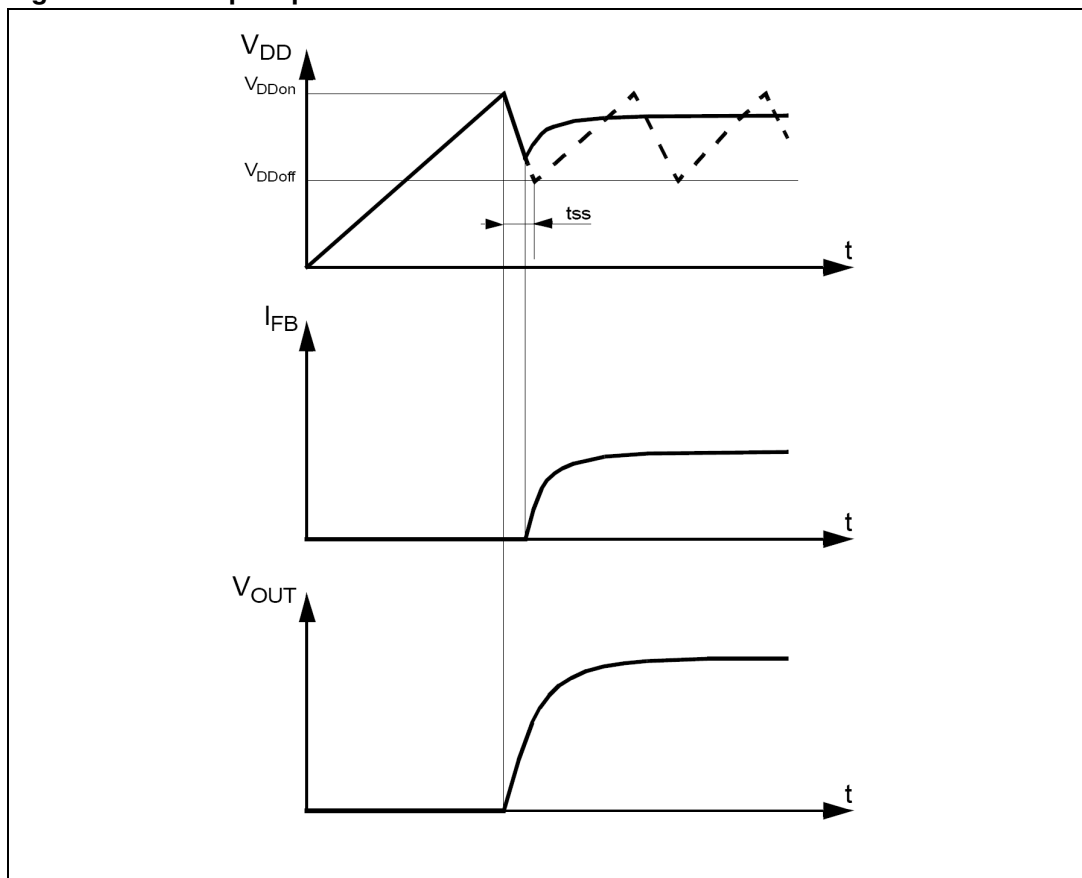
Figure 6. I_{FB} transfer function



It is then possible to build the total DC transfer function between I_D and I_{FB} as shown on [Figure 6 on page 10](#). This figure also takes into account the internal blanking time and its associated minimum turn on time. This imposes a minimum drain current under which the device is no more able to control it in a linear way. This drain current depends on the primary inductance value of the transformer and the input voltage. Two cases may occur, depending on the value of this current versus the fixed 85 mA value, as described above.

4.4 Startup sequence

Figure 7. Startup sequence



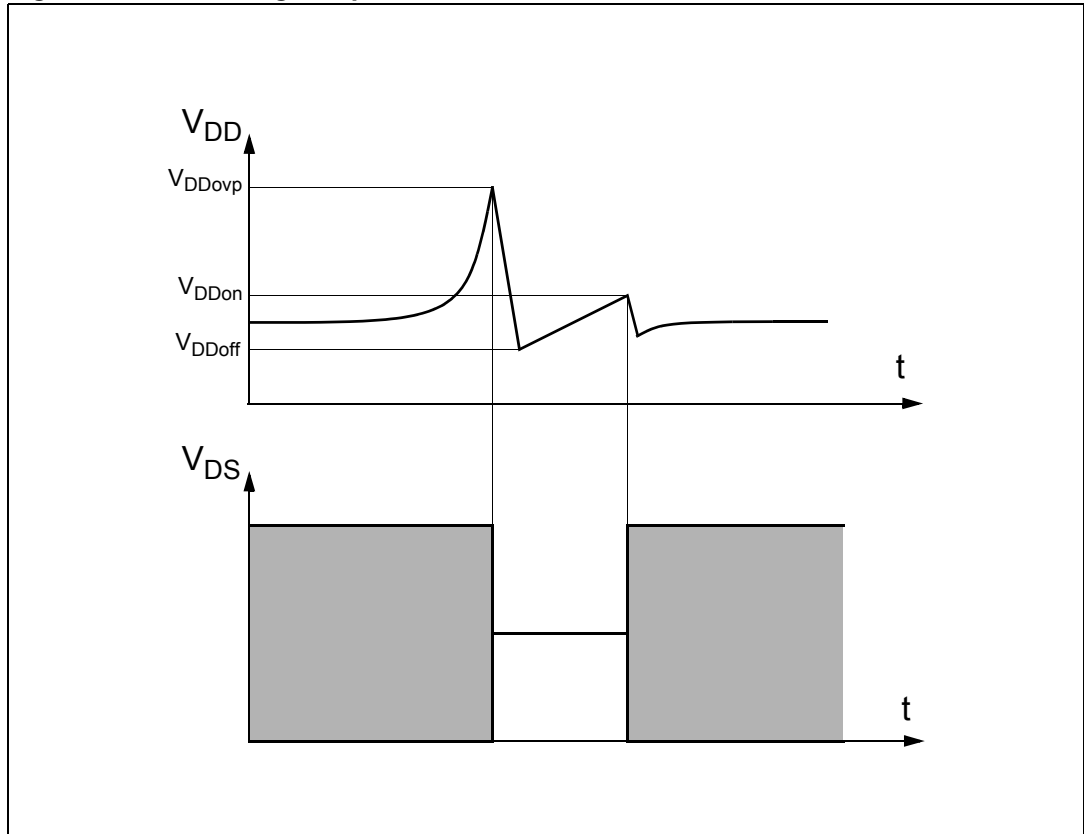
This device includes a high voltage start up current source connected on the drain of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated as long as V_{DD} is lower than $V_{DD(on)}$. When reaching $V_{DD(on)}$, the start up current source is switched OFF and the device begins to operate by turning on and off its main power MOSFET. As the FB pin does not receive any current from the optocoupler, the device operates at full current capacity and the output voltage rises until reaching the regulation point where the secondary loop begins to send a current in the optocoupler. At this point, the converter enters a regulated operation where the FB pin receives the amount of current needed to deliver the right power on secondary side.

This sequence is shown in [Figure 7](#). Note that during the real starting phase t_{ss} , the device consumes some energy from the V_{DD} capacitor, waiting for the auxiliary winding to provide a continuous supply. If the value of this capacitor is too low, the start up phase is terminated before receiving any energy from the auxiliary winding and the converter never starts up. This is illustrated also in the same figure in dashed lines.

4.5 Overvoltage threshold

An overvoltage detector on the V_{DD} pin allows the VIPer22A to reset itself when V_{DD} exceeds V_{DDovp} . This is illustrated in [Figure 8](#), which shows the whole sequence of an overvoltage event. Note that this event is only latched for the time needed by V_{DD} to reach V_{DDoff} , and then the device resumes normal operation automatically.

Figure 8. Overvoltage sequence



5 Operation pictures

Figure 9. Rise and fall time

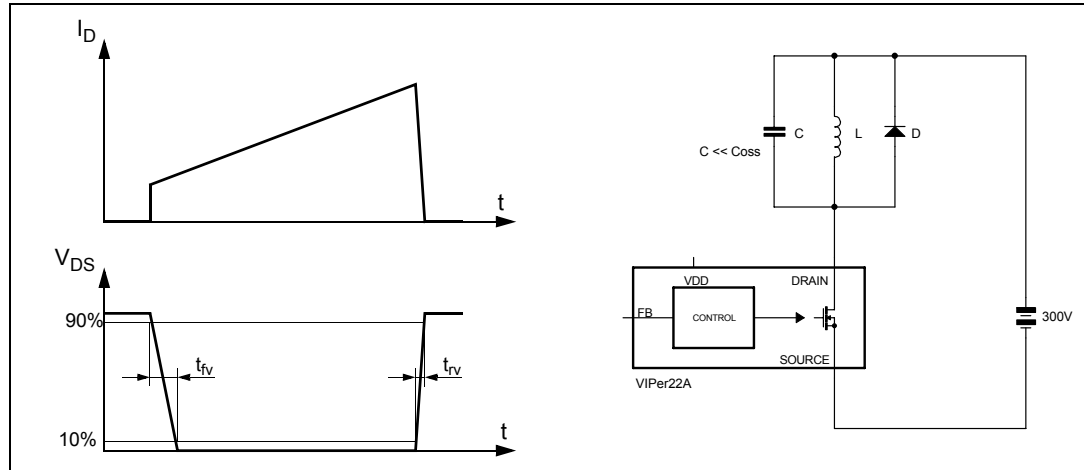


Figure 10. Start-up V_{DD} current

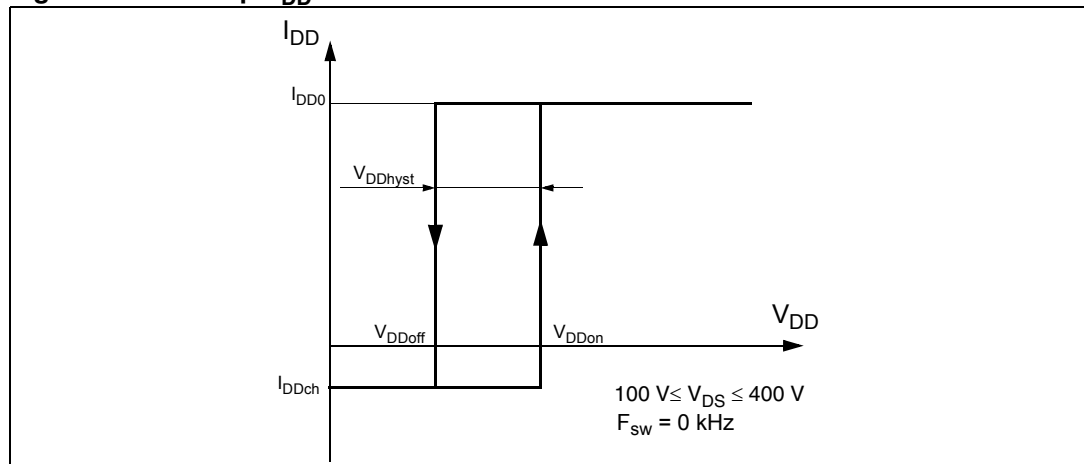


Figure 11. Restart duty-cycle

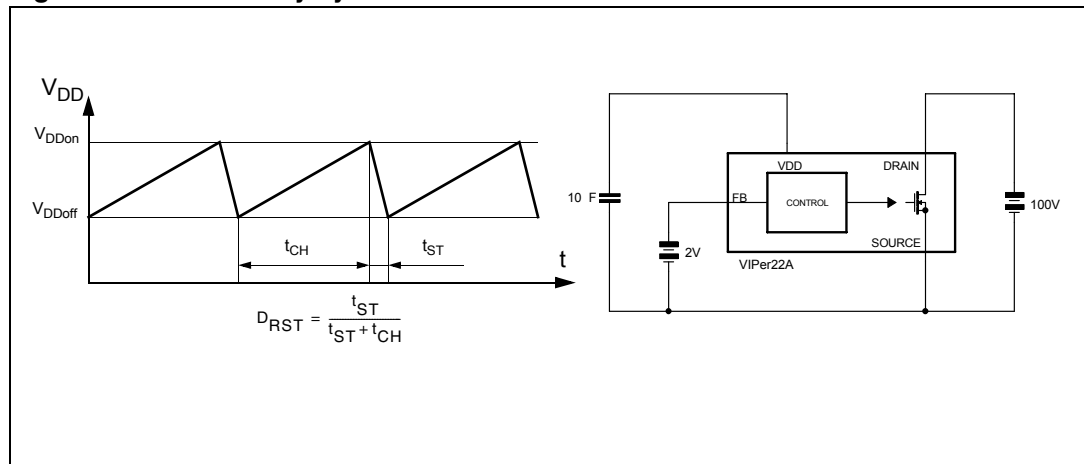


Figure 12. Peak drain current vs feedback current

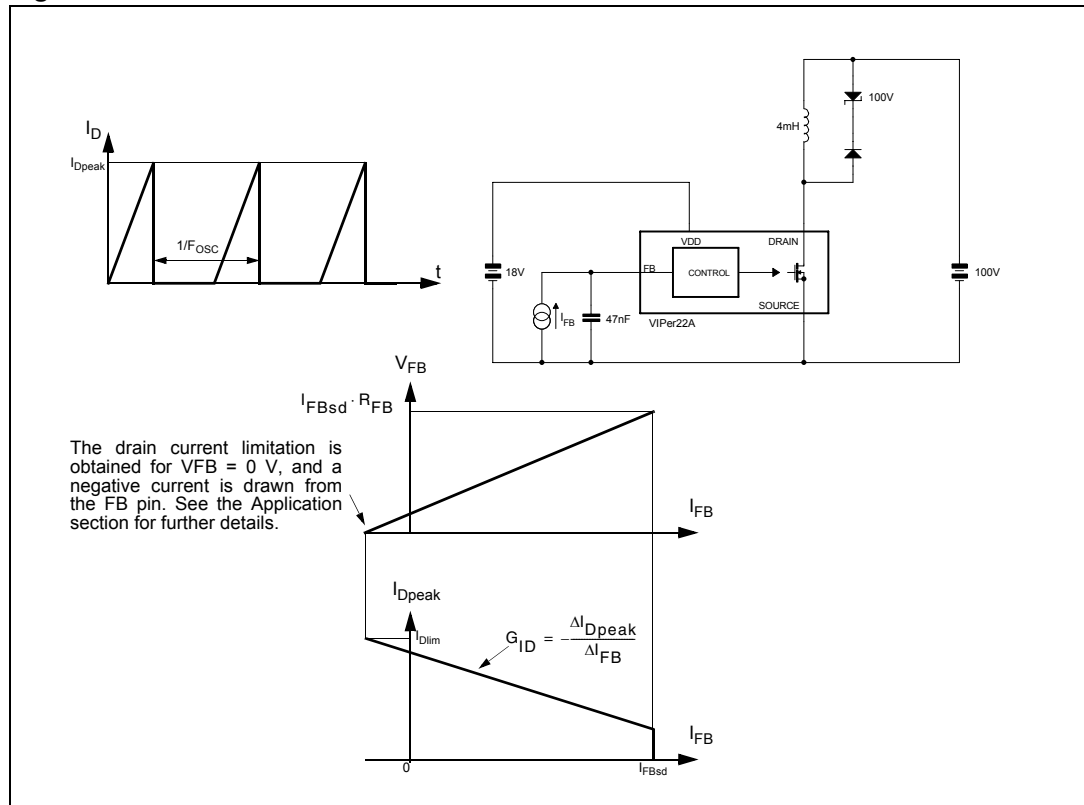


Figure 13. Thermal shutdown

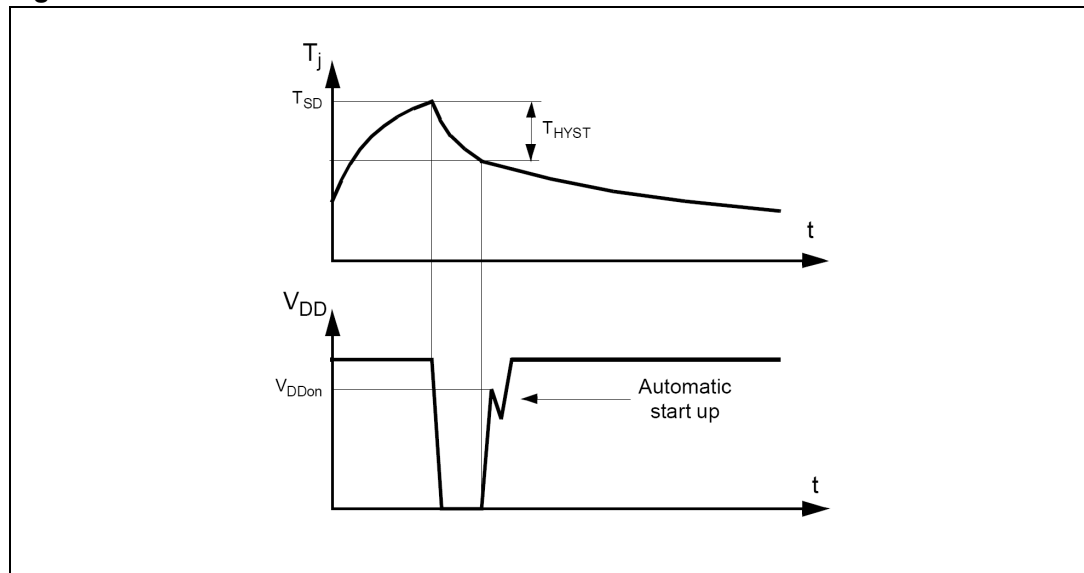


Figure 14. Switching frequency vs temperature

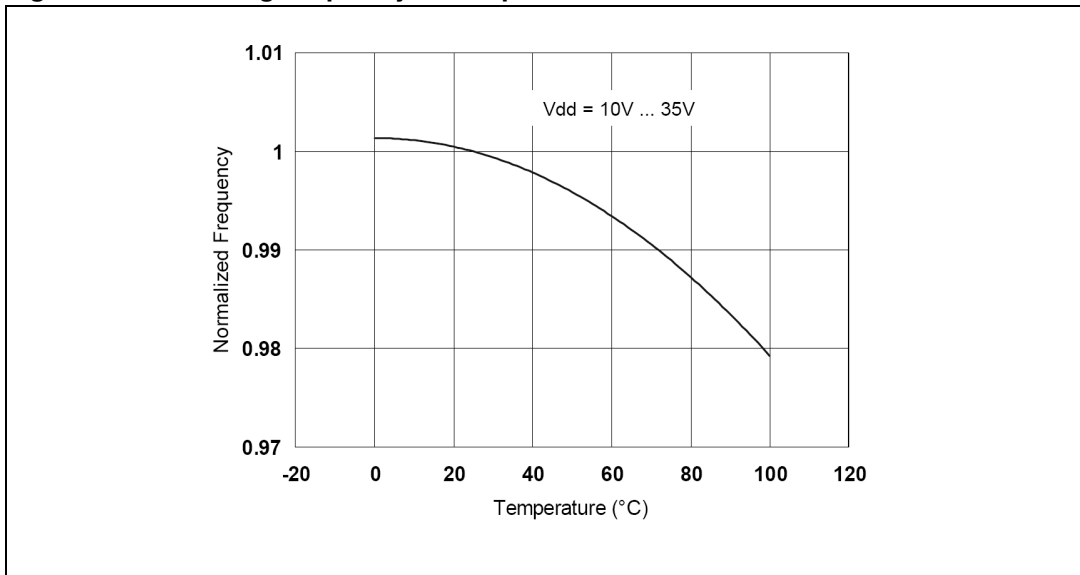
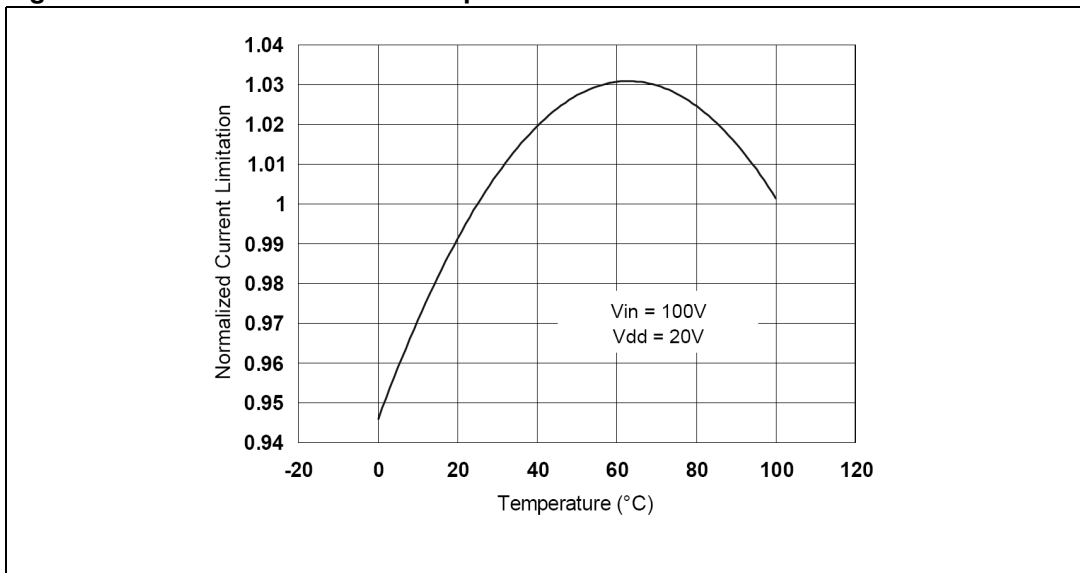


Figure 15. Current limitation vs temperature



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 11. DIP-8 mechanical data

Dim.	Databook (mm.)		
	Min.	Nom.	Max.
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

Figure 16. Package dimensions

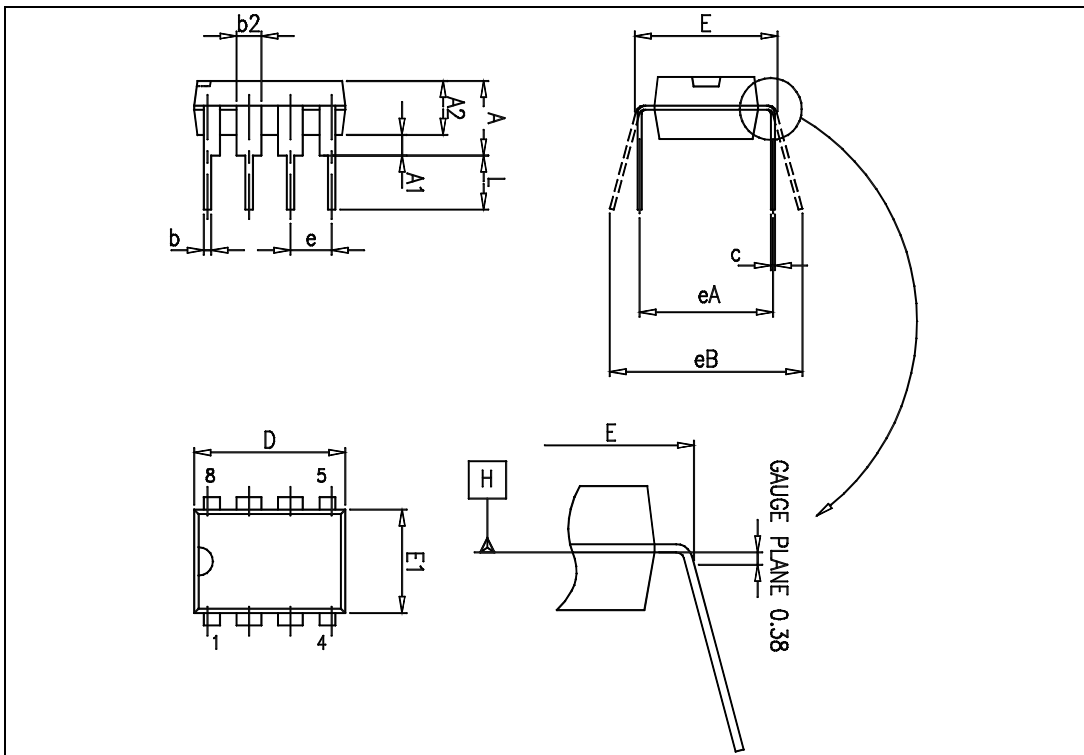
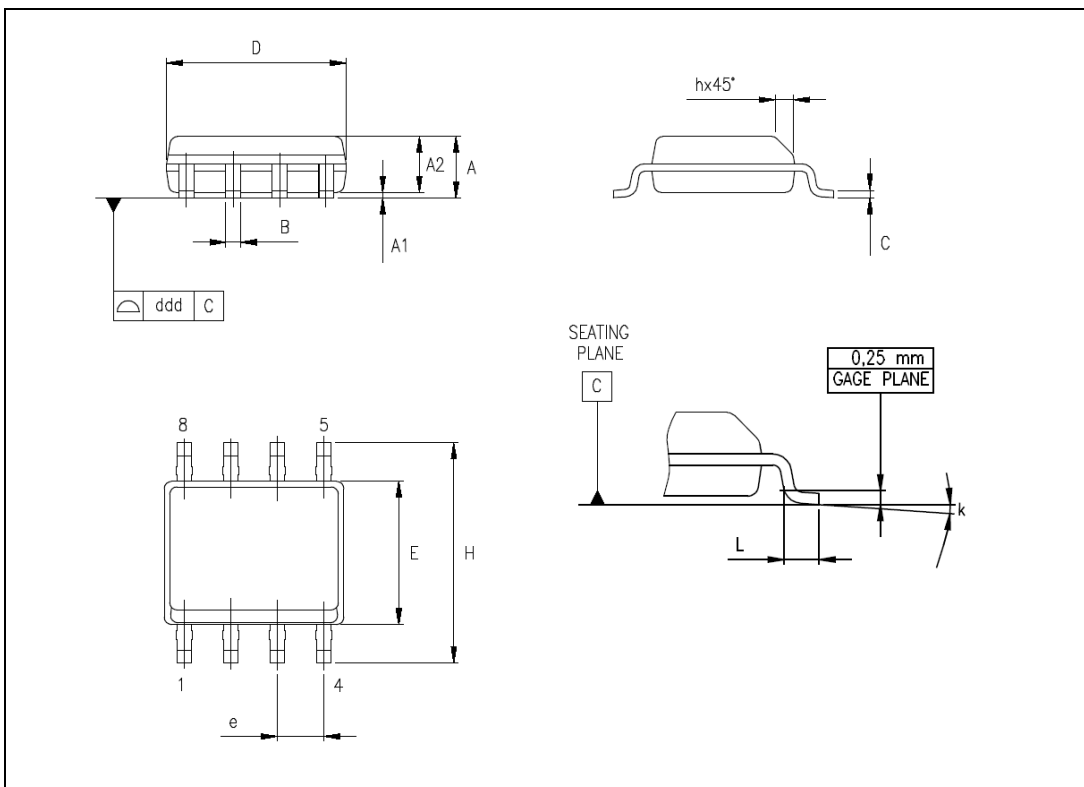


Table 12. SO-8 mechanical data

Dim.	Databook (mm.)		
	Min.	Nom.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	8° (max.)		
ddd			0.1

Figure 17. Package dimensions



7 Order codes

Table 13. Order codes

Order codes	Package	Packaging
VIPER22ASTR-E	SO-8	Tape and reel
VIPer22AS-E	SO-8	Tube
VIPer22ADIP-E	DIP-8	Tube

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
09-Feb-2006	1	Initial release.
25-Nov-2010	2	Updated Table 11 .