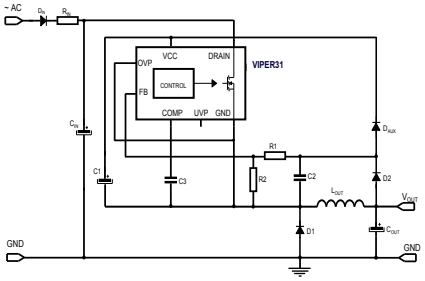
VIPER31

Datasheet

Energy saving offline high voltage converter



Product status link

VIPER31

Product label

SUSTAINABLE TECHNOLOGY

Features

- 800 V avalanche-rugged power MOSFET to cover ultra-wide VAC input range
- Embedded HV startup and sense FET
- Current mode PWM controller
- Drain current limit protection (OCP):
  - 710 mA (VIPER317)
  - 850 mA (VIPER318)
  - 990 mA (VIPER319)
- Wide supply voltage range: 4.5 V to 30 V
  - < 20 mW @ 230 V_{AC} in no-load;
  - < 430 mW @ 230 V_{AC}, 25 0mW output load
- Jittered switching frequency reduces the EMI filter cost:
  - 30 kHz ± 7% (type X)
  - 60 kHz ± 7% (type L)
  - 132 kHz ±7% (type H)
- Embedded E/A with 1.2 V reference
- Built-in soft-start for improved system reliability
- Protections with automatic restart:
  - overload/short-circuit (OLP)
  - thermal shutdown
  - overvoltage
- Protections without automatic restart:
  - pulse-skip protection to avoid flux runaway
  - undervoltage/disable
  - max. duty cycle

Application

- Low power SMPS for home appliances, home automation, industrial, consumers, lighting
- Low power adapters

Description

The VIPER31 device is a high-voltage converter that smartly integrates an 800 V avalanche rugged power MOSFET with PWM current-mode control. The 800 V breakdown allows extended input voltage range to be applied, as well as to reduce the size of the DRAIN snubber circuit. The IC can meet the most stringent energy-saving standards as it has very low consumption and operates in pulse frequency modulation at light load. Overvoltage and undervoltage protections with separate and settable intervention thresholds are available at OVP and UVP pins respectively. UVP can also be used as a disabling input for the entire SMPS, with ultra-low residual input power consumption. Integrated HV startup, sense FET, error amplifier and oscillator with frequency jitter allow a complete application to be designed with a minimum component count. Flyback, buck and buck boost topologies are supported.

1 Pin setting

Figure 1. **Connection diagram**

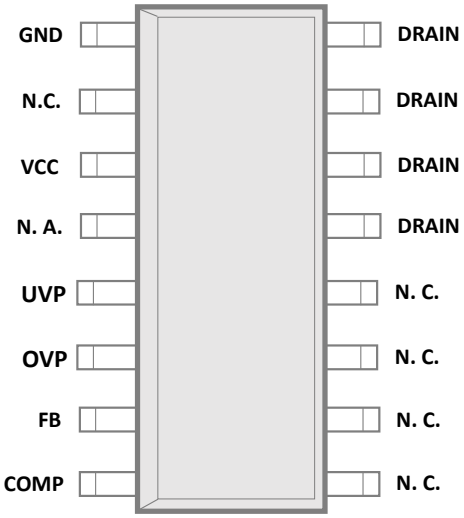


Table 1. **Pin description**

Pin number	Name	Function
1	GND	**Ground and MOSFET source.** Connection of both the source of the internal MOSFET and the return of the bias current of the device. All of the groundings of bias components must be tied to a trace going to this pin and kept separate from the pulsed current return.
2	N. C.	**Not connected.** When designing the PCB, this pin can be soldered to GND.
3	VCC	**Controller Supply**. An external storage capacitor has to be connected across this pin and GND. The pin, internally connected to the high-voltage current source, provides the VCC capacitor charging current at startup. A small bypass capacitor (0.1 µF typ.) in parallel, placed as close as possible to the IC, is also recommended, for noise filtering purposes.
4	N.A.	**Not available for user.** This pin is mechanically connected to the controller die pad of the frame. In order to improve noise immunity, it is highly recommended to connect it to GND.
5	UVP	**Undervoltage Protection.** If V_{UVP} falls below the internal threshold V_{UVP_th} (0.4 V typ.) for more than t_{UVP_DEB} time (30 ms, typ.), the IC is disabled, and its consumption reduced to ultra-low values. When V_{UVP} rises above V_{UVP_th}, the device waits for a t_{UVP_REST} time interval (30 ms, typ.) then resumes switching. The pin can be used to realize an input undervoltage protection or as a disabling input for the entire SMPS, with ultra-low residual input power consumption. If the feature is not required, the pin must be left open, which excludes the function.
6	OVP	**Overvoltage protection**. If VOVP exceeds the internal threshold V_{OVP_th} (4 V typ.) for more than t_{OVP_DEB} time (250 µsec, typ.), the PWM is disabled in auto-restart for t_{OVP_REST} (500 msec, typ.) until the OVP condition is removed, after that it restarts switching with soft-start phase. OVP pin can be used to realize an input overvoltage protection (or, in non-isolated topologies, an output overvoltage protection). If the feature is not required, the pin must be connected to GND, which excludes the function.
7	FB	**Direct feedback**. It is the inverting input of the internal transconductance E/A, internally referenced to 1.2 V with respect to GND. In non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled if FB is connected to GND pin.

Pin number	Name	Function
8	COMP	**Compensation**. This is the output of the internal E/A. A compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the control loop. In case of secondary feedback, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
9 to 12	N.C.	**Not connected.** These pins must be left floating in order to get a safe clearance distance.
13 to 16	DRAIN	**MOSFET drain**. The internal high-voltage current source sources current from these pins to charge the VCC capacitor at startup. The pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB, some copper areas under these pins decreases the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

2 Electrical and thermal ratings

Table 2. Absolute maximum ratings

Symbol	Parameter [1][2]	Min.	Max.	Unit
V_{DS}	Drain-to- source (ground) voltage		800	V
I_{DRAIN}	Pulsed drain current (pulse-width limited by SOA)		3	A
V_{CC}	VCC voltage	-0.3	30.5V	V
V_{OVP}	OVP voltage	-0.3	Internally limited[3]	V
V_{UVP}	UVP voltage	-0.3	Internally limited [3]	V
V_{FB}	FB voltage	-0.3	5 [4]	V
V_{COMP}	COMP voltage	-0.3	Internally limited [3]	V
P_{TOT}	Power Dissipation @ Tamb < 50°C		1[5]	W
T_J	Junction Temperature operating range	-40	150	°C
T_{STG}	Storage Temperature	-55	150	°C

1. *stresses beyond those listed absolute maximum ratings may cause permanent damage to the device.*
2. *exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability*
3. *by internal clamp between 4.75 V and 5.25 V or Vcc + 0.6 V, whichever is lower*
4. *the AMR value is intended when VCC ≥ 5 V, otherwise the value VCC + 0.3 V has to be considered.*
5. *when mounted on a standard single side FR4 board with 100 mm² (0.155² inch) of Cu (35 µm thick)*

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
		SO16N	
R_{TH-JC}	Thermal resistance junction to case[1] (dissipated power = 1W)	10	°C/W
R_{TH-JA}	Thermal resistance junction to ambient[1] (dissipated power = 1W)	120	°C/W
R_{TH-JC}	Thermal resistance junction to case[2] (dissipated power = 1W)	5	°C/W
R_{TH-JA}	Thermal resistance junction to ambient[2] (dissipated power = 1W)	85	°C/W

1. *when mounted on a standard single side FR4 board with minimum copper area*
2. *when mounted on a standard single side FR4 board with 100mm² (0.155² inch) of Cu (35 µm thick)*

Figure 2. R_{th_JA} versus copper area

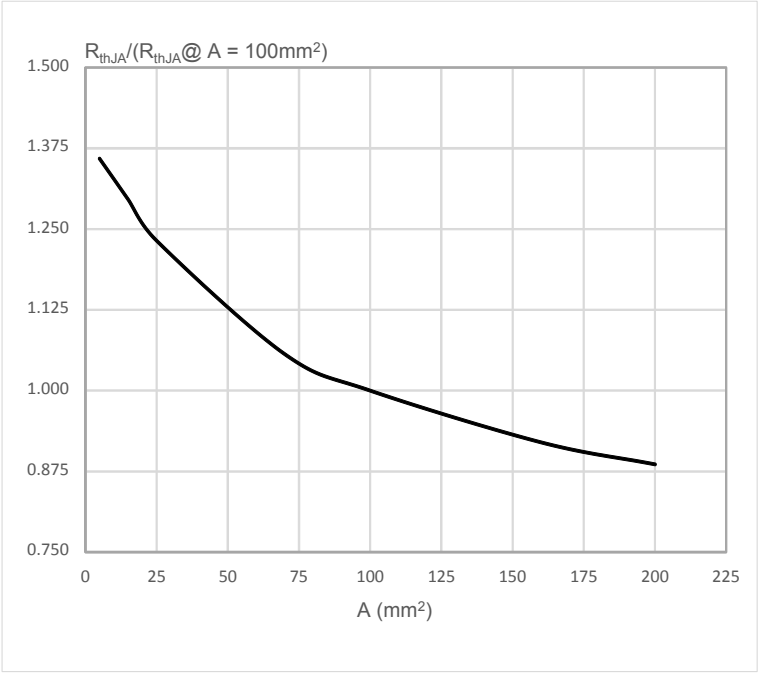


Table 4. Avalanche characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{AR}	Avalanche current	Repetitive and non-repetitive. Pulse-width limited by T_{Jmax}			1.15	A
EAS	Single pulse avalanche energy(1)	$I_{AS} = I_{AR}$, V_{DS} = 100 V, Starting T_J = 25°C			3	mJ

1. *Parameter derived by characterization*

2.1 Electrical characteristics

Tj = -40 to 125°C, V_{CC} = 9 V (unless otherwise specified)

Table 5. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, $V_{COMP} = V_{GND}$, T_J = 25°C	800			V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V, $V_{COMP} = V_{GND}$, T_J = 25°C			1	µA
I_{OFF}	OFF state drain current	V_{DRAIN} = max. rating, $V_{COMP} = V_{GND}$, T_J = 25°C			60	µA
$R_{DS(on)}$	Static drain-source ON-resistance	I_{DRAIN} = 400 mA, T_J = 25°C			3.5	Ω
		I_{DRAIN} = 400 mA, T_J = 125°C			7	Ω

Table 6. Supply section

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
High-voltage startup current source							
V_{BVDSS_SU}	Breakdown voltage of startup MOSFET	T_J = 25°C		800			V
V_{HV_START}	Drain-source startup voltage					24	V
R_G	Startup resistor	$V_{FB} > V_{FB\_REF}$, V_{DRAIN} = 400 V, V_{DRAIN} = 600 V		36	45	54	MΩ
I_{CH1}	V_{CC} charging current at startup	V_{DRAIN} = 100V, $V_{CC} \leq$ 1V		0.5	1	1.5	mA
I_{CH2}	V_{CC} charging current	$V_{FB} > V_{FB\_REF}$, V_{DRAIN} = 100V, 1V < V_{CC} <V_{CCon}		7.6	8.8	10	
IC supply and consumptions							
V_{CC}	Operating voltage range			4.5		30	V
V_{Ccon}	VCC startup threshold			7.5	8	8.5	V
V_{Cson}	HV current source turn-on threshold	V_{CC} falling		4	4.25	4.5	V
V_{Ccoff}	UVLO			3.75	4	4.25	V
I_q	Quiescent current	Not switching, $V_{FB} > V_{FB\_REF}$	X, L versions			0.35	mA
			H version			0.48	
I_{CC}	Operating supply current, switching	V_{DS} = 150 V, V_{COMP} = 1.2 V, F_{OSC} = 30 kHz			1.25	1.7	mA
		V_{DS} = 150 V, V_{COMP} = 1.2 V, F_{OSC} = 60 kHz			1.5	2	
		V_{DS} = 150 V, V_{COMP} = 1.2 V, F_{OSC} = 132 kHz			2.25	2.8	

Note: 1. *Current supplied only during the main MOSFET OFF time.*
2. *Parameter assured by design and characterization.*

Table 7. Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E/A						
V_{FB_REF}	Reference voltage		1.175	1.2	1.225	V
V_{FB_DIS}	E/A disable voltage		150	180	210	mV
$I_{FB\_PULL\ UP}$	Pull-up current		0.9	1	1.1	µA
G_M	Trans conductance	V_{COMP}=1.5 V, V_{FB} >VFBREF	400	550	700	µA/V
I_{COMP1}	Max. source current	V_{COMP}=1.5 V, V_{FB} =0.5 V	75	100	125	µA
I_{COMP2}	Max. sink current	V_{FB}=2 V, V_{COMP}=1.5 V	75	100	125	µA
$R_{COMP(DYN)}$	Dynamic resistance	V_{COMP}=2.7 V, V_{FB} =G_{ND}	13	15	17	kΩ
V_{COMPH}	Current limitation threshold		2.75	3.1	3.45	V
V_{COMPL}	PFM threshold		0.6	0.8	1	V
H_{COMP}	$\Delta V_{COMP}/\Delta I_{DRAIN}$	VIPER317*	3.8	4.2	4,6	
		VIPER318*	3.2	3.5	3.8	V/A
		VIPER319*	2.9	3.2	3.5	
OLP and timing						
I_{DLIM}	Drain current limitation	T_J= 25°C , VIPER317*	675	710	745	mA
		T_J= 25°C , VIPER318*	810	850	890	
		T_J= 25°C , VIPER319*	940	990	1040	
		VIPER317*(1)	639	710	781	
		VIPER318*(1)	765	850	935	
		VIPER319*(1)	891	990	1089	
I^2f	Power coefficient $I_{DLIM\_TYP}^2$ x F_{OSC_TYP}	VIPER317L	-10%	30.2	+10%	A^2·kHz
		VIPER317H		66.5		
		VIPER318X		21.7		
		VIPER318L		43.4		
		VIPER318H		95.4		
		VIPER319X		29.4		
		VIPER319L		58.8		
		VIPER319H		129.4		
I_{Dlim_PFM}	Drain current limitation at light load	T_J=25°C, V_{COMP}=V_{COMPL}(2) VIPER317* (1)	80	110	140	mA
		T_J=25°C, V_{COMP}=V_{COMPL}(2) VIPER318*(1)	100	130	160	
		T_J=25°C, V_{COMP}=V_{COMPL}(2) VIPER319*(1)	120	150	180	

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{OVL}	Overload delay time		45	50	55	ms
t_{OVL_max}	Max. overload delay time	When in pulse skipping			100	ms
t_{SS}	Soft-start time		5	8	11	ms
t_{ON_MIN}	Minimum turn-on time	V_{CC}=9 V, V_{COMP}=1 V, V_{FB}=V_{FB_REF}	250	300	350	ns
$t_{RESTART}$	Restart time after fault		0.625	1	1.375	s
UVP						
V_{UVP_th}	UVP threshold	V_{CC} =9 V, V_{COMP}=1 V, $V_{FB=VFB\_REF}$	0.38	0.4	0.42	V
$I_{UVP\_pull-up}$	UVP pull-up current			-1		µA
t_{UVP_DEB}	Debounce time before UVP tripping		18.75	30	41.25	ms
t_{UVP_REST}	Debounce time for restoring normal operation from UVP		18.75	30	41.25	ms
I_{q_DIS}	Quiescient current during UVP	Not switching, V_{FB}>V_{FB_REF}		0.25	0.35	mA
OVP						
V_{OVP_th}	Overvoltage protection threshold	V_{CC}=9 V, V_{COMP}=1 V, V_{FB}=V_{FB_REF}	3.85	4	4.15	V
t_{OVP_DEB}	Debounce time before OVP tripping		156	250	344	µs
t_{OVP_REST}	Restart time after overvoltage protection tripping		312	500	688	ms
Oscillator						
F_{OSC}	Switching frequency	T_J =25°C VIPER31*X	27	30	33	kHz
		T_J = 25°C, VIPER31*L	54	60	66	
		T_J = 25°C, VIPER31*H	119	132	145	
$F_{OSC\ MIN}$	Min. switching frequency	T_J= 25°C (3)	13.5	15	16.5	kHz
F_D	Modulation depth	(4)		±7·F_{OSC}		%
F_M	Modulation frequency	(4)		200		Hz
D_{MAX}	Max. duty cycle	(4)	70		80	%
Thermal shutdown protection						
T_{SD}	Thermal shutdown temperature threshold	(4)	150	160		°C

1. *Measured at Vin = 100 Vdc in Flyback topology, with 1.5 mH transformer primary inductance*
2. *See Section 4.10 Pulse frequency modulation*
3. *See Section 4.7 Pulse skipping*
4. *Parameter assured by design and characterization.*

3 Typical electrical characteristics

Figure 3. I_{DLIM} vs. T_J

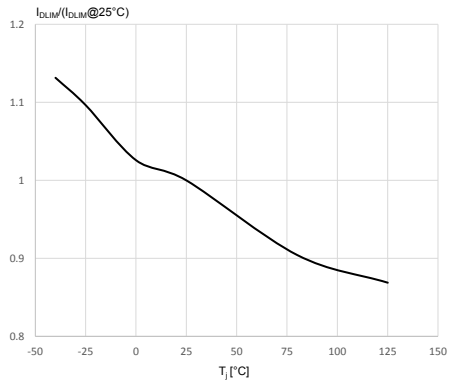


Figure 4. F_{OSC} vs. T_J

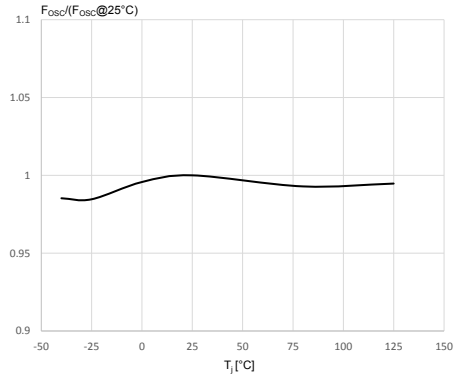


Figure 5. V_{HV_START} vs. T_J

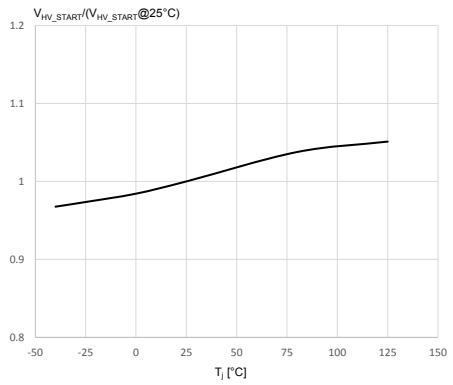


Figure 6. VF_{B_REF} vs. T_J

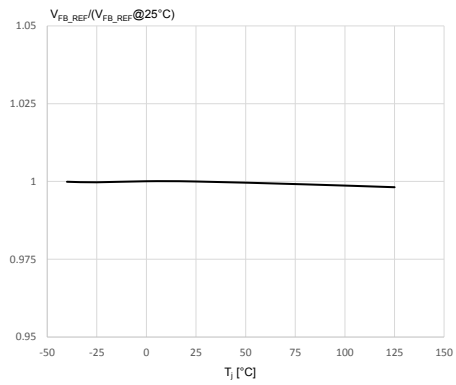


Figure 7. Quiescent Current I_q vs. T_J

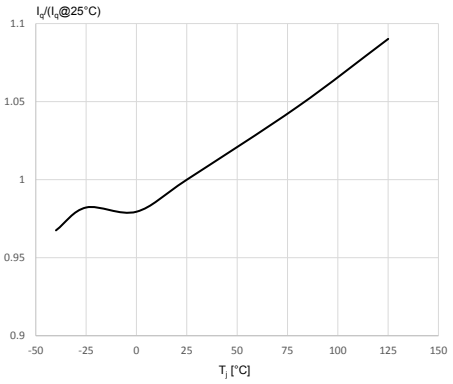


Figure 8. Operating current I_{CC} vs. T_J

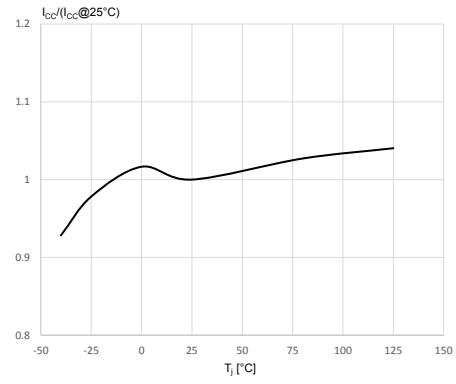


Figure 9. I_{CH1} vs. T_J

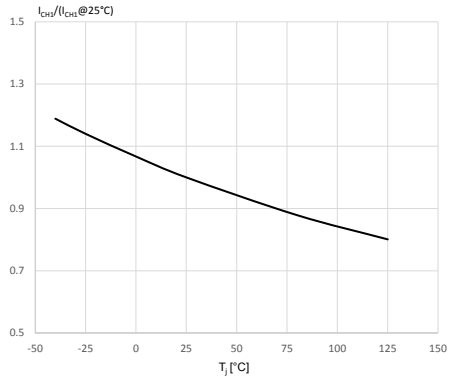


Figure 10. I_{CH2} vs. T_J

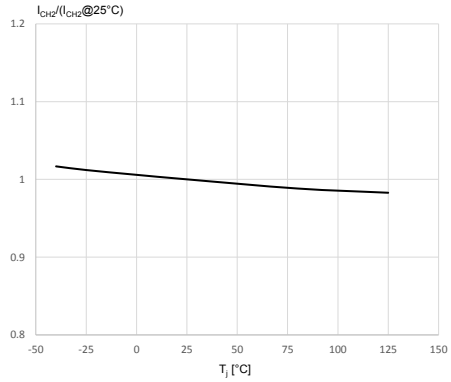


Figure 11. I_{CH1} vs. V_{DRAIN}

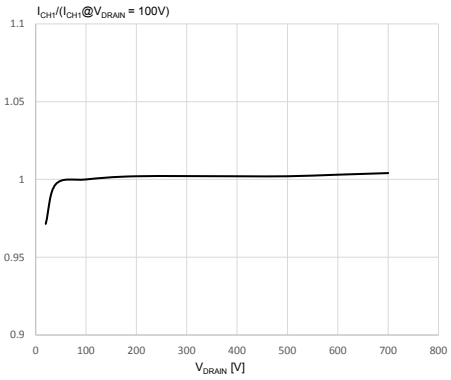


Figure 12. I_{CH2} vs. V_{DRAIN}

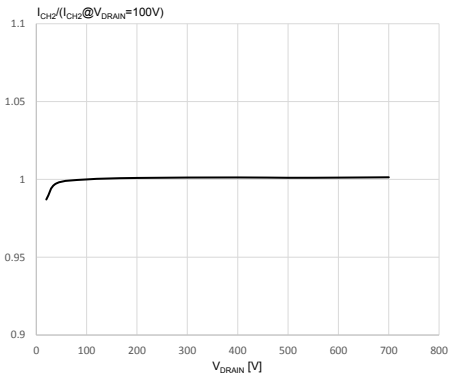


Figure 13. G_M vs. T_J

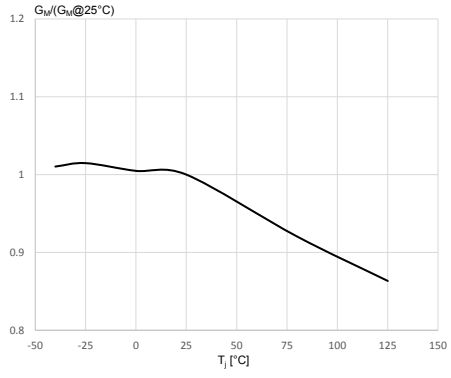


Figure 14. I_{COMP} vs. T_J

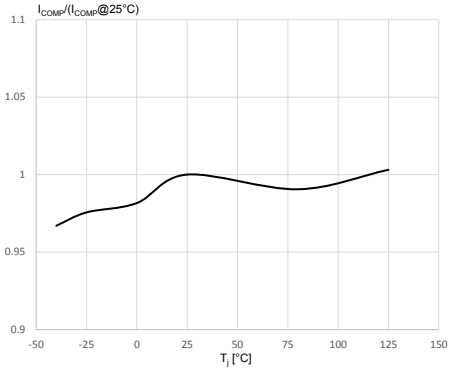


Figure 15. R_{DSON} vs. T_J

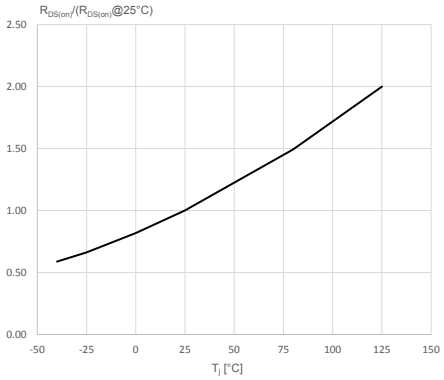


Figure 16. R_{DSON} vs. I_{DRAIN}

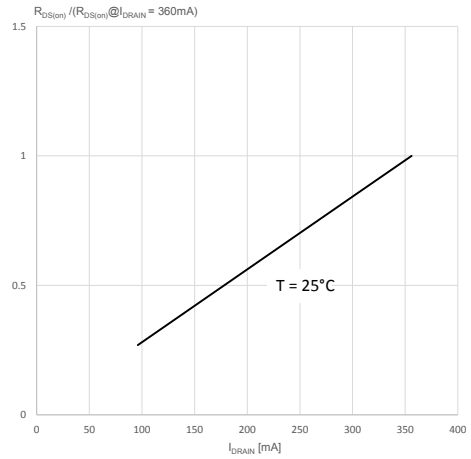


Figure 17. Static drain-source on resistance

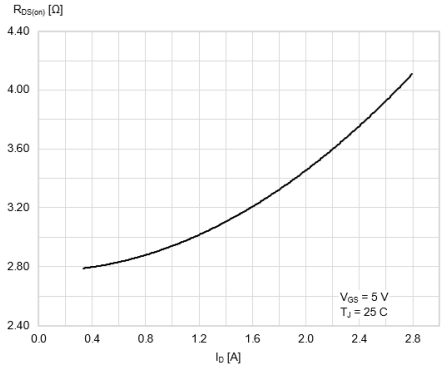


Figure 18. Power MOSFET C_{OSS} vs. V_{DS} @ V_{GS}=0, f=1MHz

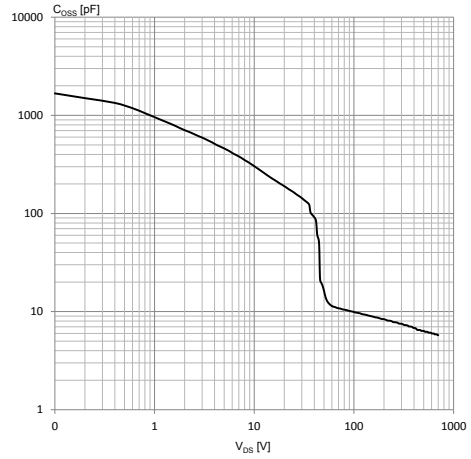


Figure 19. V_{BVDSS} vs. T_J

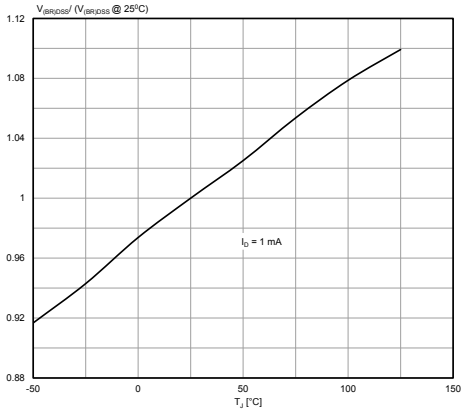


Figure 20. Output characteristic

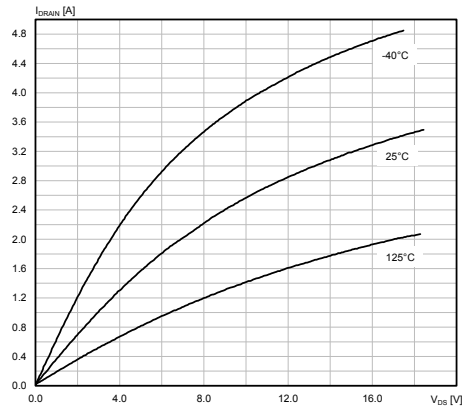


Figure 21. **SOA SO16N package**

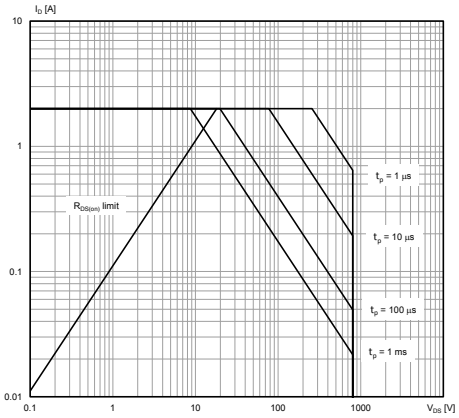
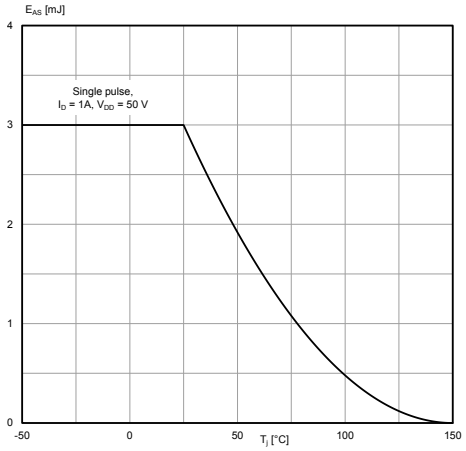


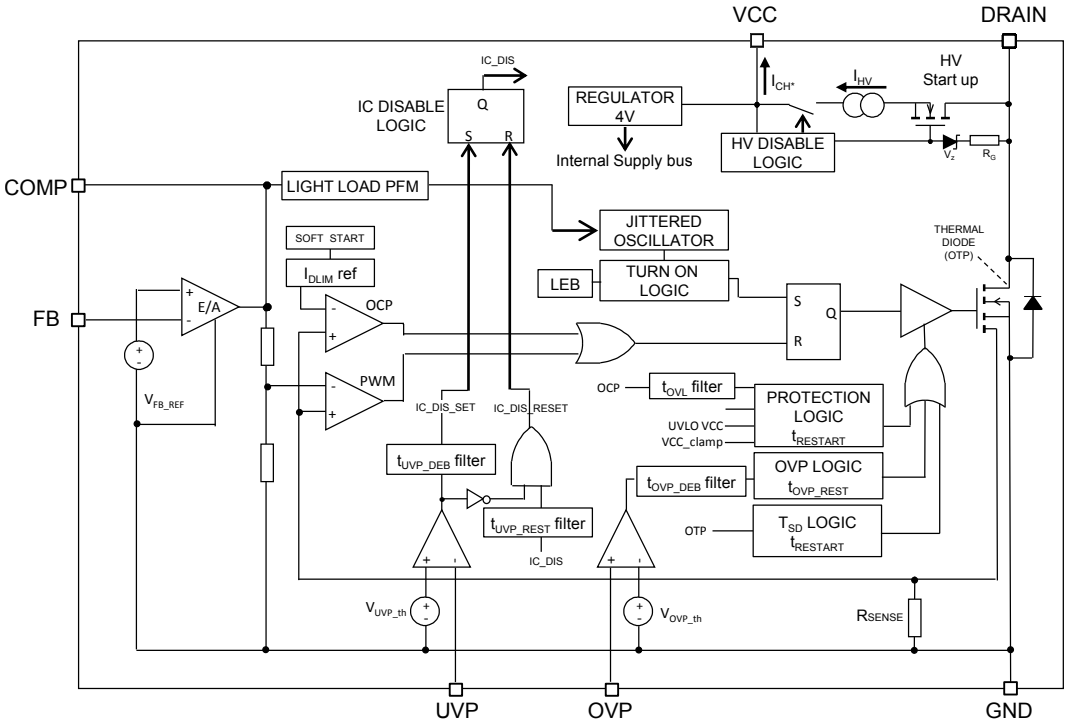
Figure 22. **Maximum avalanche energy vs. Tj**



4 General description

4.1 Block diagram

Figure 23. **Block diagram**



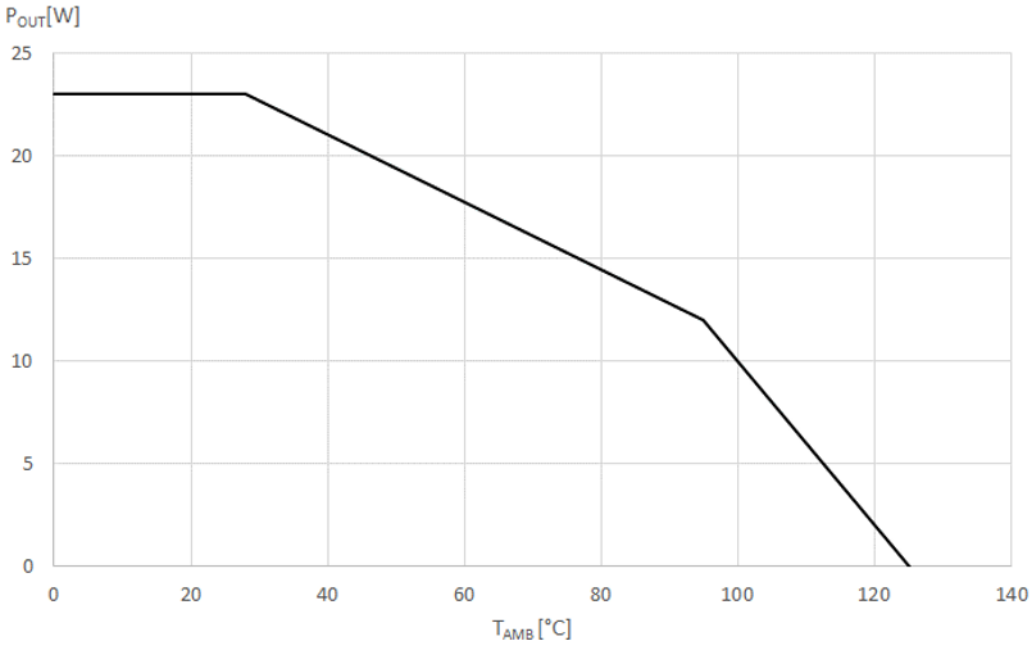
4.2 Typical power capability

Table 8. **Typical power**

Vin: 230 V_{AC}		Vin: 85-265 V_{AC}	
Adapter (1)	Open Frame (2)	Adapter (1)	Open Frame (2)
27 W	31 W	16 W	19 W

1. *Typical continuous power in non-ventilated enclosed adapter measured at 50°C ambient.*
2. *Maximum practical continuous power in an open frame design at 50°C ambient, with adequate heat sinking.*

Figure 24. **Typical deliverable output power vs. T_{AMB} (Vin: 85-265V_{AC})**



4.3 Primary MOSFET

The primary switch is implemented with an avalanche rugged N-channel MOSFET with 800 V minimum breakdown voltage, V_{BVDSS}, and 3.5 Ω maximum on-resistance, $R_{DS(on)}$.

The sense-FET is embedded and allows a virtually lossless current sensing.

The MOSFET gate driver controls the gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions the embedded pull-down circuit holds the gate low in order to ensure that the MOSFET cannot be turned on accidentally.

4.4 High-voltage startup

The embedded high-voltage startup includes both the 800 V startup FET, whose gate is biased through the resistor R_G, and the switchable HV current source, delivering the current I_{HV}. The major portion of I_{HV}, (I_{CH}), charges the capacitor connected to VCC pin. A minor portion is sunk by the controller block.

Power on: at startup, as the voltage across the DRAIN pin exceeds the V_{HV_START} threshold, the HV current source is turned on, charging linearly the VCC capacitor with the current I_{CH2} (8.8 mA typ.). This charging current is reduced to I_{CH1} (1 mA typ.) in case V_{CC} is lower than 1 V (typical value), in order to limit IC power dissipation in case the pin is accidentally shorted to GND.

As V_{CC} reaches the startup threshold, V_{CCon}, the chip starts operating, the primary MOSFET is enabled to switch, the HV current source is disabled and the device is powered by the energy stored in the VCC capacitor. The IC can be supplied through a transformer auxiliary winding or, in case of not isolated topologies with $V_{OUT} \geq 5$ V, directly from the converter's output.

The supply operating range is from 4.5 V to 30.5 V. If VCC pin voltage exceeds 30.5 V (referred to V_{GND}), the internal clamp could be reached, which causes the VIPER31 to stop switching.

This condition is potentially dangerous for the VIPER31 and must be avoided, by means of proper transformer design and/or external protection (zener diode between VCC and GND pins).

In normal operation the HV current source is always kept off by maintaining V_{CC} above V_{Cson}, so its residual consumption is given by the power dissipated on R_G only, calculated as follows:

Equation 1

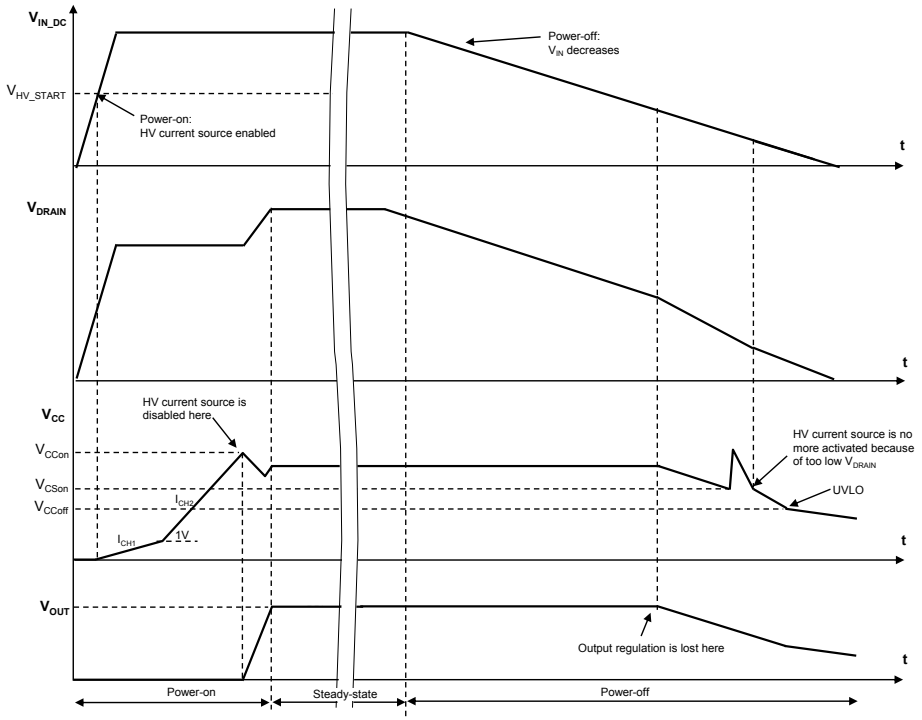
(1)

$$P_{HV}(V_{IN}) = V_{IN}^2/R_G$$

At nominal input voltage (230 V_{AC}), typical and worst-case consumptions are 2.4 mW and 3.0 mW respectively (corresponding to R_G_typ = 45 Mohm and R_G_min = 36 Mohm). This means that, with a careful design, the overall no-load input power consumption of the application can be maintained very low (typically, below 10 mW @230 V_{AC})

Power-off: when the IC is disconnected from the mains, or there is a mains interruption, for some time the converter keeps on working, powered by the energy stored in the input bulk capacitor. When it is discharged below a critical value, the converter is no longer able to keep the output voltage regulated. During the power down, when the DRAIN voltage becomes too low, the HV current source remains off and the IC is stopped as soon as V_{CC} drops below the UVLO threshold, V_{Ccoff}.

Figure 25. Power ON and power OFF



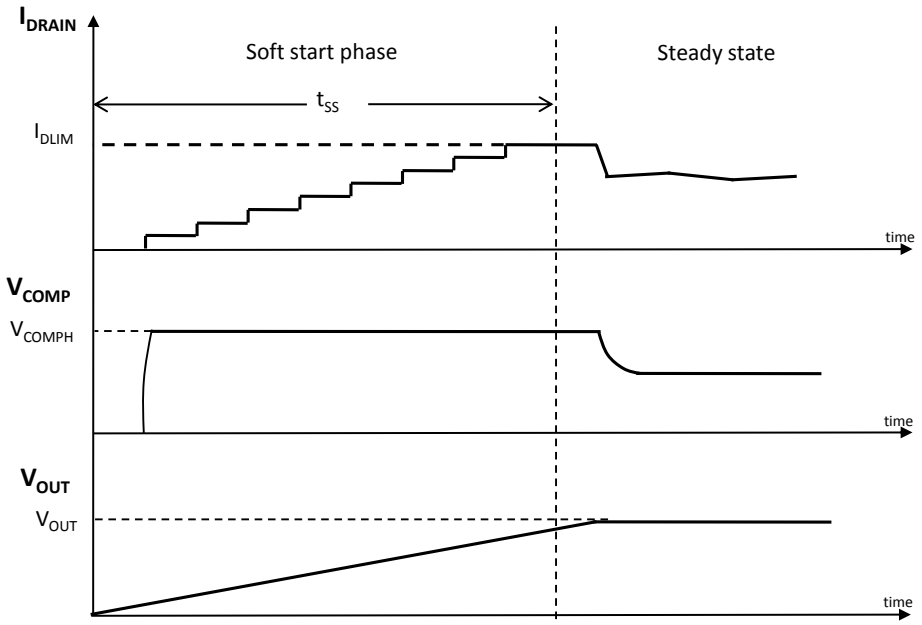
4.5 Soft startup

The internal soft-start function of the VIPer31 progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM}.

The soft-start time, t_{SS}, which is internally set at 8 ms, is activated at any attempt of converter power-on and at any restart after a fault event.

The feature is used to reduce the stress of the power components and increase the reliability of the system.

Figure 26. **Soft startup**



4.6 Oscillator

The IC embeds a fixed frequency oscillator with jittering feature. The switching frequency is modulated by approximately ±7%·F_{OSC} at 200 Hz rate. The purpose of the jittering is to get a spread-spectrum action that distributes the energy of each harmonic of the switching frequency over a number of frequency bands, having the same energy on the whole but smaller amplitudes. This helps to reduce the conducted emissions, especially when measured with the average detection method or, which is the same, to pass the EMI tests with an input filter of smaller size with respect to the one that should be needed in absence of jittering feature. Three switching frequency options, F_{OSC}, are available: 30 kHz (X type), 60 kHz (L type) and 132 kHz (H type).

4.7 Pulse skipping

The IC embeds a pulse skip circuit that operates in the following way:

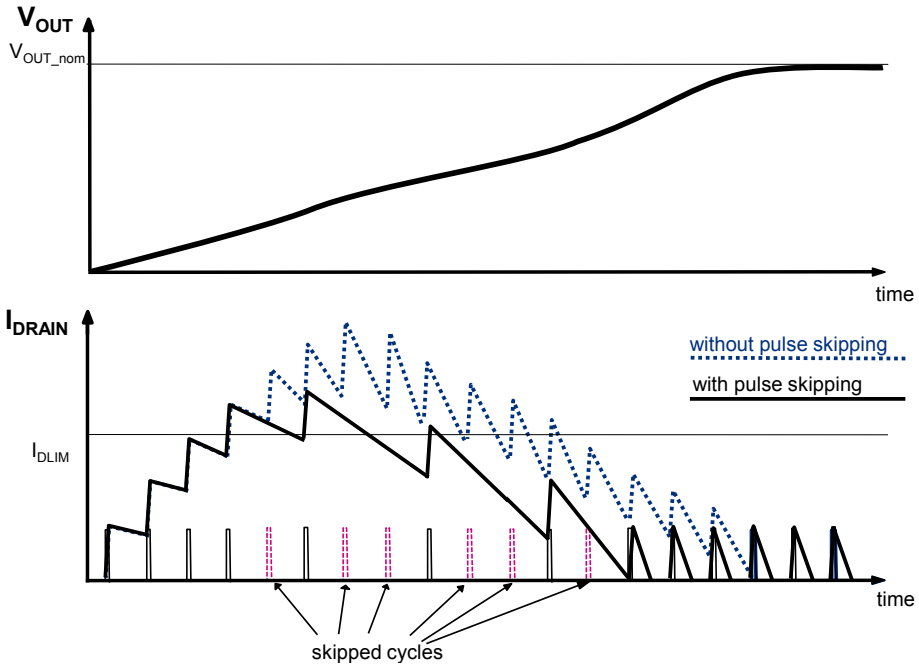
- Each time the DRAIN peak current exceeds I_{DLIM} level within t_{ON_MIN}, the next switching cycle is skipped. The cycles can be skipped until the minimum switching frequency F_{OSC_MIN} (15 kHz) is reached.
- Each time the DRAIN peak current does not exceed I_{DLIM} within t_{ON_MIN}, the next switching cycle is restored. The cycles can be restored until the nominal switching frequency FOSC is reached.

The protection is intended in order to avoid the so called “flux runaway” condition often present at converter startup and due to the fact that the primary MOSFET, which is turned on by the internal oscillator, cannot be turned off before the minimum on-time.

During the on-time, the inductor is charged through the input voltage and, if it cannot be discharged by the same amount during the off-time, in every switching cycle there is a net increase of the average inductor current, that can reach dangerously high values until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance. This condition is common at converter startup, because of the low output voltage.

In the following Figure 27. Pulse skipping during startup the effect of pulse skipping feature on the DRAIN peak current shape is shown (solid line), compared with the DRAIN peak current shape when pulse skipping feature is not implemented (dashed line). Providing more time for cycle-by-cycle inductor discharge when needed, this feature is effective in keeping low the maximum DRAIN peak current avoiding the flux runaway condition.

Figure 27. **Pulse skipping during startup**



4.8 Direct feedback

The IC embeds a transconductance type error amplifier (E/A) whose inverting input and output are FB and COMP, respectively. The internal reference voltage of the E/A is V_{FB_REF} (1.2 V typical value referred to GND). In non-isolated topologies, a positive output voltage can be tightly set through a simple voltage divider applied among the output voltage terminal, FB and GND.

The E/A output is scaled down and fed into the PWM comparator, where it is compared to the voltage across the sense resistor in series to the sense-FET, thus setting the cycle-by-cycle drain current limitation.

An R-C network connected on the output of the error amplifier (COMP) is usually used to stabilize the overall control loop.

The FB is provided with an internal pull-up to prevent a wrong IC behavior when the pin is accidentally left floating.

The E/A is disabled if the FB voltage is lower than V_{FB_DIS} (200 mV, typ).

4.9 Secondary feedback

When a secondary feedback is required, the internal E/A has to be disabled shorting FB to GND ($V_{FB} < V_{FB\_DIS}$). With this setting, COMP is internally connected to the parallel of a 100 uA current generator and the 15 kΩ (typ.) $R_{COMP(DYN)}$ resistor, and the voltage across COMP is set by the current sunk.

This allows to set the output voltage value through an external error amplifier (TS431 or similar) placed on the secondary side, whose error signal is used to set the DRAIN peak current setpoint corresponding to the output power demand. If isolation is required, the error signal must be transferred through an optocoupler, with the phototransistor collector connected across COMP and GND.

4.10 Pulse frequency modulation

If the output load is decreased, the feedback loop reacts by lowering V_{COMP}, which reduces the DRAIN peak current setpoint. The minimum value is I_{DLIM_PFM}, corresponding to the V_{COMPL} threshold.

If the load is further decreased, the DRAIN peak current value is maintained at I_{DLIM_PFM} and some PWM cycles are skipped. This kind of operation is referred to as “pulse frequency modulation” (PFM), the number of the skipped cycles depending on the balance between the output power demand and the power transferred from the input. The result is an equivalent switching frequency which can go down to some hundreds Hz, thus reducing all the frequency-related losses.

This kind of operation, together with the extremely low IC quiescent current, allows very low input power consumption in no-load and light load, while the low DRAIN peak current value, I_{DLIM_PFM}, prevents any audible noise which could arise from low switching frequency values. When the output load is increased, V_{COMP} increases and PFM is exited. V_{COMP} reaches its maximum at V_{COMPH}, corresponding to the DRAIN current limitation (IDLIM).

4.11 Overload protection

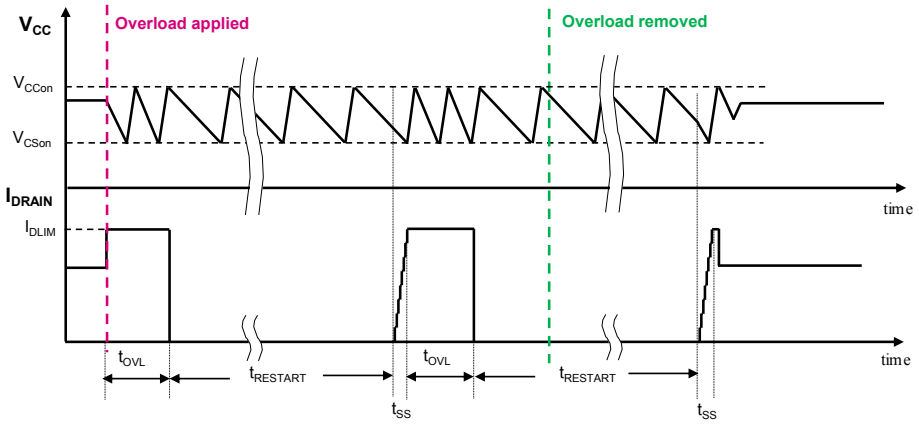
In order to manage the overload condition the IC embeds the following main blocks: the OCP comparator to turn off the power MOSFET when the drain current reaches its limit (I_{DLIM}), the up and down OCP counter to define the turn-off delay time in case of continuous overload (t_{OVL} = 50 ms typ.) and the timer to define the restart time after protection tripping ($t_{RESTART}$ = 1 sec, typ.).

In case of short-circuit or overload, the control level on the inverting input of the PWM comparator is greater than the reference level fed into the inverting input of the OCP comparator. As a result, the cycle-by-cycle turn off of the power switch is triggered by the OCP comparator instead of by the PWM comparator. Every cycle this condition is met, the OCP counter is incremented. If the fault condition persists for a time greater than t_{OVL} (corresponding to the counter end-of-count), the protection is tripped, the PWM is disabled for $t_{RESTART}$, then it resumes switching with soft-start and, if the fault is still present, it is disabled again after t_{OVL}. The OLP management prevents the IC from being indefinitely operated at I_{DLIM} and the low repetition rate of the restart attempts of the converter avoids overheating the IC in case of repeated fault events.

After the fault removal, the IC resumes working normally. If the fault is removed before the protection tripping (before t_{OVL}), the t_{OVL} counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the fault is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period ot have elapsed before resuming switching.

In fault condition, V_{CC} is kept between V_{CSon} and V_{CCon} by the periodical activation of the HV current source, which recharges the VCC capacitor to V_{Ccon} any time the IC internal consumption discharges it to V_{Cson}.

Figure 28. Overload protection



4.12 Undervoltage protection

If the voltage across the UVP pin (V_{UVP}) falls below the internal threshold V_{UVP_th} (0.4 V typ.) for a time greater than t_{UVP_DEB} (30 ms, typ.), the IC is disabled and its consumption is reduced to ultra-low values (I_{q_DIS}).

When V_{UVP} rises above V_{UVP_th}, the IC must wait t_{UVP_REST} (30 ms, typ.) before resuming switching.

Both t_{UVP_DEB} and t_{UVP_REST} are intended to filter out possible noises/disturbances of the line, which could affect the correct operation of the function. They are obtained through two separate up/down counters:

DEB (REST) up/down counter has a deb_eoc (rest_eoc) end-of-count. The operation is illustrated in Figure 29. UVP timing.

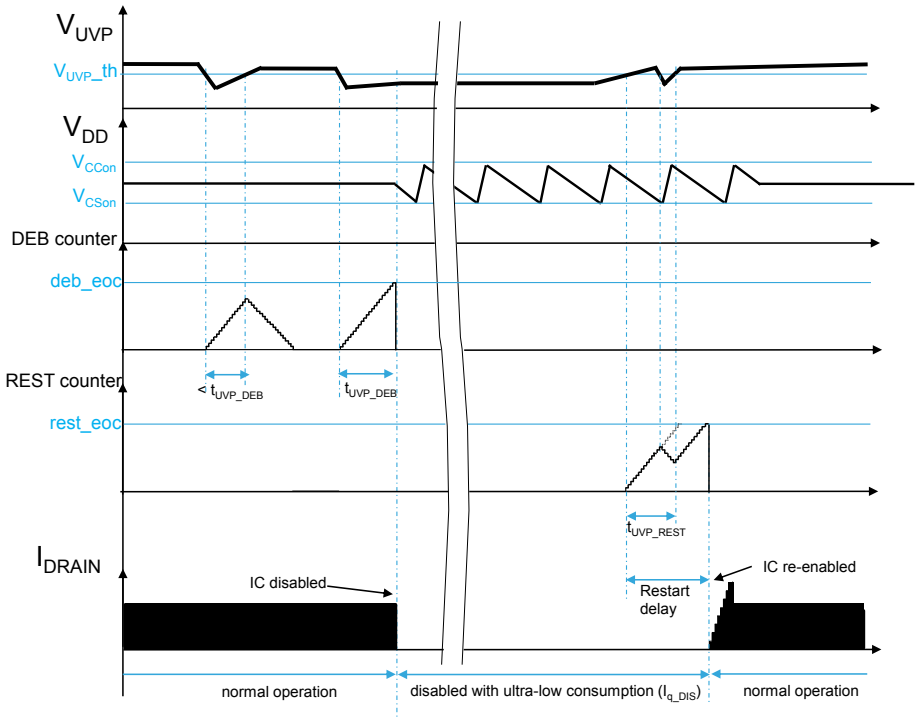
If the counter starts from zero and counts always up, end-of-count is reached in a time interval t_{UVP_DEB} (t_{UVP_REST}).

If V_{UVP} falls below V_{UVP_th}, the DEB counter is incremented. If V_{UVP} increases above V_{UVP}_th before uvp_eoc is reached, the counter is decremented. If the count goes back down to zero, a disturbance on the UVP pin is assumed and there is no consequence on the IC behavior.

If V_{UVP} stays below V_{UVP_th} until the counter reaches deb_eoc: the device is disabled; most of the internal blocks are turned off and the internal consumption is reduced to I_{q_DIS}; V_{CC} is maintained between V_{Cson} and V_{Ccon} by the periodical activation of the internal HV-current source; the DEB counter is reset. Of course, if during the count-up V_{UVP} exceeds V_{UVP_th} for some time, the DEB counter is decremented during that time and the IC disable is delayed accordingly.

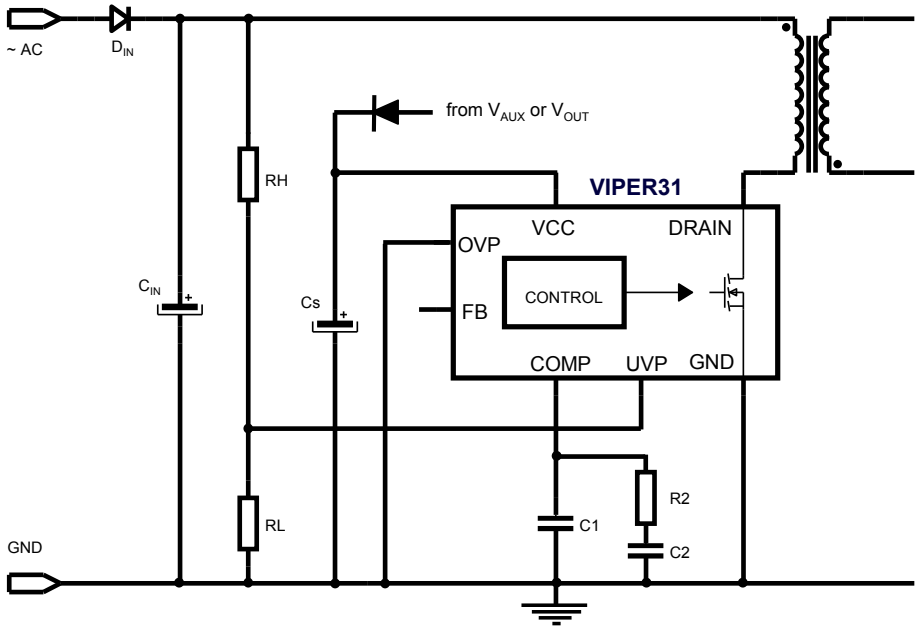
With IC disabled: if V_{UVP} rises above V_{UVP_th}, the REST counter is incremented, and when it reaches rest_eoc (corresponding to t_{UVP_REST}), the IC resumes switching. Of course, if during the count-up, V_{UVP} falls below V_{UVP_th} for some time, the REST counter is decremented during that time and the IC re-enabling is delayed accordingly.

Figure 29. UVP timing



An input undervoltage protection can be easily realized connecting the rectified mains to UVP pin through a voltage divider, as shown in Figure 30. Connection for input undervoltage protection/disable (isolated or non-isolated topologies).

Figure 30. **Connection for input undervoltage protection/disable (isolated or non-isolated topologies)**



If UVP function is not required, the UVP pin must be left floating. In this case, noise immunity of the pin is guaranteed by the internal pull-up $I_{UVP\_pull\text{-}up}$ (1 uA, typ.) present in the UVP block.

If UVP function is required, RH value can be set arbitrarily, but some Mohms at least are recommended in order to minimize the power consumption of the UVP network. Then, if V_{in_UVP} is the desired input undervoltage threshold, the value of RL can be found from the following formula:

Equation 2

(2)

$$RL = \frac{V_{UVP\_th}}{\frac{V_{in\_UVP} - V_{UVP\_th}}{RH} + I_{UVP\_pull-up}}$$

Equation 3

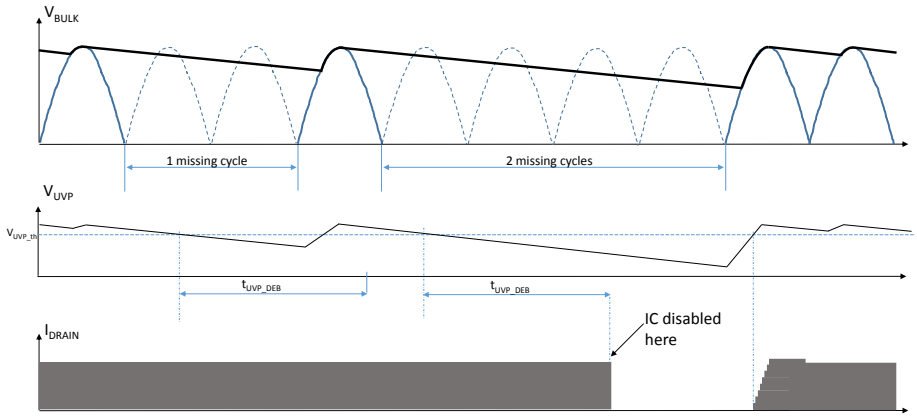
(3)

$$PUVP\left(Vin\right) = \frac{Vin^2}{RH + RL}$$

Thanks to the ultra-low consumption, the UVP pin can be used as an input to disable the SMPS from external, reaching the lowest input power consumption while the SMPS is still connected to the AC mains but not delivering power to its output.

The purpose of the UVP debounce time t_{UVP_DEB} is also to guarantee some hold-up in case of a missing cycle of the input line, as illustrated in Figure 31. Hold-up in case of input line missing cycles.

Figure 31. **Hold-up in case of input line missing cycles**



4.13 Overvoltage protection

If the voltage across OVP pin (V_{OVP}) exceeds the internal threshold V_{OVP_th} (4 V typ.) for a time greater than t_{OVP_DEB} (250 us, typ.), the PWM is disabled in autorestart for t_{OVP_REST} time (500 ms, typ.), until V_{OVP} falls below V_{OVP_th}.

The time interval t_{OVP_DEB} is intended to filter out possible noises/disturbances of the line, which could affect the correct operation of the function, and is obtained through an up/down counter, where t_{OVP_DEB} is the time the counter needs to reach its end-of-count (ovp_eoc) starting from zero and counting always up.

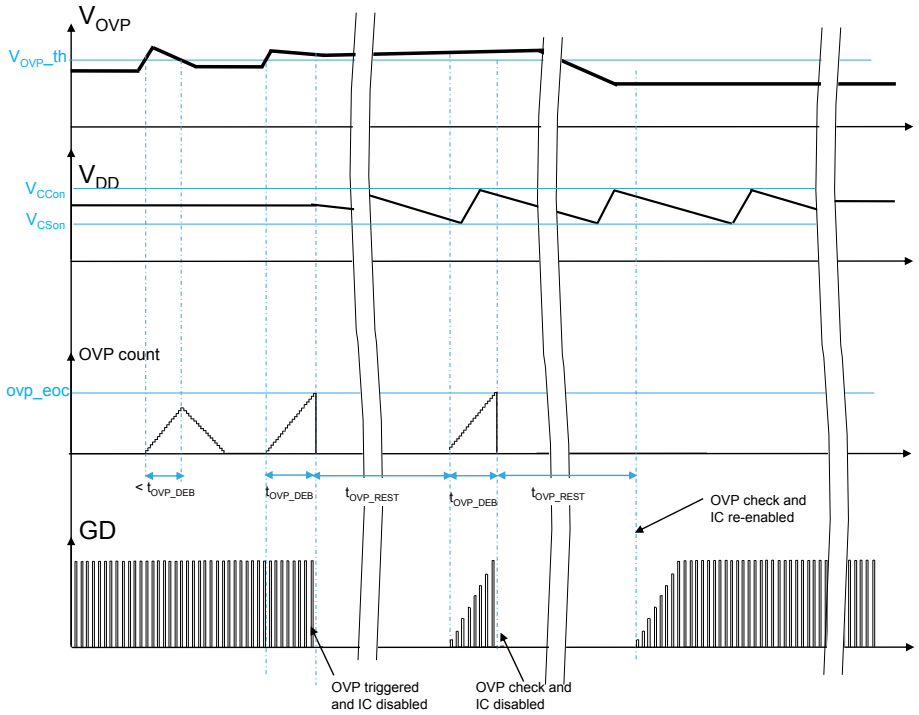
The operation is shown in Figure 32. OVP timing. When V_{OVP} exceeds V_{OVP_th}, the up/down OVP counter is incremented.

If V_{OVP} falls below V_{OVP_th} before the OVP counter reaches ovp_eoc, the counter is decremented. If the count goes down to zero, a disturbance on the OVP pin is assumed and there is no consequence on the IC behavior.

If V_{OVP} stays above V_{OVP_th} until the OVP counter reaches ovp_eoc: the PWM is disabled in autorestart for a t_{OVP_REST} time interval; the OVP counter is reset; V_{CC} is maintained between V_{Cson} and V_{Ccon} by the periodical activation of the internal HV-current source. Of course, if during the count-up V_{OVP} falls below V_{OVP_th} for some time, during that time the counter is decremented and the PWM disable is delayed accordingly.

When V_{OVP} drops below V_{OVP_th}, the IC waits for the end of t_{OVP_REST}, then restarts with soft-start phase.

Figure 32. **OVP timing**



An input overvoltage protection can be easily realized connecting the rectified mains to OVP pin through a voltage divider, as shown in Figure 33. Connection for input overvoltage protection (iso/non-iso topologies).

In case of non-isolated topologies, with the same principle an output overvoltage protection can be implemented, as shown in Figure 34. Connection for output overvoltage protection (non-iso topologies).

If the OVP feature is not required, OVP pin must be connected to GND, which excludes the function.

If the OVP feature is required, RH value can be set arbitrarily, but some Mohms at least are recommended in order to minimize the power consumption of the OVP network. Then, if V_{in/out_OVP} is the desired input/output overvoltage threshold, the value of RL can be calculated from the following formula:

Equation 4

(4)

$$RL = \frac{RH}{\frac{V_{in/out\_OVP}}{V_{OVP\_th}} - 1}$$

The power consumption of the OVP network at given Vin is expressed as:

Equation 5

(5)

$$\mathrm{POVP}\left(\mathrm{Vin}\right) = \frac{\mathrm{Vin}^2}{\mathrm{RH} + \mathrm{RL}}$$

in case of connection for input overvoltage protection and

Equation 6

(6)

$$\mathrm{POVP}\left(\mathrm{VOUT}\right) = \frac{\mathrm{VOUT}^2}{\mathrm{RH} + \mathrm{RL}}$$

in case of connection for output overvoltage protection.

Figure 33. **Connection for input overvoltage protection (iso/non-iso topologies)**

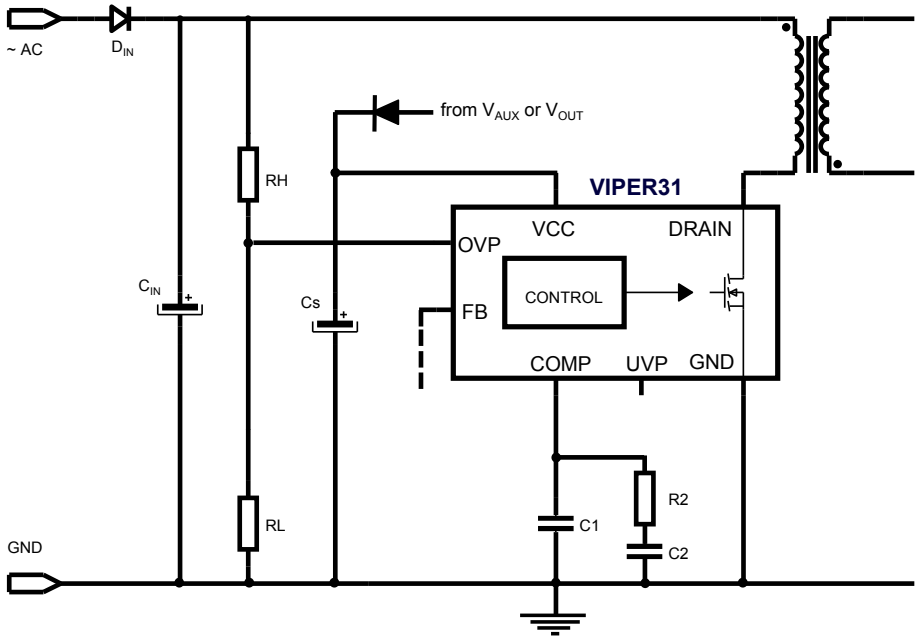
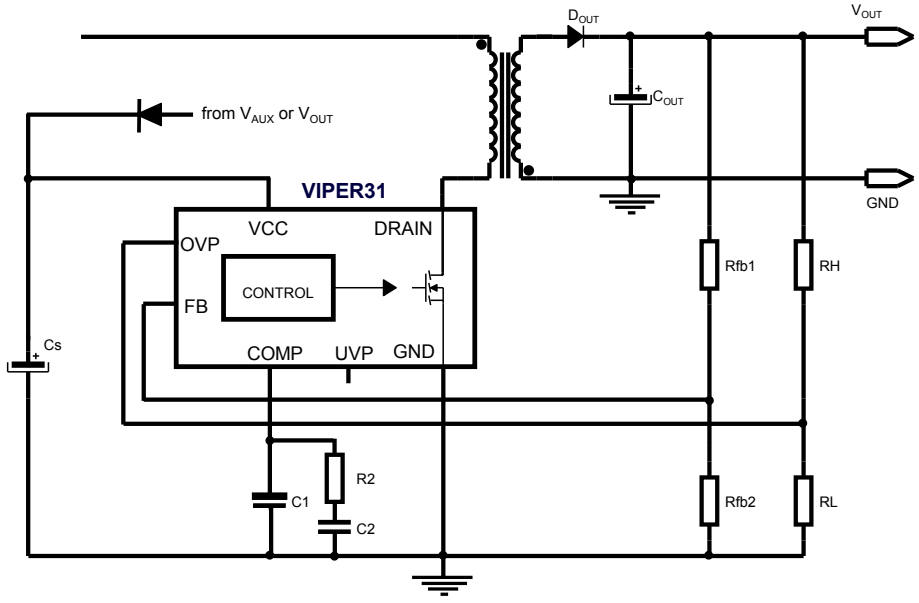


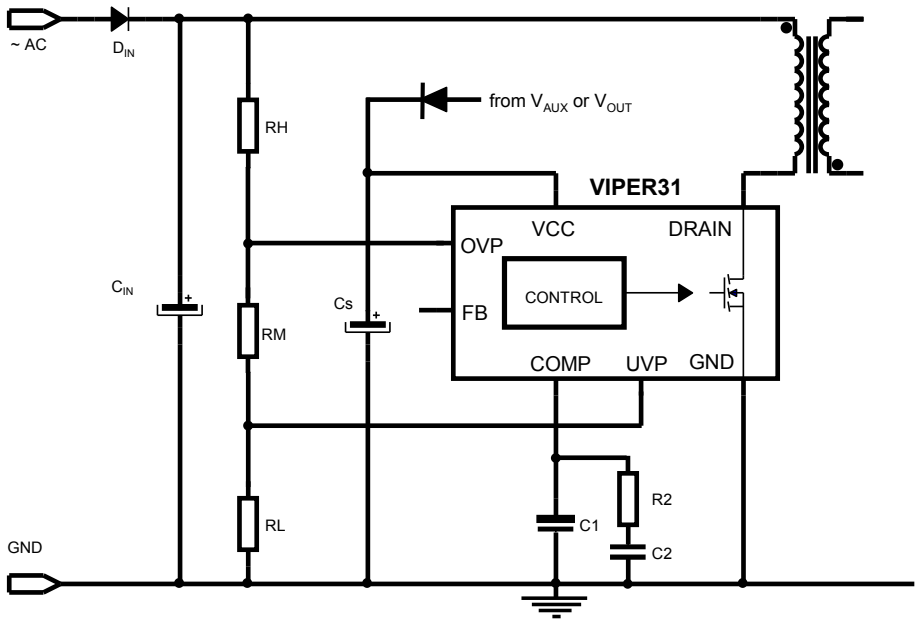
Figure 34. **Connection for output overvoltage protection (non-iso topologies)**



4.14 Undervoltage and overvoltage protection

If both undervoltage and overvoltage protections are required, they can be set independently from each other through a single voltage divider, as illustrated in the figure below.

Figure 35. **Connection for input and output overvoltage protections (iso/non-iso topologies)**



The voltage divider equations are:

Equation 7

(7)

$$V_{in\_UVP} = \left(\frac{V_{UVP\_th}}{RL} - I_{UVP\_pull-up}\right) \cdot (RH + RM + RL) + RL \cdot I_{UVP\_pull-up}$$

Equation 8

(8)

$$V_{in\_OVP} = \left(V_{OVP\_th} - \frac{RH}{RH + RM + RL} \cdot \left(RL \cdot I_{UVP\_pull-up}\right)\right) \cdot \frac{RH + RM + RL}{RM + RL}$$

Considering that the value of RH is much higher than the values of RM and RL (Mohms vs. kohms), equations 7 and 8 can be approximated into Eq. 7.a) and Eq. 8.a) respectively:

Equation 7.a

(7.a)

$$V_{in\_UVP} \sim \left(\frac{V_{UVP\_th}}{RL} - I_{UVP\_pull-up}\right) \cdot RH + RL \cdot I_{UVP\_pull-up}$$

Equation 8.a

(8.a)

$$V_{in\_OVP} \sim \left(V_{OVP\_th} - RL \cdot I_{UVP\_pull-up}\right) \cdot \frac{RH}{RM + RL}$$

Selecting arbitrarily the RH value, Equation 7.a) can be solved for RL:

Equation 9

(9)

$$RL = \frac{V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH - \sqrt{\left(V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH\right)^2 - 4 \cdot V_{UVP\_th} \cdot I_{UVP\_pull-up} \cdot RH}}{2 \cdot I_{UVP\_pull-up}}$$

and Equation 8.a) for RM:

Equation 10

(10)

$$RM = \left(V_{OVP\_th} - RL \cdot I_{UVP\_pull-up}\right) \cdot \frac{RH}{V_{in\_OVP}} - RL$$

The power consumption of the UVP-OVP network at given Vin is expressed as:

Equation 11

(11)

$$P_{UVP\_OVP}\left(V_{in}\right) = \frac{V_{in}^2}{RH + RM + RL}$$

As an example, if V_{in_UVP} and V_{in_OVP} design values are 50 Vdc and 450 Vdc respectively, and RH is set to 6 Mohm: from Equations 9 and 10 we have RL = 43 kohm, and RM = 60 kohm respectively, while from Equation 11 the power consumption of the network at 230 Vac is about 17 mW.

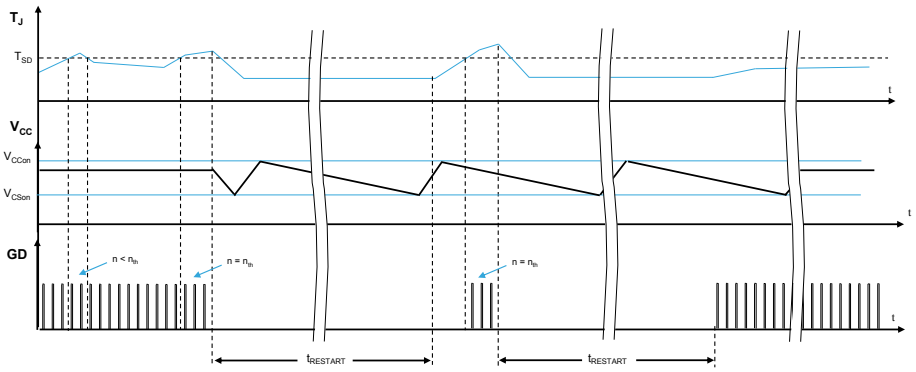
4.15 Thermal shutdown

The power MOSFET junction temperature is sensed during the on-time through a diode integrated into the HV section of the chip. If a junction temperature higher than the internal threshold TSD (160°C, typ.) is measured, the PWM is disabled for $t_{RESTART}$. In order to increase robustness against electromagnetic noises, the protection is triggered only if the condition is met for nth = 3 consecutive switching cycles.

After $t_{RESTART}$, the IC resumes switching with soft-start phase: if a junction temperature above TSD is still measured for nth consecutive switching cycles, the protection is triggered and PWM is disabled again for $t_{RESTART}$; otherwise normal operation is restored.

During $t_{RESTART}$, V_{CC} is maintained between V_{Cson} and V_{Ccon} by the HV current source periodical activation. Such a behavior is summarized in Figure 36. Thermal shutdown timing diagram.

Figure 36. Thermal shutdown timing diagram



5 Application information

5.1 Typical schematics

Figure 37. **Flyback converter (non-isolated)**

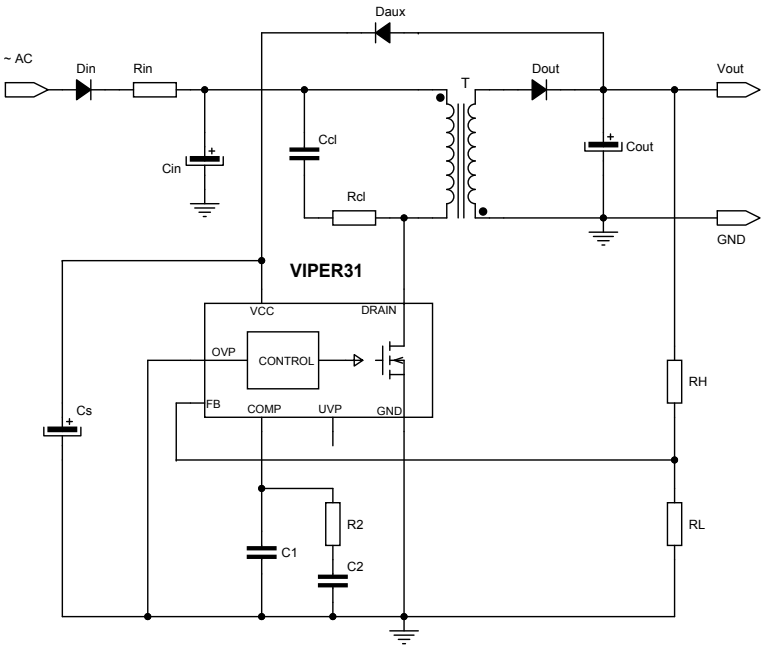


Figure 38. **Flyback converter (isolated)**

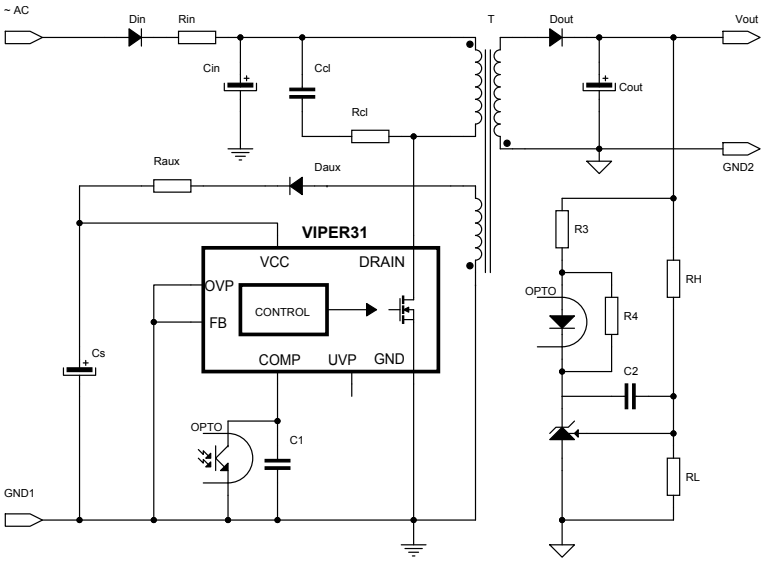


Figure 39. **Flyback converter (primary regulation)**

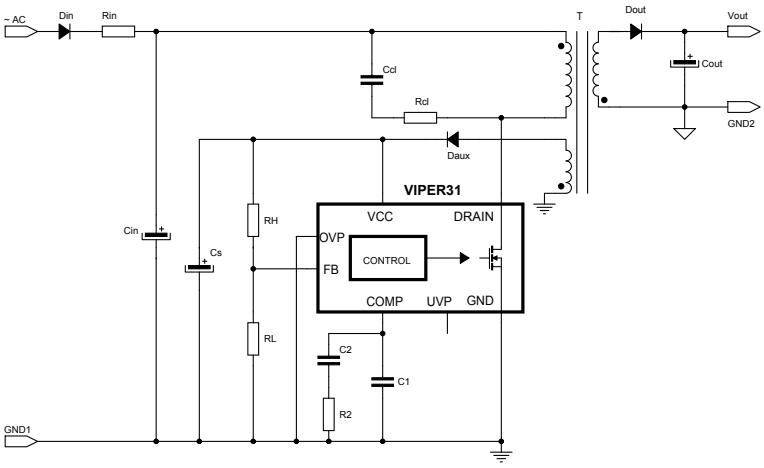


Figure 40. **Buck converter**

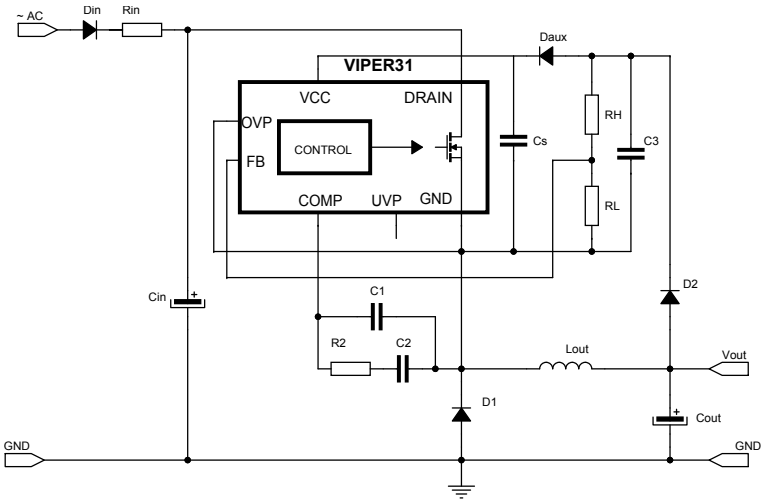
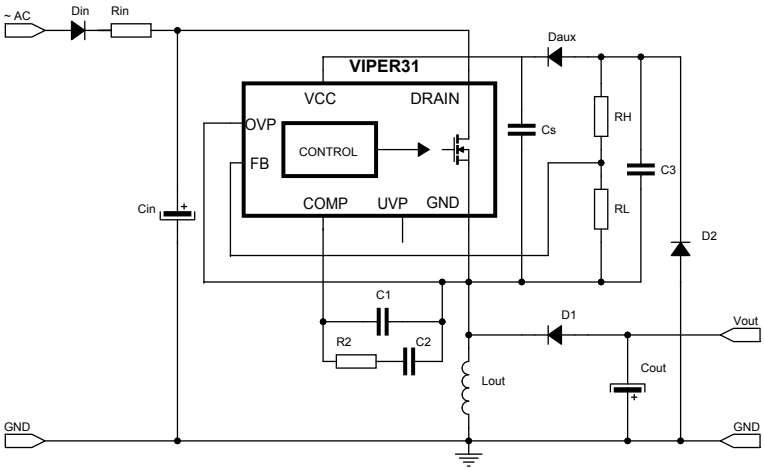


Figure 41. **Buck-boost converter**



5.2 Energy saving performances

The VIPer31 allows the design of applications compliant with the most stringent energy saving regulations. In order to show the typical performances achievable, the active mode average efficiency and the efficiency at 10% of the rated output power of a single output flyback converter using VIPer31 have been measured and are reported in Table 9. In addition, Figures 52 and 53 show no-load and light load consumptions.

Table 9. Power supply efficiency, VOUT = 15 V

Parameter	V_{IN}	10% output load efficiency [%]	Active mode average efficiency [%]	Pin @ no-load [mW]
Flyback iso, 15V/1.2A	115 V_{AC}	83.2	85.9	26.0
	230 V_{AC}	77.4	86.6	29.7

Figure 42. PIN versus VIN in no-load, VOUT = 15V

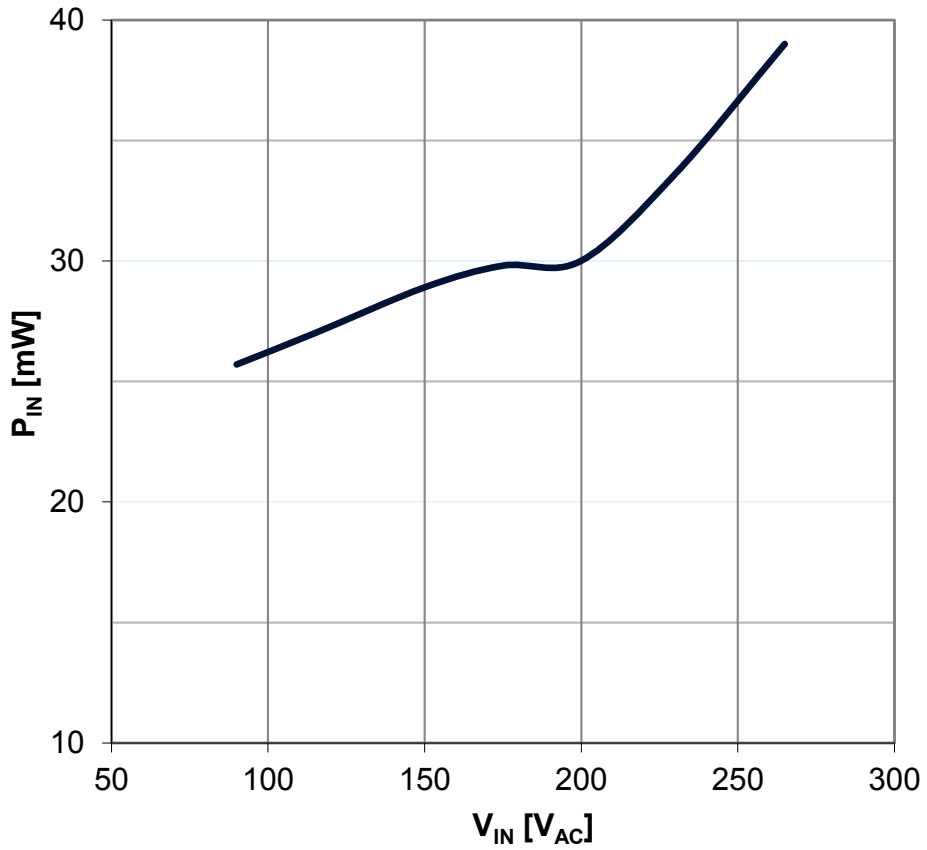
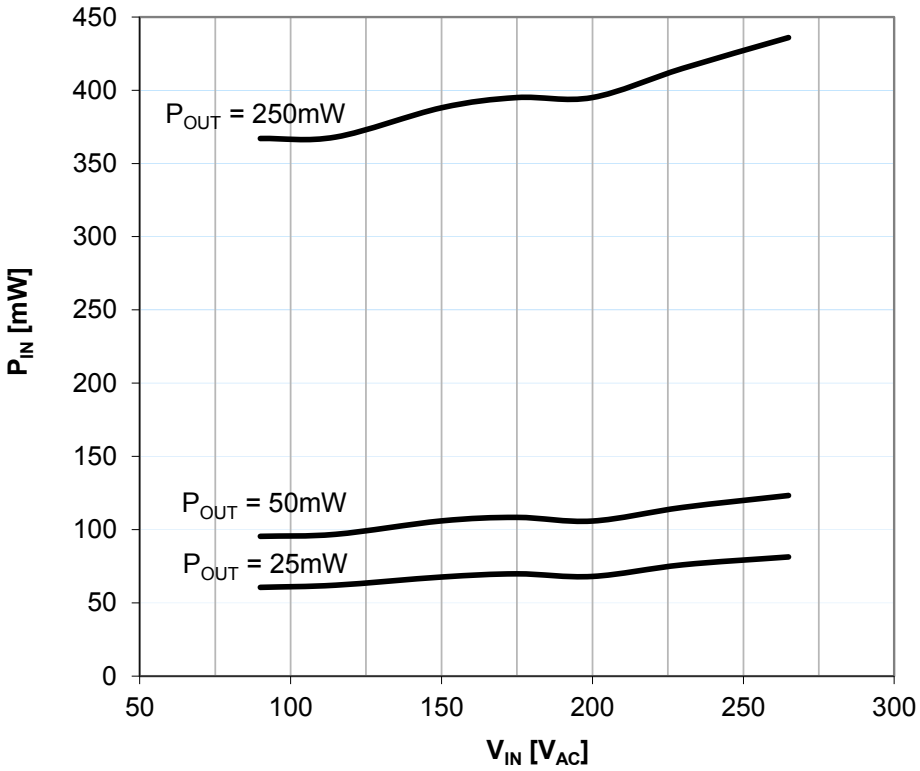


Figure 43. **PIN versus VIN in light-load, VOUT = 15V**



5.3 Layout guidelines and design recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the VIPer as well. The main reasons to have a proper PCB layout are to:

- Provide clean signals to the IC, ensuring good immunity against external noises and switching noises
- Reduce the electromagnetic interferences, both radiated and conducted, to pass more easily the EMC

When designing an SMPS using VIPer, the following basic rules should be considered:

- **Separating signal from power tracks:** generally, traces carrying signal currents should run far from those carrying pulsed currents or with quickly swinging voltages. Signal ground traces should be connected to the IC signal ground, GND, using a single “star point”, placed close to the IC. Power ground traces should be connected to the IC power ground, GND. The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible. In case of two layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.
- **Filtering sensitive pins:** some crucial points of the circuit need or may need filtering. A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 µF) should be connected across VCC and GND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.
- **Keep power loops as confined as possible:** minimize the area circumscribed by current loops where high pulsed currents flow, in order to reduce its parasitic self-inductance and the radiated electromagnetic field: this greatly reduces the electromagnetic interferences produced by the power supply during the switching. In a flyback converter the most critical loops are: the one including the input bulk capacitor, the power switch, the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier and the output capacitor. In a buck converter the most critical loop is the one including the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.
- **Reduce line lengths:** any wire acts as an antenna. With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high-voltage spikes. By reducing line lengths, the level of radiated energy that is received is reduced, and the resulting spikes from electrostatic discharges are lower. This also keeps both resistive and inductive effects to a minimum. In particular, all of the traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and fat as possible.
- **Optimize track routing:** as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them when designing the power path.
- **Improve thermal dissipation:** an adequate copper area has to be provided under the DRAIN pins as heat sink, while it is not recommended to place large copper areas on the GND.

Figure 44. **Recommended routing for flyback converter**

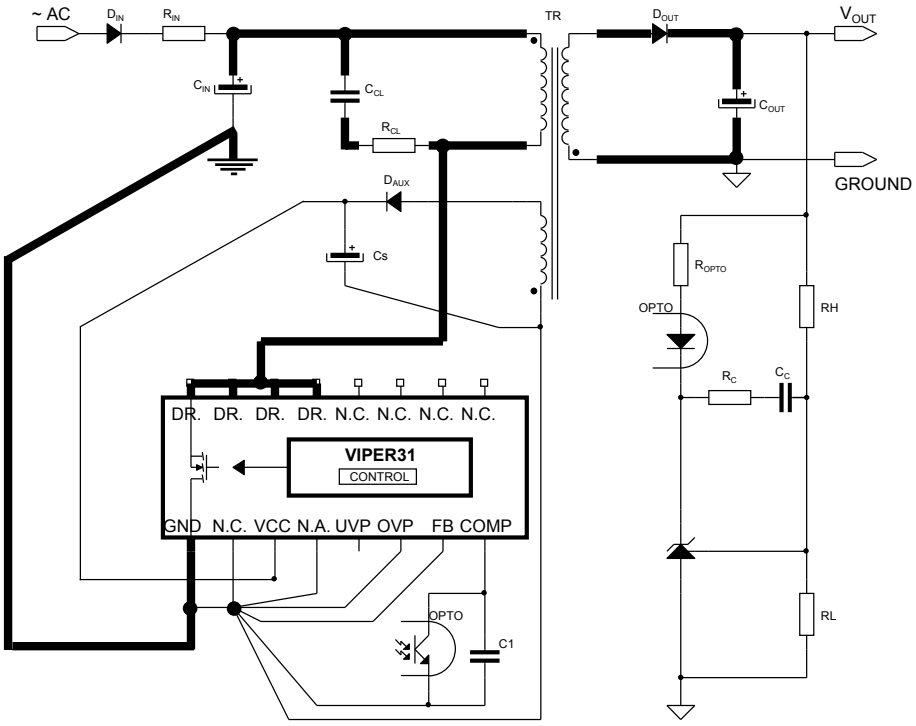
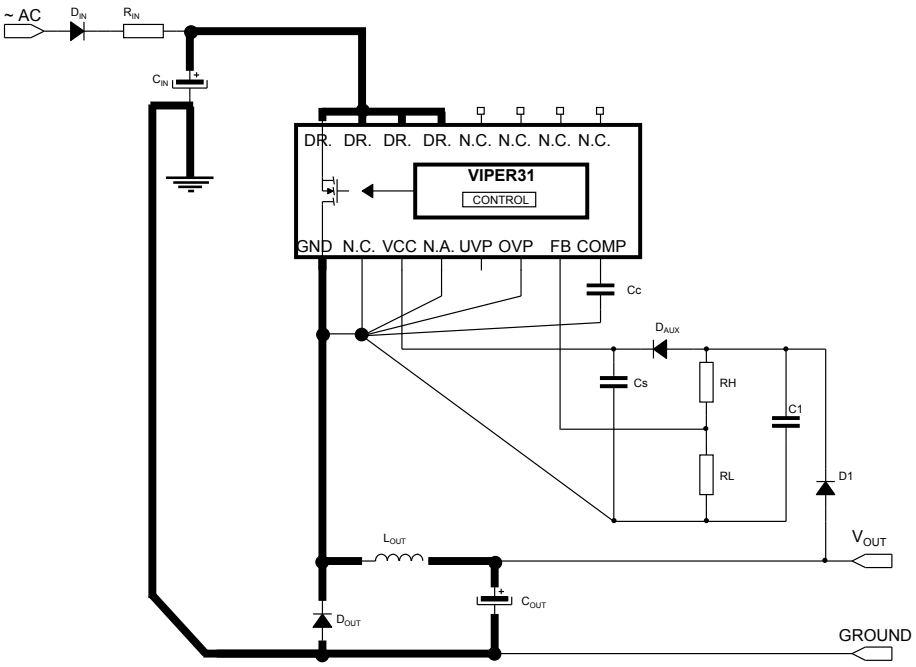


Figure 45. **Recommended routing for buck converter**



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO16N package information

Figure 46. SO16N package outline

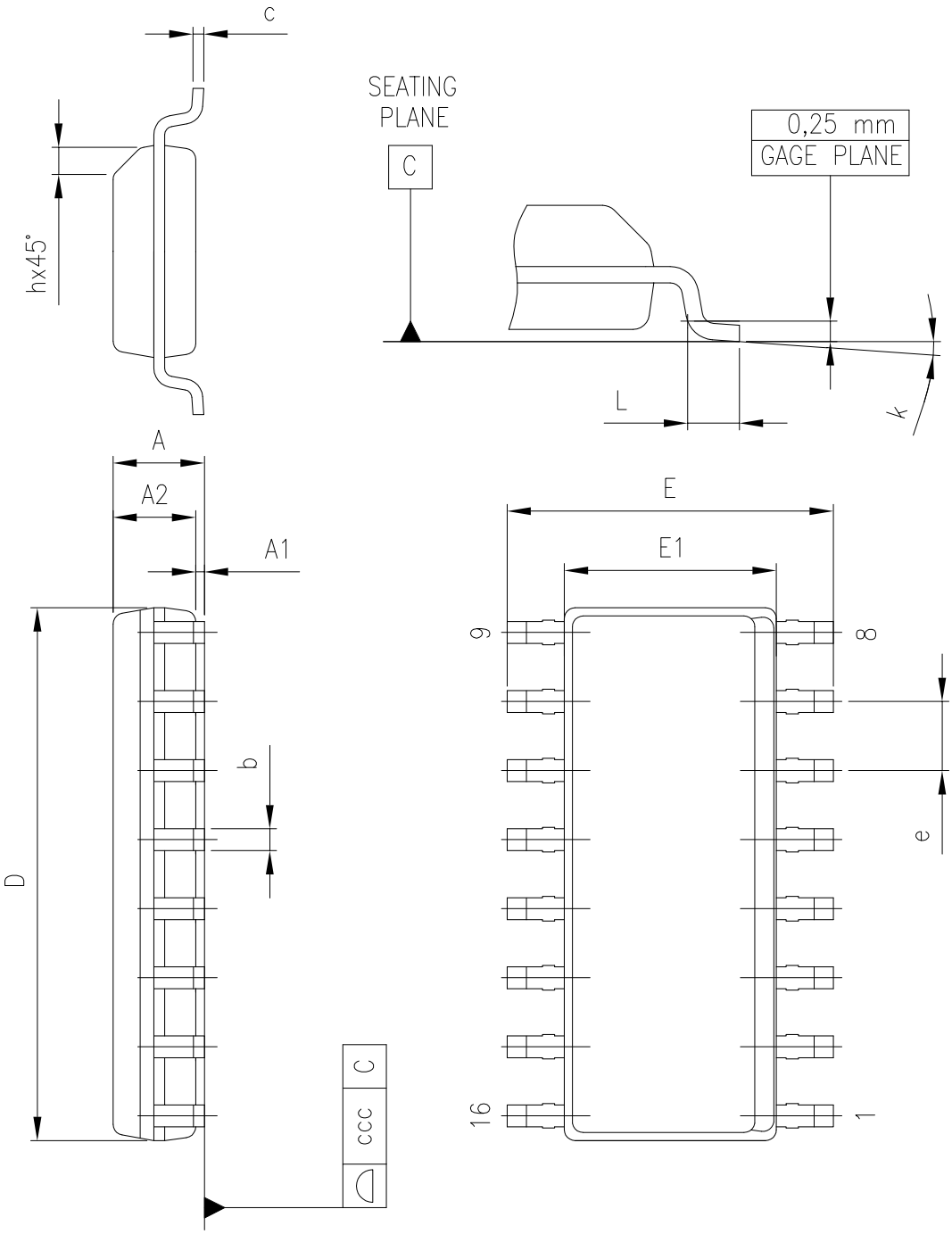


Table 10. **SO16N mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

7 Order code

Table 11. **Order code**

Order code	I_{DLIM} (OCP) typ	FOSC ± jitter	Package
VIPER318XDTR	**850** mA	30 kHz ± 7%	SO16N tape and reel
VIPER319XDTR	**9**90 mA		
VIPER317LDTR	**7**10 mA	60 kHz ± 7%	
VIPER318LDTR	**85**0 mA		
VIPER319LDTR	**9**90 mA		
VIPER317HDTR	**7**10 mA	132 kHz ± 7%	
VIPER318HDTR	**85**0 mA		
VIPER319HDTR	**9**90 mA		

Revision history

Table 12. **Document revision history**

Date	Version	Changes
31-Mar-2020	1	Initial release.
8-Jun-2020	2	Updated Section Features; updated Table 6, Table 7, Table 11; updated figures in Section 5.1 Typical schematics; minor text update.
17-Nov-2020	3	Added data for VIPER317/318/319 in Section Features, in Table 7 and Table 11

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