Product Specifications		
PART NO.:	**VL37R4G63B-D4SB**	**REV: 1.0**

GENERAL INFORMATION

32GB 4Gx64 DDR5 SDRAM NON-ECC UNBUFFERED UDIMM 288-PIN

Description

The VL37R4G63B is a 4Gx64 DDR5 SDRAM UDIMM module provide a high speed, high density, low power consumption and high stability. This dual rank memory module consists of sixteen DDR5 SDRAMs 2Gx8 bits with 32 banks (8 bank group) in BGA packages, and a 1024 bytes SPD EEPROM with Hub function (SPD5 Hub), and a PMIC added on the module improves power regulation, reduces motherboard complexity and brings a better DIMM-level power delivery. This module is a 288-pin dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR5 SDRAM.

Features

- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Dual rank
- Fast data transfer rate: 4800MT/s
- VDD = VDDQ = 1.1V (1.067V min ~ 1.166V max)
- VPP = 1.8V (1.746V min ~ 1.908V max)
- 32 Banks (8 Bank Group)
- Programmable CAS latency (posted CAS): 40 (DDR5-4800)
- Programmable Additive Latency: CL-2 clock
- 16-bit prefetch
- Burst Length: 16 by default
- Bi-directional Differential Data-Strobe
- Internal ZQ calibration
- On Die Termination (ODT)
- Average Refresh period:
  3.9us at Tcase < 85ºC, 1.95us at 85ºC < Tcase < 95ºC
- Connectivity Test Mode (TEN) is supported
- Asynchronous reset
- SPD with Hub function, Integrated Temperature Sensor (0.5ºC accuracy)
- Lead-free, RoHS compliant
- JEDEC standard compliant
- Gold edge contacts
- PCB: Height 31.25mm (1.230”), double sided component
- Operating temperature (TOPER): - Commercial (0ºC to +95ºC)
  - Industrial (-40ºC to +95ºC)

Order Information:

VL37R4G63B - D4 S B - X

- OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- DRAM DIE: B
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  D4: DDR5-4800 @ CL40
- VL: Lead-free/RoHS

DRAM component: SAMSUNG K4RAH086VB-BCQK

Pin Description

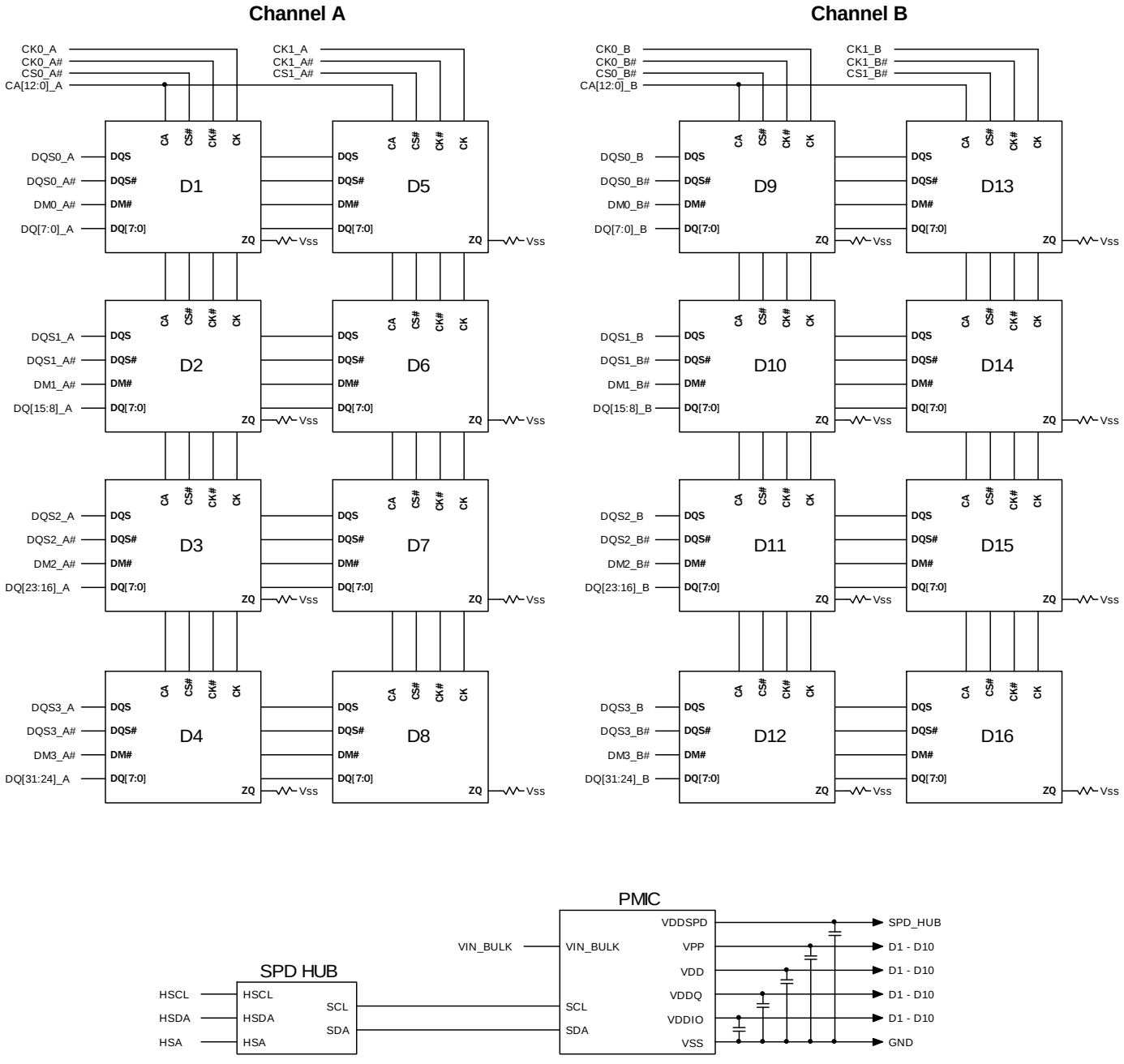
Pin Name	Function
CA0_A ~ CA12_A, CA0_B ~ CA12_B	SDRAM Command/Address bus
CS0_A# ~ CS1_A#, CS0_B# ~ CS1_B#	SDRAM Chip Select
DQ0_A ~ DQ31_A, DQ0_B ~ DQ31_B	DIMM memory data bus
*CB0_A ~ CB3_A, *CB0_B ~ CB3_B	DIMM ECC check bits
DQS0_A ~ DQS4_A, DQS0_B ~ DQS4_B	SDRAM data strobes (positive line of differential pair)
DQS0_A# ~ DQS4_A#, DQS0_B# ~ DQS4_B#	SDRAM data strobes (negative line of differential pair)
DM0_A# ~ DM3_A#, DM0_B# ~ DM3_B#	SDRAM data masks
CK0_A, CK1_A, CK0_B, CK1_B	SDRAM clocks (positive line of differential pair)
CK0_A#, CK1_A#, CK0_B#, CK1_B#	SDRAM clocks (negative line of differential pair)
HSCL	SidebandBus clock
HSDA	SidebandBus data
HSA	SidebandBus address
ALERT#	SDRAM ALERT
RESET#	Set DRAMs to a Known State
VIN_BULK	5V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use
*: These pins are not used in this module.	

PIN CONFIGURATION - UNBUFFERED DIMM

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	145	VIN_BULK	50	VSS	194	DQ31_A	96	VSS	240	DQS4_B
2	RFU	146	VIN_BULK	51	CB0_A*	195	VSS	97	CB0_B*	241	VSS
3	RFU	147	PWR_GOOD	52	VSS	196	CB2_A*	98	VSS	242	CB2_B*
4	HSCL	148	HSA	53	CB1_A*	197	VSS	99	CB1_B*	243	VSS
5	HSDA	149	RFU	54	VSS	198	CB3_A*	100	VSS	244	CB3_B*
6	VSS	150	VSS	55	DQS4_A#	199	VSS	101	DQ0_B	245	VSS
7	RFU	151	PWR_EN	56	DQS4_A	200	ALERT#	102	VSS	246	DQ2_B
8	VSS	152	RFU	57	VSS	201	VSS	103	DQ1_B	247	VSS
9	DQ0_A	153	VSS	58	CS0_A#	202	CS1_A#	104	VSS	248	DQ3_B
10	VSS	154	DQ2_A	59	VSS	203	VSS	105	DQS0_B#	249	VSS
11	DQ1_A	155	VSS	60	CA0_A	204	CA1_A	106	DQS0_B	250	DM0_B#
12	VSS	156	DQ3_A	61	CA2_A	205	CA3_A	107	VSS	251	VSS
13	DQS0_A#	157	VSS	62	VSS	206	VSS	108	DQ4_B	252	DQ6_B
14	DQS0_A	158	DM0_A#	63	CA4_A	207	CA5_A	109	VSS	253	VSS
15	VSS	159	VSS	64	CA6_A	208	CA7_A	110	DQ5_B	254	DQ7_B
16	DQ4_A	160	DQ6_A	65	VSS	209	VSS	111	VSS	255	VSS
17	VSS	161	VSS	66	CA8_A	210	CA9_A	112	DQ8_B	256	DQ10_B
18	DQ5_A	162	DQ7_A	67	CA10_A	211	CA11_A	113	VSS	257	VSS
19	VSS	163	VSS	68	VSS	212	VSS	114	DQ9_B	258	DQ11_B
20	DQ8_A	164	DQ10_A	69	CA12_A	213	RFU	115	VSS	259	VSS
21	VSS	165	VSS	70	RFU	214	RFU	116	DM1_B#	260	DQS1_B#
22	DQ9_A	166	DQ11_A	71	VSS	215	VSS	117	VSS	261	DQS1_B
23	VSS	167	VSS	72	CK0_A	216	CK1_A	118	DQ12_B	262	VSS
24	DM1_A#	168	DQS1_A#	73	CK0_A#	217	CK1_A#	119	VSS	263	DQ14_B
25	VSS	169	DQS1_A	74	VSS	218	VSS	120	DQ13_B	264	VSS
26	DQ12_A	170	VSS	75	RFU	219	RFU	121	VSS	265	DQ15_B
27	VSS	171	DQ14_A	KEY				122	DQ16_B	266	VSS
28	DQ13_A	172	VSS					123	VSS	267	DQ18_B
29	VSS	173	DQ15_A					124	DQ17_B	268	VSS
30	DQ16_A	174	VSS	76	RFU	220	RFU	125	VSS	269	DQ19_B
31	VSS	175	DQ18_A	77	VSS	221	VSS	126	DQS2_B#	270	VSS
32	DQ17_A	176	VSS	78	CK0_B	222	CK1_B	127	DQS2_B	271	DM2_B#
33	VSS	177	DQ19_A	79	CK0_B#	223	CK1_B#	128	VSS	272	VSS
34	DQS2_A#	178	VSS	80	VSS	224	VSS	129	DQ20_B	273	DQ22_B
35	DQS2_A	179	DM2_A#	81	RFU	225	RFU	130	VSS	274	VSS
36	VSS	180	VSS	82	CA12_B	226	RFU	131	DQ21_B	275	DQ23_B
37	DQ20_A	181	DQ22_A	83	VSS	227	VSS	132	VSS	276	VSS
38	VSS	182	VSS	84	CA10_B	228	CA11_B	133	DQ24_B	277	DQ26_B
39	DQ21_A	183	DQ23_A	85	CA8_B	229	CA9_B	134	VSS	278	VSS
40	VSS	184	VSS	86	VSS	230	VSS	135	DQ25_B	279	DQ27_B
41	DQ24_A	185	DQ26_A	87	CA6_B	231	CA7_B	136	VSS	280	VSS
42	VSS	186	VSS	88	CA4_B	232	CA5_B	137	DM3_B#	281	DQS3_B#
43	DQ25_A	187	DQ27_A	89	VSS	233	VSS	138	VSS	282	DQS3_B
44	VSS	188	VSS	90	CA2_B	234	CA3_B	139	DQ28_B	283	VSS
45	DM3_A#	189	DQS3_A#	91	CA0_B	235	CA1_B	140	VSS	284	DQ30_B
46	VSS	190	DQS3_A	92	VSS	236	VSS	141	DQ29_B	285	VSS
47	DQ28_A	191	VSS	93	CS0_B#	237	CS1_B#	142	VSS	286	VQ31_B
48	VSS	192	DQ30_A	94	VSS	238	VSS	143	RFU	287	VSS
49	DQ29_A	193	VSS	95	RESET#	239	DQS4_B#	144	RFU	288	RFU

*: These pins are not used in this module.

FUNCTION BLOCK DIAGRAM



Notes:

1. ZQ resistors are 240 ohms +/-1%

SPEED BIN

Symbol	D4 DDR5-4800 (40-40-40)[1]	Unit
tCK(min)	0.416	ns
CAS Latency	40	nCK
tRCD(min)	16.640	ns
tRP(min)	16.640	ns
tRAS(min)	32.000	ns
tRC(min)	48.640	ns
Note: 1. Speed bin is in order of CL-nRCD-nRP		

ADDRESS CONFIGURATION

Configuration		2Gb x8
Bank Address	BG Address	BG0~BG2
	Bank Address in a BG	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32
Row Address		R0~R15
Column Address		C0~C9
Page size		1KB

AC & DC OPERATING CONDITIONS

DDR5 DIMM Voltage Requirements

The DIMM input voltage requirements and the SDRAM voltage requirements are not identical. The DIMM voltage requirements must meet the PMIC input voltage requirements. The PMIC output voltage requirements must meet the SDRAM voltage requirements. There must be some allowance for a small voltage drop across the DIMM for both supply voltages and PMIC output voltages. Table 15 defines the requirements from the Host at the DIMM socket and at the post-PMIC SDRAM pin. Some modules have lower current requirements. Each specific module configuration must meet the PMIC 50x0, SDRAM, DDR5RCDxx and DDR5DBxx voltage requirements for its worst case supply currents

DC Operating Conditions[1,2,3]

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (A)	Power State
		Min	Typical	Max		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2.5/2.0	Operational
SWA, SWB	PMIC Output Supply Voltage	-	1.1	-	6	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	12	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	2	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020	Operational

NOTE:

1. During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply.
2. The ramp up rate between 300 mV and 4.0 V.
3. The ramp down rate between 4.0 V and 300 mV.
4. The area under the curve above VIN_Bulk = TBD V. VIN_Bulk_AC spec must also be satisfied.
5. The minimum input current requirement is to deliver the maximum output current on VOUT_1.8V and VOUT_1.0V LDO plus the current
6. VIN_Bulk = 5.0 V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static
7. VIN_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load. VR_EN signal is static
8. 20 MHz bandwidth limited measurement for all voltages in the table
9. Voltages are measured at the DIMM gold fingers and at PMIC output pins
10. The SDRAM specification must be met and take precedence over this document
11. Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances
12. Typical voltage is platform dependent. This is a suggested value only

Operating Temperature Ranges

Parameter/Condition	Device Rating	Symbol	Min	Normal	Extended
Commercial Temperature	CT	TOPER-CT	0ºC	85ºC	95ºC
Industrial Temperature	IT	TOPER-IT	-40ºC	85ºC	95ºC

NOTE:

1. The operating temperature is the case surface temperature on the center-top side of the DDR5 device. For measurements conditions, refer to JESD51-2
2. Normal is the maximum limit when device is operating in the Normal Temperature Mode
3. Extended is the maximum limit when device is operating in the Extended Temperature Mode
4. Support for the Industrial Temperature device is TBD

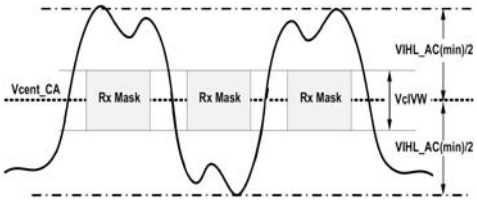
INPUT/OUTPUT MEASUREMENT LEVELS

DRAM CA, CS Input Levels

Symbol	Parameter	D4 DDR5-4800		Unit	Note
		Min	Max		
VciVW	CA Rx Mask voltage p - p	-	130	mV	1,2,4
TciVW	CA Rx Timing Window	-	0.2	UI	1,2,3,4,8
VIHL_AC	CA Input Pulse Amplitude	-	150	mV	7
TciPW	CA Input Pulse Width	0.58		UI	5,8
SRIN_cIVW	Input Slew Rate over VciVW	1	7	V/ns	6

NOTE:

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift
2. Rx mask voltage VciVW total(max) must be centered around Vcent_CA(pin mid)
3. Rx differential CA to CK jitter total timing window at the VciVW voltage levels
4. Defined over the CA internal VREF range. The Rx mask at the pin must be within the internal VREF CA range irrespective of the input signal common mode
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid)
6. Input slew rate over VciVW Mask centered at Vcent_CA(pin mid)
7. VIHL_AC does not have to be met when no transitions are occurring
8. UI=tCK(avg)min



CA VIHL_AC definition (for each input pulse)

Differential Input Levels

Symbol	Parameter	Value	Unit	Note
$V_{IHdiff}CK$	Differential input high measurement level (CK, CK#)	0.75 x $V_{diffpk-pk}$	V	1,2
$V_{ILdiff}CK$	Differential input low measurement level (CK, CK#)	0.25 x $V_{diffpk-pk}$	V	1,2
$V_{IHdiff}DQS$	Differential input high measurement level (DQS, DQS#)	0.75 x $V_{diffpk-pk}$	V	1,2
$V_{ILdiff}DQS$	Differential input low measurement level (DQS, DQS#)	0.25 x $V_{diffpk-pk}$	V	1,2

NOTE:

1. Vdiffpk-pk is the mean high voltage minus the mean low voltage over TBD samples
2. All parameters are defined over the entire clock common mode range

Single-ended / Differential Output Levels

Symbol	Parameter	Value	Unit	Note
V_{OH}	Output high measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
V_{OL}	Output low measurement level (for output SR)	0.25 x V_{pk-pk}	V	1
V_{OHdiff}	Differential output high measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	2
V_{OLdiff}	Differential output low measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	2

NOTE:

1. V pk-pk is the mean high voltage minus the mean low voltage over TBD samples
2. Vdiff pk-pk is the mean high voltage minus the mean low voltage over TBD samples

INPUT/OUTPUT CAPACITANCE

Symbol	Parameter	D4 (DDR5-4800)		Unit	Note
		Min	Max		
C_{IO}	Input/output capacitance	0.45	0.9	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS and DQS#	-	0.4	pF	1,2,3,5
C_{CK}	Input capacitance, CK and CK#	0.2	0.6	pF	1,3
C_{DCK}	Input capacitance delta CK and CK#	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL & ADD pins only)	0.2	0.6	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	pF	1,3,7,8
C_{DI_ADD}	Input capacitance delta (All ADD pins only)	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.4	1.5	pF	1,3
$C_{Loopback}$	Input/output capacitance of Loopback	0.3	1.0	pF	1,2,3
C_{TEN}	Input capacitance of TEN	0.2	2.3	pF	1,3,12

NOTE:

1. This parameter is not subject to production test. This parameter is measured by using vendor specific measurement methodology.It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VPP applied with all other signal pins floating. Measurement procedure TBD
2. DQ, DM#, DQS, DQS#, TDQS, TDQS#, LBDQ and LBDQS. Although the DM#, TDQS, TDQS#, LBDQ and LBDQS pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK-CK#
5. Absolute value of CIO(DQS)-CIO(DQS#)
6. CI applies to CS# and CA[13:0]
7. CDI CTRL applies to CS#
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CK)+CI(CK#))
9. CDI_ADD_ CMD applies to CA[13:0]
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CK)+CI(CK#))
11. CDIO = CIO(DQ,DM)-Avg(CIO(DQ,DM))
12. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information

IDD & IPP SPECIFICATIONS

Parameter	Symbol	D4 (DDR5-4800)	Unit
		IDD Max	
		VDD 1.1V, VDDQ 1.1V, VPP 1.8V	
Operating One Bank Active-Precharge Current / IPP Current	IDD0	332.2	mA
Operating Four Bank Active-Precharge Current / IPP Current	IDD0F	365.2	mA
Precharge Standby Current / IPP Current	IDD2N	250.8	mA
Precharge Power-Down Current / IPP Current	IDD2P	191.4	mA
Precharge Standby Non-Target Command Current / IPP Current	IDD2NT	244.2	mA
Active Standby Current / IPP Current	IDD3N	268.4	mA
Active Power-Down Current / IPP Current	IDD3P	200	mA
Operating Burst Read Current / IPP Current	IDD4R	787.6	mA
Operating Burst Write Current / IPP Current	IDD4W	930.6	mA
Burst Refresh Current (Normal Refresh Mode) / IPP Current	IDD5B	578.6	mA
Burst Refresh Current (Fine Granularity Refresh Mode) / IPP Current	IDD5F	563.2	mA
Burst Refresh Current (Same Bank Refresh Mode) / IPP Current	IDD5C	354.2	mA
Self Refresh Current: Normal Temperature Range / IPP Current	IDD6N	94.6	mA
Operating Bank Interleave Read Current / IPP Current	IDD7	1170.4	mA
Maximum Power Saving Deep Power Down Current / IPP Current	IDD8	68.2	mA
Note: IDD specification is based on Samsung DDR5 16Gb 2Gx8 B-die components.			

TIMING PARAMETERS

Timing Parameters by Speed Bin

Parameter	Symbol	D4 (DDR5-4800)		Unit	Note
		Min	Max		
Clock Timing					
Average Clock Period	tCK(avg)	0.416	-	ns	1
Command and Address Timing					
Read to Read command delay for same bank in same bank group	tCCD_L	Max(8nCK, 5ns)		nCK,ns	8
Write to Write command delay for same bank in same bank group	tCCD_L_WR	Max(32nCK, 20ns)		nCK,ns	8
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	Max(16nCK, 10ns)		nCK,ns	8
Read to Write command delay for same bank group	tC- CD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6,8
Write to Read command delay for same bank in same bank group	tCCD_L_ WTR	CWL + WBL/2 + Max(16nCK,10ns)		nCK,ns	4,6,8
Read to Read command delay for differ- ent bank in same bank group	tCCD_M	tCCD_L		nCK,ns	8
Write to Write command delay for differ- ent bank in same bank group	tCCD_M_WR	tCCD_L_WR		nCK,ns	8
Write to Read command delay for differ- ent bank in same bank group	tC- CD_M_WTR	tCCD_L_WTR		nCK,ns	4,6,8
Read to Read command delay for differ- ent bank group	tCCD_S	8		nCK	8
Write to Write command delay for differ- ent bank group	tCCD_S_WR	8		nCK	8
Read to Write command delay for differ- ent bank group	tC- CD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE		nCK,ns	3,5,6,8
Write to Read command delay for differ- ent bank group	tCCD_S_ WTR	CWL + WBL/2 + Max(4nCK,2.5ns)		nCK,ns	4,6,8
Write to Read with Auto Precharge com- mand delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP		nCK,ns	2,4,6,8
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(8nCK, 5ns)		nCK,ns	8
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(8nCK, 5ns)		nCK,ns	8
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8		nCK	8
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8		nCK	8
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 13.333ns)	-	nCK, ns	8
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 16.666ns)	-	nCK, ns	7,8
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)		nCK,ns	8
Precharge to Precharge command de- lay	tPPD	2		nCK	8
Write recovery time	tWR	30		ns	8

NOTE:

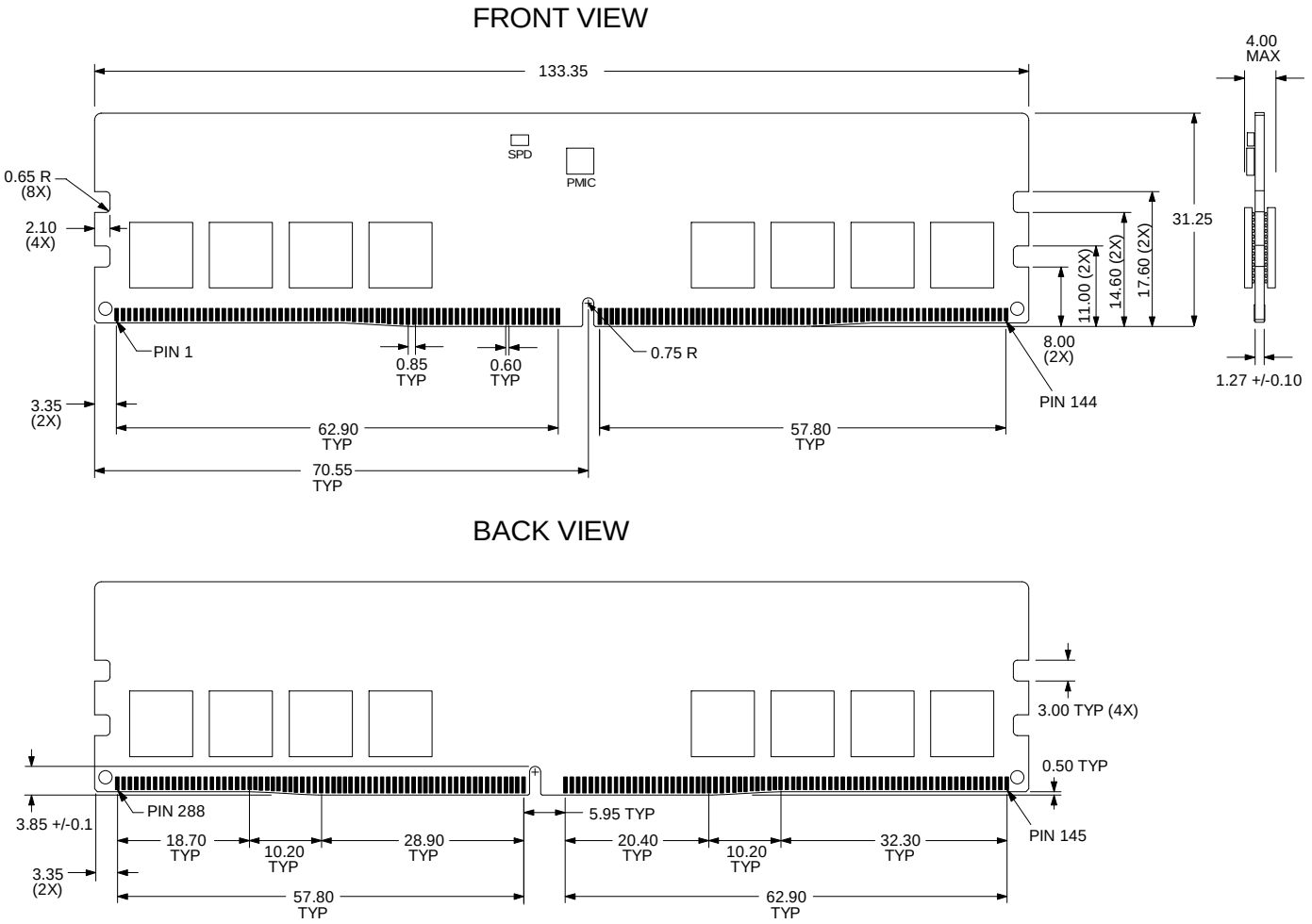
1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.
2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms, nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).
3. RBL: Read burst length associated with Read command.
   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode. RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode.
   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
4. WBL: Write burst length associated with Write command.
   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode.
   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode.
   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode.
5. The following is considered for tRTW equation. 1tCK needs to be added due to tDQS2CK. Read DQS offset timing can pull in the tRTW timing. 1tCK needs to be added when 1.5tCK postamble.
6. CWL=CL-2.
7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb).
8. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.

DDR5 Function Matrix

DDR5 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Functions	Supported
Write Leveling	YES
Temperature controlled Refresh	YES
Fine Granularity Refresh	YES
Same Bank Refresh	YES
Refresh for Management	NO
Data Mask	YES
Command Address Inversion	YES
TDQS	YES
ZQ calibration	YES
DQ Vref Training	YES
Per DRAM Addressability	YES
Mode Register Readout	YES
WRITE CRC	YES
READ CRC	YES
CA Parity	YES
Programmable Preamble/Postamble	YES
Maximum Power Saving Mode	YES
Connectivity Test Mode	YES
Bit Error Rate Test	YES
Package Output Driver Test Mode	YES
3DS	NO
CA Training Mode	YES
CS Training Mode	YES
DQS interval Oscillator	YES
ECC Transparency and Error Scrub	YES
Lookback	YES
Duty Cycle Adjuster	YES

Package Dimensions



Notes: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.