ENT-AN1280
User Guide
VSC8257/VSC8258 Evaluation Board

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Contents

1 Revision History 1
1.1 Revision 1.3 1
1.2 Revision 1.2 1
1.3 Revision 1.1 1
1.4 Revision 1.0 1
2 VSC8257/VSC8258 Evaluation Board 2
2.1 References 2
3 Quick Start 3
4 Hardware Options 4
4.1 Power Supply Options 4
4.2 Reference Clock Options 4
5 Software 5
5.1 USBXpress® Driver Installation 5
5.2 GUI Setup 5
5.3 Main Page 6
5.4 Routing 7
5.5 BIST 8
5.6 SFP+ 9
5.7 Register List 9
5.8 RMON 10
5.9 KR Status 10
5.10 I/O Control 11
5.11 Clocking 11
5.12 Command Line Interface 12
6 Usage Examples 14
6.1 Packet BIST 14
6.2 PRBS31 BER 14

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Revision 1.3 was published in September 2018. There were no changes to the technical content.

1.2 Revision 1.2

Revision 1.2 was published in October 2016. The latest GUI interface was added.

1.3 Revision 1.1

Revision 1.1 was published in October 2015. The improved interface was added.

1.4 Revision 1.0

Revision 1.0 was published in June 2014. It was the first publication of this document.

2 VSC8257/VSC8258 Evaluation Board

Supporting 1000BASE-X, 10GBASE-R, 10GBASE-W, and other protocols, the VSC8258 is a quad serial Ethernet PHY with IEEE 1588-2008 and media access control security (MACsec) support. The VSC8257 is a quad serial Ethernet PHY with IEEE 1588-2008 support. MACsec functions are permanently disabled in a VSC8257 product.

There are four bidirectional ports (interchangeably called channel), each consisting of an Rx path (ingress) and a Tx path (egress). The Rx path receives serial data from the line side (RXIN), de-serializes it to 64-bit bus to the processing core, then serializes it back to the appropriate serial stream at the host side (RXOUT). The Tx path receives a serial stream from the host side (TXIN), de-serializes it to 64-bit bus to the processing core, then serializes it back at the line side (TXOUT).

A GUI is provided for the user to control the evaluation board from a PC using a USB cable. The GUI allows the user to configure devices, access registers, and run scripts. The GUI may be used without an evaluation board in a demonstration mode to provide an introduction to the device features.

The default configuration of the evaluation board allows the user to easily connect it to lab equipment such as a high-speed oscilloscope, bit error rate tester, or protocol analyzer (IXIA, Spirent, and so on) through SMA cables or fiber.

An external 5 V power supply is required to power to the evaluation board, shown as follows. On-board voltage regulators are used to supply the 1.0 V, 1.2 V, and 2.5 V power rails for the device.

Figure 1 • VSC8258 Evaluation Board

The following sections detail the evaluation board configuration and the features of the hardware and software associated with the board. While VSC8258EV is used throughout this document, the VSC8257EV will behave similarly.

2.1 References

The following documents provide more information on the device and evaluation board.

- VSC8258 datasheet
- VSC8258 evaluation board schematics

3 Quick Start

The following items are recommended for use during evaluation of the evaluation board.

- VSC8257/8258 evaluation board (included in the kit)
- USB cable (included in the kit)
- GUI installation file (available on the website)
- SR/LR SFP+ module (not included)
- Fiber patch cable (not included)
- Pattern generator or protocol tester
- Oscilloscope
- Personal computer running Windows XP or 7

The following steps allow a user to bring up the VSC8258EV, receive traffic from a tester, loop traffic internal to the device, and transmit back to the tester.

1. Provide 5 V power supply to the evaluation board.
2. Connect the USB cable to the evaluation board (J34) and to a PC.
3. Insert a 10G module into P1 (channel 2).
4. Connect the optical patch cable to the module and to the 10G tester.
5. Install the USB driver as described in section USBXpress® Driver Installation.
6. Install the GUI software as described in section GUI Setup.
7. Launch the GUI.
8. From the EVB connection window, select the matching board serial number and click **Launch GUI**.
9. The clock is pre-configured at 156.25 MHz.
10. On the main page, click the **10G LAN Mode** option. This will initialize the device. Due to the speed of the microcontroller and USB interface, this operation may take a minute. During initialization, the bottom status bar will indicate initialization in progress. When completed, the text will change to indicate so. Closing the GUI and re-launching without power cycling the board or pressing the reset button will retain the previously initialized mode.
11. After initialization, the respective line- or host-side Rx and Tx PLL status will show a green state. The 10G protocol tester should also indicate a link-up condition. Because there is no valid data present at the XAUI receiver, end-to-end traffic will not flow.
12. On the Routing tab, enable Loopback L3 for channel 0 (R)XAUI Rx. The 10G tester should now see valid packets at its receiver.

4 Hardware Options

The following sections describe the hardware options.

4.1 Power Supply Options

The evaluation board can also be powered by an external 5 V power supply. Use a pair of banana cables to connect a bench-style power supply capable of 4 A at 5 V to the board. Connect 5 V to J45 and GND to J46.

4.2 Reference Clock Options

The evaluation board is preconfigured with a clock frequency of 156.25 MHz.

5 Software

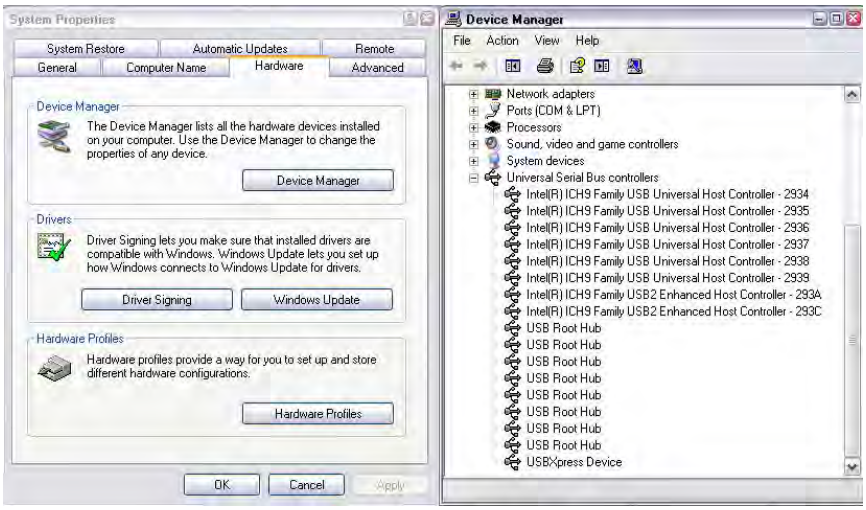
Although the device's internal registers can be accessed through three different interfaces—MDIO, two-wire serial, or SPI—the software makes use of the SPI port. On the evaluation board, a F340 microcontroller acts as the SPI master that controls the PHY. The PC communicates with the microcontroller through a USB connection.

5.1 USBXpress® Driver Installation

First, the USBXpress development kit needs to be downloaded from the Silicon Labs website. Follow the installation directions after downloading the development kit.

Once the USBXpress driver is installed, connect the USB cable to the evaluation board and the PC. In order to double check that the USBXpress driver is installed and recognizing the evaluation board, go to the Control Panel, and click on **System** > **Hardware** > **Device Manager**. Inspect the Universal Serial Bus controllers listed to see if "USBXpress Device" appears. The following image shows that the PC has recognized a connected USBXpress device.

Figure 2 • USBXpress in PC's Device Manager



5.2 GUI Setup

Run the setup file to install the GUI. Once installed, the user should launch the GUI, which will bring up the initial window shown in the following image.

Figure 3 • Evaluation Board Selection Window

The GUI will detect the serial number of the connected evaluation board(s). If there are multiple boards connected on the same PC, click on the drop down menu, and select the desired evaluation board serial number. The two status lights will turn green when the F340 microcontroller is detected and the appropriate device is present. Click **Launch GUI**.

If the device indicator (for example, “VSC8258 Present”) does not turn green, check the voltage rails with a multimeter to ensure the VDD rails reached the proper levels, thus ruling out current limiting as the cause. Also, check the SiUSBXp.dll file in the same directory as the MalibuGUI.exe resides to ensure the version of it matches to the version of the USBExpress driver installed. In the same directory, one can file SiUSBXp_old33, SiUSBXp_new4000, SiUSBXp_new4040_32bit dll files. Determine which one of the three files match to the version of the installed USBExpress driver, and then rename that file to be SiUSBxp.dll.

5.3 Main Page

The following image shows the GUI main page.

Figure 4 • GUI Main Page

The serial number of the evaluation board appears on the left corner of the page along with the silicon revision, communication protocol used, and the port address. SPI is the communication protocol used and Channel 0’s default port address is 00.

The Mode Initialization box allows the user to initialize the 10G LAN mode. During device initialization, which may take upwards of 4 minutes due to the microcontroller limitations, the “INITIALIZING” message will appear in the lower corner of the window. When completed, a message dialogue box will pop up.

When the communication is successfully established, it should say “CONNECTED” at the bottom left corner of the main page.

The dashboard on the left contains the Status and BER tabs.

The Status box shows the Host and line side PLL status per channel for the receiver and transmit sides. The LED illuminates green when the appropriate PLL is activated.

The following image shows the PRBS31 pattern generator and checker.

Figure 5 • GUI Main Page—PRBS31

Click **Start Generator** and **Start Checker** to start the BIST. This begins the synchronization and error checking on the selected channel, along with a timer. The cumulative number of bit errors and the cumulative bit error rate are displayed.

Stop Checker will stop the timer and polling of the error count. This will retain the last values. While enabled, the error count register polling is not interrupted when any other page/tab is viewed.

Every channel has its own generator and checker, which allows two or more channels to be started at the same time.

5.4 Routing

As shown, the routing page provides various options available for routing traffic between the host side and the line side. A data path diagram of the loopbacks is displayed on the top of this page.

Figure 6 • GUI Routing Page

There are seven loopbacks available. Three of the loopbacks are host-side loopbacks. These include loopback H2, loopback H3, and loopback H4. Loopback H2 is the shallow loopback located in the XAUI-PHY block before the 8b/10b endec. The deeper loopback includes loopback H3 in the PCS block right after the
64b/66b gearbox and loopback H4 at the WIS block after the framer.

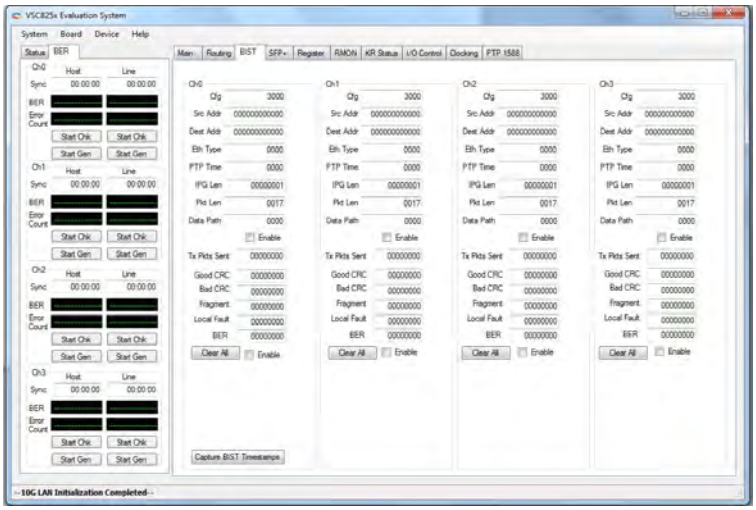
The other three loopbacks are line-side loopbacks (that is, SFI in and looped back to SFI out). This includes loopback L3, loopback L2C, loopback L2, and loopback L1. Loopback L3 is the loopback at the PMA block while loopback L2 is the loopback right before the data hits the XGXS block. The deepest loopback, L1, is the loopback after the 8b/10b endec. When using loopback L1 with an external 10G tester, the entire chip is exercised with the exception of the XAUI input and output buffers.

The GUI allows the user to turn on host- and line-side loopbacks for 10G LAN and 1G LAN modes. Checking the box enables the loopback while un-checking disables it.

5.5 BIST

The following image shows the BIST page.

Figure 7 • GUI BIST Page



The BIST page is not for PRBS BIST, but for packet-based BIST. There is a packet BIST engine on each channel. The DA, SA, type, PTP time, packet length, IPG length, and the data could be configured. The CFG, configuration register, and the data path registers are also programmable. The definition of CFG register is listed in table Generator Configuration (GEN_CFG), Address: 4xE900. The data path register is reserved for factory use. The current GUI only supports BIST sending data at PMA output and receiving data from PMA input.

On the checker side, there are counters for the good packets, CRC error, fragmentation error, and local fault.

The generator and checker can be individually enabled for each channel. The BIST on the right column is a packet bist engine. When enabled, the DUT will be sending packetized PRB31 traffic out at PMA output and receiving packetized traffic in at PMA input.

Note: After inputting the value to the corresponding box, make sure a return is hit, or the input value may not take effect. Also, the settings may not reflect the updated values until the user exits this page and then returns to it.

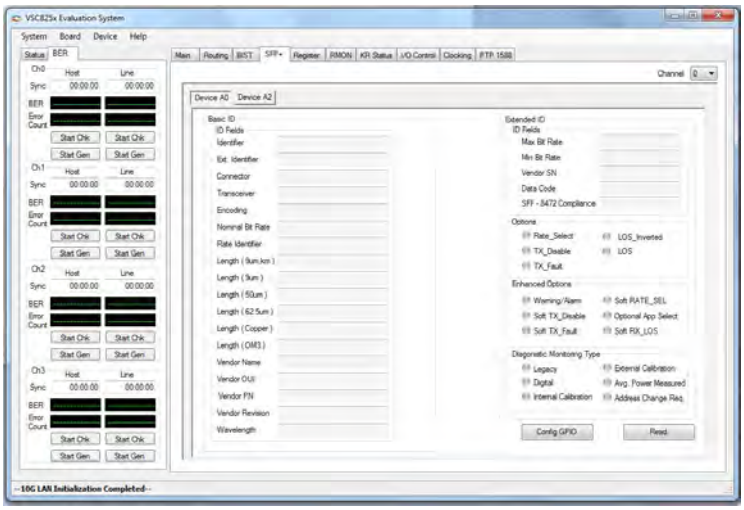
Table 1 • Generator Configuration (GEN_CFG), Address: 4xE900

Bit	Name	Access	Description	Default
14:12	LENOFS	R/W	Decrease pktlen by lenofs	0x3
11:4	SRATE	R/W	Number of standard frames between PTP frames	0x00
2	IDLES	R/W	Generate all idles 0: Generate frames 1: Generate idles only	0x0
1	PTP_ENABLE	R/W	Generate PTP frames 0: Generate standard frames 1: Generate PTP frames	0x0
0	ENABLE	R/W	Enable packet generator 0: Generator is disabled 1: Generator is enabled **Note:** Pattern generator data cannot simultaneously be inserted in the egress and ingress data paths. Insertion of pattern generator data into the paths is controlled by 4xEA20.7 and 4xEA20.8. **Note:** There are additional restrictions in using this bit for 1G mode. Please consult the factory.	0x0

5.6 SFP+

The information of the SFP+ module registers could be read through the GPIOs of the VSC8258 that are configured as I2C master to interface with the I2C registers of the SFP+, as shown.

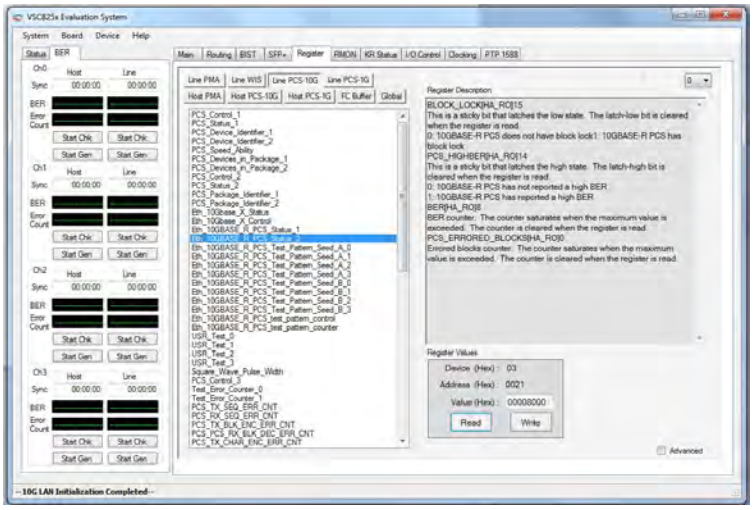
Figure 8 • GUI SFP+ Page



5.7 Register List

The following image shows the register list page.

Figure 9 • GUI Register List Page



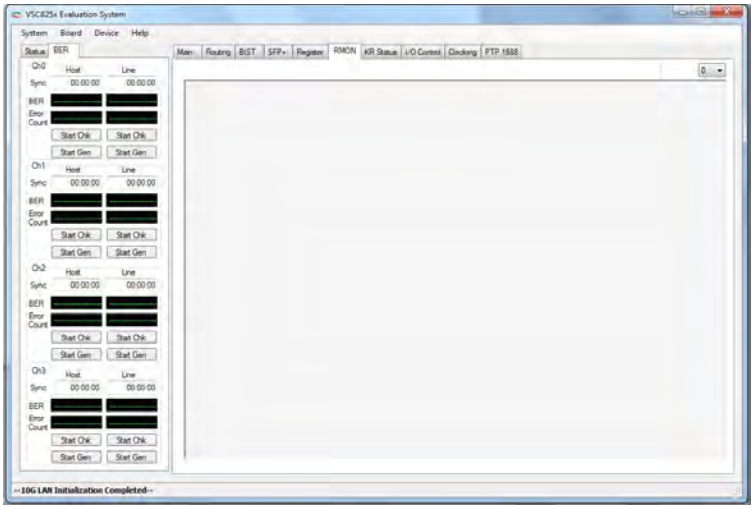
The Register List page provides read and write access to device registers. They are grouped into nine tabs. To select a register, click on the name in the list. The register's description, address, read/write capability, and current value are displayed. To write to a device register, highlight the desired register, enter the hexadecimal value in the "Value (Hex)" box, and click **Write**. Clicking **Read** will read the same register, showing the register's new contents.

There is an advanced mode where, when enabled, users can jump to any device and any register offset by typing in the corresponding values without going through the specific register tab.

5.8 RMON

The RMON page, shown as follows, is not available in current GUI.

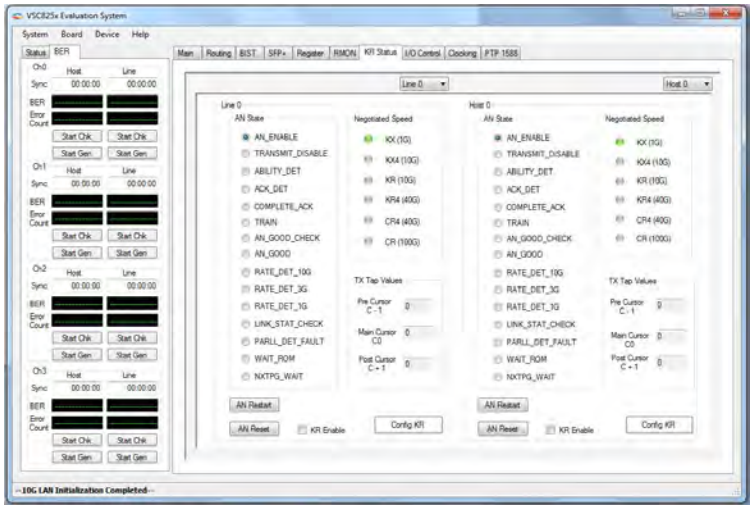
Figure 10 • GUI RMON Page



5.9 KR Status

The following image shows the pull-down menu for KR status.

Figure 11 • GUI KR Status Page

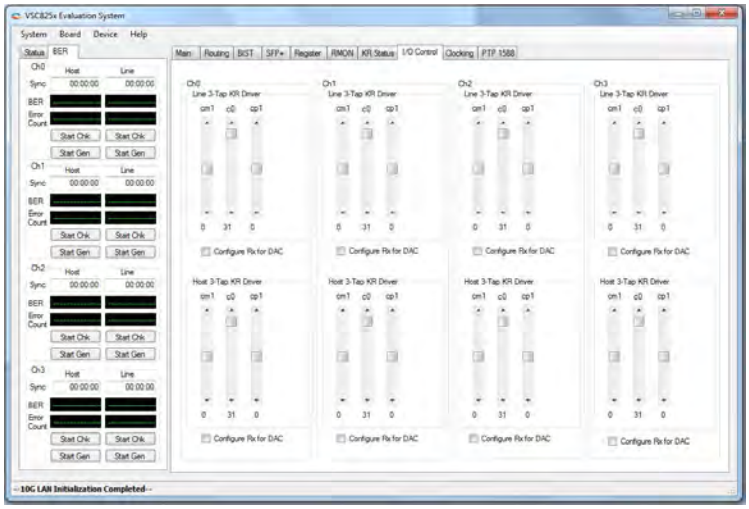


When the line side is connected to a link partner through a backplane, the KR mode could be enabled by clicking on **config KR** first and then **KR enable**. The user will see the green light move and it should eventually reside at AN_GOOD state and indicate KR (10G) is negotiated. The values of the resulted C-1, C0, and C+1 will also be updated at the Tx Tap Values box.

5.10 I/O Control

The following image shows the I/O control page.

Figure 12 • GUI I/O Control Page

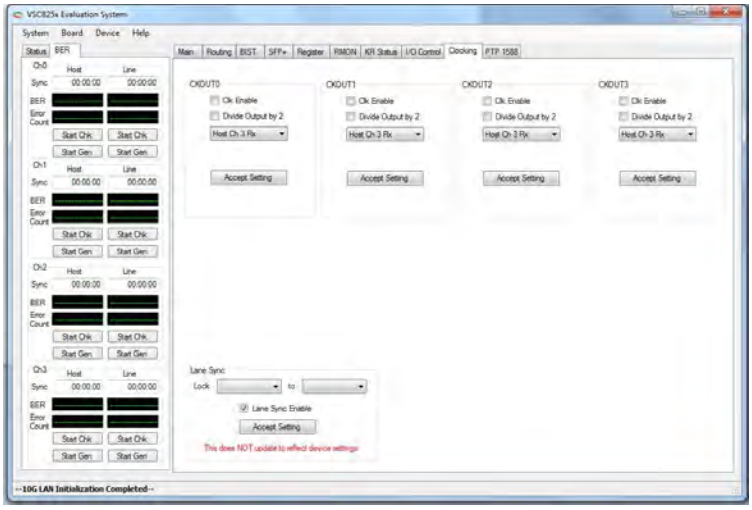


On this page, the user can adjust the pre-cursor, main cursor, and post-cursor of the transmitter of each lane. On the receiver side, the default mode is for SR/LR/ER. To have the mode support DAC, the user can enable it by clicking on **Configure for Rx DAC**. The summation of the Cm1, C0, and Cp1 must not exceed 31 and the user has to maintain this restriction.

5.11 Clocking

The following image shows the clocking page.

Figure 13 • GUI Clocking Page



In this page, there are actually two main categories: the source for the output clocks and the source for the lane sync feature.

For the output clocks, CKOUTn, the user can first enable that output and then select if the output clock frequency should be divided by 1 or by 2. When it is divided by 2, the result is a 161 MHz clock output derived from the selected source. When it is divided by 1, then the frequency will be 322 MHz. The selection of the clock source include the host/line side CMU divided down clock or the host/line-side recovered clock from data.

For the lane sync feature, the user can select the Tx clock of each channel (line or host) to be lane synced (locked) to the local reference clock or the Rx clock of the same channel or the Rx clock from other channels.

Note: When cross-connect is enabled, the Tx clocks of all host channels must be lane synced to the local reference clock.

5.12 Command Line Interface

Clicking on **Board** > **Vitesse CLI** from the toolbar opens the command line interface (CLI) window. From here, users can load initialization files or other scripts. When the **Load Macro** button is clicked, another window will appear allowing the user to select the script.

The following example describes WS_P03_81_ae_00_00_00_02_00 where WS is SPI command**:**

P03 is the port of the F340 processor used for the SPI
Bit 55 = 1 is write and = 0 is read
Bit 54:53 is the port/channel number: it is port 0
Bit 52:48 is device number: it is 0x1
Bit 47:32 is the register address: it is 0xAE00
Bit 31:0 is the value for the register: it is 0x000000200

The following images show the command line interface.

Figure 14 • Command Line Interface I

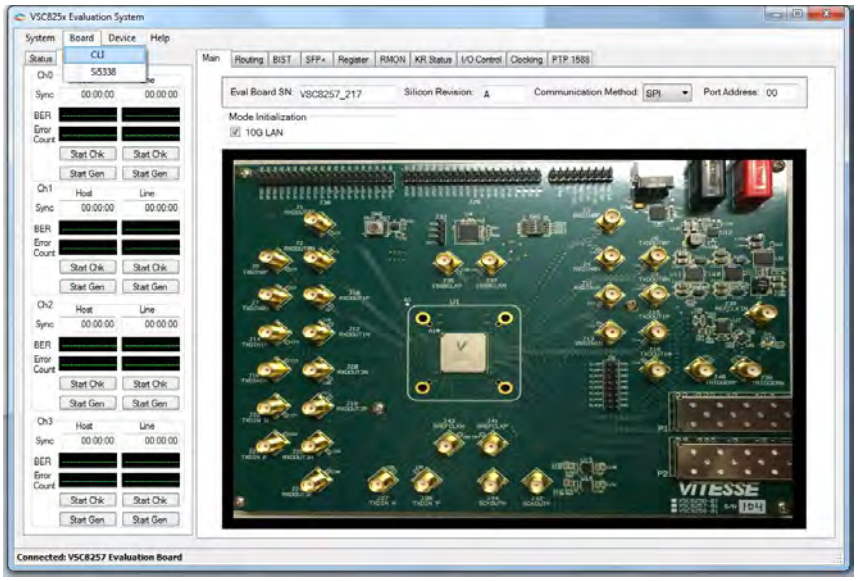
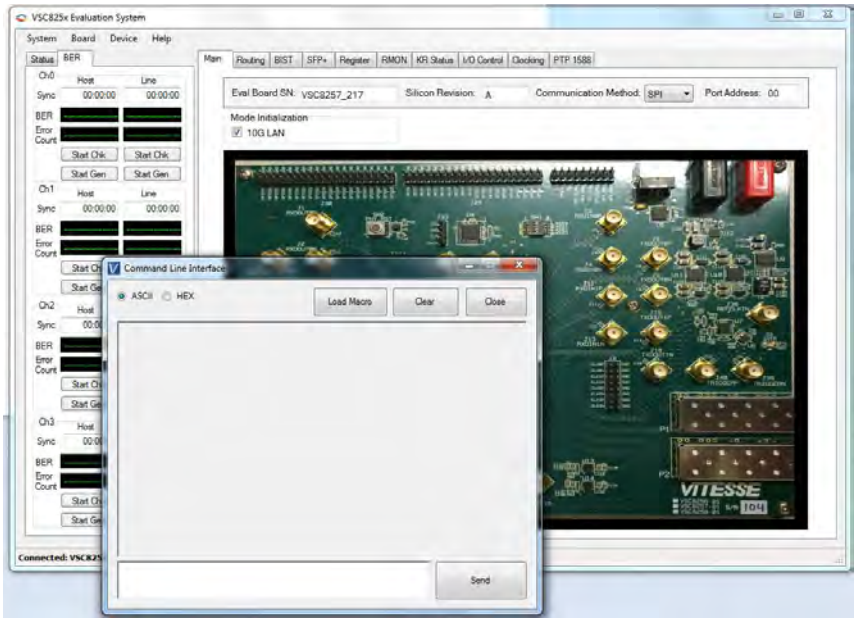


Figure 15 • Command Line Interface II



6 Usage Examples

The following sections describe usage examples.

6.1 Packet BIST

Go to the BIST page. Check the **Enable** box above Tx Packets sent to display the Tx packet sent. Then, check the **Enable** box under the BER to enable the packet BIST checker. The count of valid packets will be seen in the box for Good CRC and there are also counters for Bad CRC, Fragmentation, and Local Fault. The configuration registers might not get updated until the user leaves and then returns to this page.

6.2 PRBS31 BER

The PRBS31 BER resides on the BER page on the right column of the GUI display.

1. On the BER page click **Start Generator** and **Start Checker** to exercise the PRBS31 BER. Starting the checker will start the timer and show the current error count and bit error rate. The value of Error Count and BER is continuous and updated once every second. Click **Stop Checker** to stop the timer. The display will retain the last error count and BER.
2. Clicking **Start Checker** again will clear the error counts and restart the polling and calculation.
3. The 1-second polling will continue even if the user moves to other pages or tabs.