VSC8584
User Guide
VSC8584 Evaluation Board

Microsemi

a **Microchip** company

Contents

1   Revision History

The revision history describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1   Revision 1.0

Revision 1.0 of this datasheet was published in January 2014. This was the first publication of the document.

2 Introduction

The VSC8584 device is a low-power, quad-port Gigabit Ethernet transceiver with four SerDes interfaces for quad-port dual media capability. It also includes an integrated quad port I2C multiplexer (MUX) to control SFPs or PoE modules. The VSC8584 supports IEEE 802.1AE 128/256-bit MACsec protocols to meet the security requirements for protecting data traversing Ethernet LANs, and also includes Vitesse's patent-pending distributed timing technology VeriTime™ that delivers the industry's most accurate IEEE 1588v2 timing implementation. The VSC8584 device offers a seamless integration between IEEE 1588v2 and the MACsec engine with no loss of precision. The VSC8584 also supports a ring resiliency feature that allows a 1000BASE-T connected PHY port to switch between master and slave timing without having to interrupt the 1000BASE-T link.

This document describes the architecture and usage of the VSC8584 Evaluation Board (VSC8584EV). The VSC8584EV may be used to evaluate a family of devices which include VSC8584. These devices vary with respect to the number of ports, supported interfaces, and available features. This document specifically addresses the VSC8584 device. The Quick Start section describes how to bring-up the evaluation board along with install and run the graphical user interface (GUI), used to control the evaluation board.

Figure 1 • VSC8584EV Evaluation Board
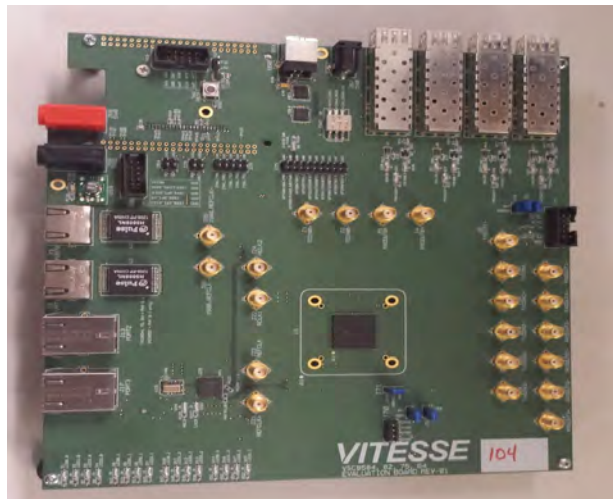
The following reference documents provide additional information about the operation of the VSC8584 evaluation board.

- VSC8564 Datasheet (https://www.vitesse.com/products/product.php?number=VSC8564)
- VSC8582 Datasheet (https://www.vitesse.com/products/product.php?number=VSC8582)
- VSC8575 Datasheet (https://www.vitesse.com/products/product.php?number=VSC8575)
- VSC8584 Datasheet (https://www.vitesse.com/products/product.php?number=VSC8584)
- IEEE1588v2 and SyncE – Applications and Operation Using Vitesse's Synchronization Solution (http://www.vitesse.com/products/download.php?fid=4767&number=VSC8574)
- VSC8584 GUI (https://www.vitesse.com/products/product.php?number=VSC8584)

3   General Description

The evaluation board in Figure 1 provides the user a way to evaluate the VSC8584 device in multiple configurations. Four RJ-45 connectors are provided for copper media interfaces. The four SFP cages allow for evaluation of the fiber media interconnects. The MAC interface is provided via SMA connectors.

For access to all of the features of the device, an external microcontroller is used to configure the on-board clock chip via a two-wire serial bus and the VSC8584 via the MDIO bus. The graphical user interface (GUI) enables the user to access the registers.

The evaluation board uses a Zarlink device to synthesize a 125 MHz reference clock signal from a 20 MHz crystal which serves as the REFCLK input.

3.1   Key Features

3.1.1   Copper Port RJ45 Connections

PHY Ports 2 and 3 use UDE RTA 1648BAK1A with integrated magnetic while PHY Ports 0 and 1 use generic RJ45 connectors with discrete Pulse H5008 magnetics.
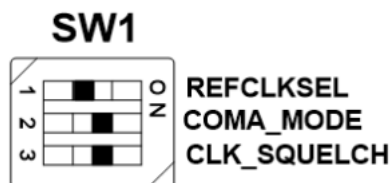
3.1.2   SGMII/QSGMII MAC SMA

SGMII SMA connections are provided for all PHYs while the QSGMII SMA connection is available only on PHY0.

3.1.3   Switch Block Control

Set the SW1 switch as shown in the figure below.

Figure 2 • SW1 Switch Control

3.1.4   Zarlink ZL30343 SyncE G.8262/SETS

The Zarlink ZL30343 is initialized by default to provide a 125 MHz differential LVPECL clock to VSC8584 REFCLK inputs. (Note: the ZL30343 can be programmed to provide LVDS differential clock in conjunction with an LVDS termination provided for REFCLK, please refer to the Zarlink manual for programming its output drive).

Also, the ZL30343 can support synchronization with the VSC8584 PHY recovered clock for SyncE operation. The ZL30343 is initialized to lock a recovered clock output if one is enabled and available from the VSC8584 PHY. If no recovered clock signal is available, then the ZL30343 will select the crystal oscillator (U16) as default reference source for holdover operation. ZL30343 will indicate locked versus holdover status by driving LED D33 or D34. See the Zarlink documentation for more discussion concerning its operation. See the VSC8584 datasheet for configuring recovered clock output pin behavior.

Please ensure three-way resistive connections R19 and R22 are appropriately connected to feedback the VSC8584's recovered clock outputs into the ZL30343 device, if synchronization to a recovered clock source is desired.

3.1.5   External 1588 Clock Option

The user may choose to provide an external 1588 REFCLK via SMA connections to J65 and J66. Zero ohm jumpers may need to be removed and or installed to connect via these clock inputs. The board is built with connections for external 1588 REFCLK, unless otherwise indicated in documentation accompanying the specific board delivered.

3.1.6   External RefClk Option

The user may choose to provide an external PHY REFCLK via SMA connections to J21 and J23. Zero ohm jumpers may need to be removed and or installed to connect via these clock inputs. As per section 2.1.4, and unless otherwise indicated in documentation accompanying the specific board, the board is built with a REFCLK connection driven by the ZL30343, instead of using an external REFCLK source.

### 3.1.7   1588 Daisy-Chain SPI Time-Stamping Connection

The VSC8584 device enables daisy-chaining multiple devices to reduce the number of pins required to transmit time stamping information to system ASICs gathering IEEE 1588 time stamps. For users with two or more 8584EV boards, the following single-ended connections shown below are required from the master device to slave device:

- J75 pin 6 to J77 pin 6 (1588_SPI_CLK output → input)
- J75 pin 4 to J77 pin 4 (1588_SPI_CS ouput → input)
- J75 pin 2 to J77 pin 2 (1588_SPI_MISO output → 1588_SPI_MOSI input)

See section 3.5.4 for register programming to enable this interface.

Recommendation: for SPI daisy chaining use a Molex 10 pin ribbon cable with one-to-one connections

Figure 3 • 1588 Daisy-Chain SPI Interconnect
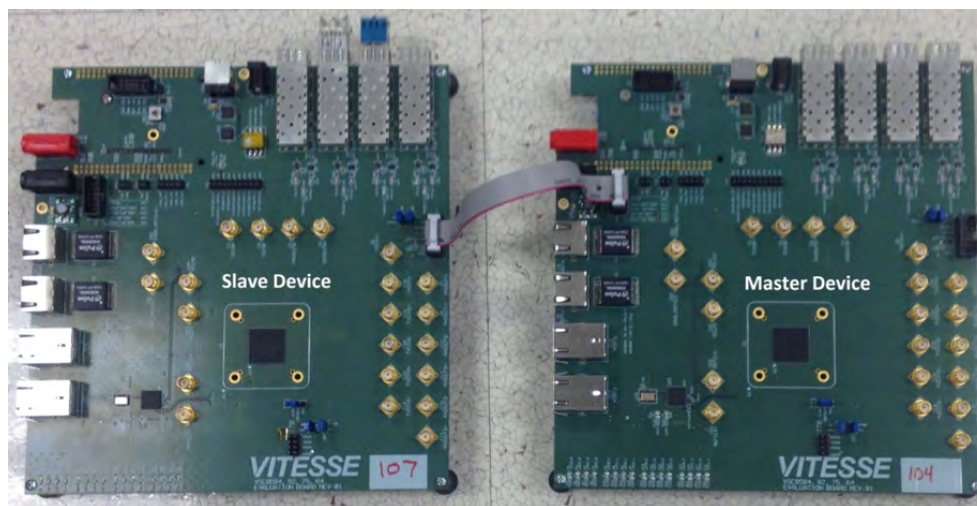
Once enabled along with proper initialization of the 1588 IP block, time-stamped 1588 traffic in the egress direction will generate a similar sequence on the serialized timestamp daisy-chain as shown in the following illustration. See the VSC8584 datasheet section about Serial Time Stamp Output Internface for a more detailed functional description.

Figure 4 • 1588 Daisy-Chain SPI Traffic Pattern (PHY port 3 egress)
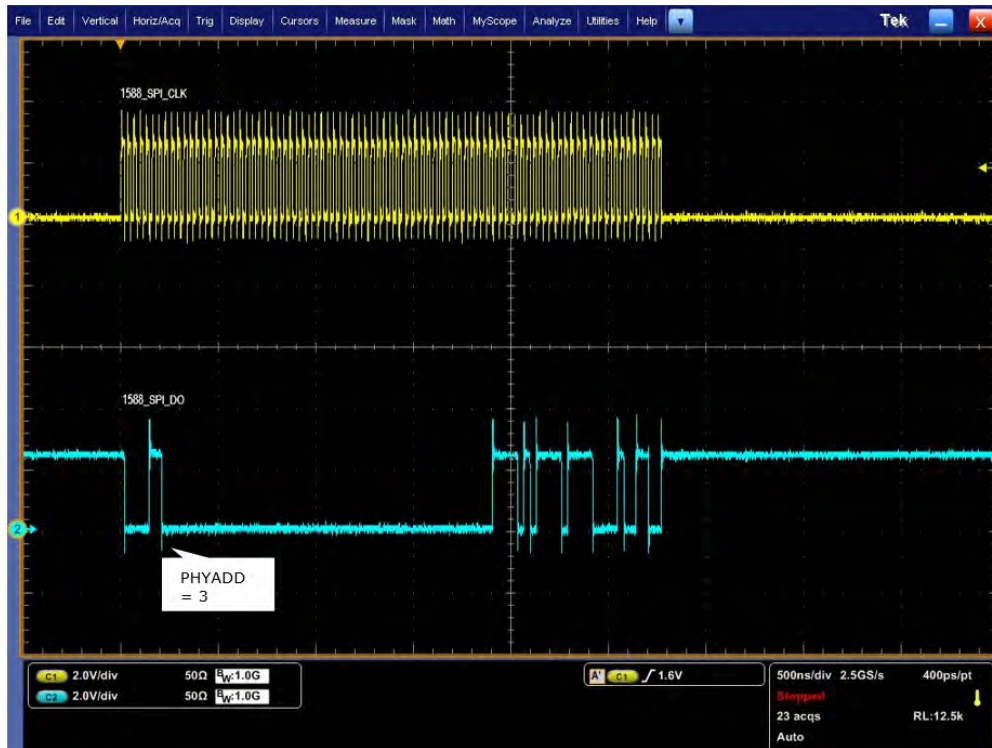
3.1.8   Network Interface Microcontroller Card

A "Rabbit" microcontroller card is included to facilitate a software interface to the registers on the VSC8584. The controller card has a hard coded static IP address. Refer to the label on the card for the value. This address is required by the user to initiate communications via the board and the GUI.

Note: The factory programmed Rabbit board IP address is 10.9.70.193.

4 Quick Start

This section shows the quick start for the VSC8584.

4.1 Connecting the Power Supply

The evaluation board uses 5 VDC to power the on-board regulators creating the 3.3 V, 2.5 V, and 1.0 V rails which drive the devices as well as modules. The evaluation board can be powered up using the power pack which provides the 5 VDC. Simply plug the AC adaptor into a wall socket and the barrel end into J67 (see the upper right corner of Figure 1). Immediately the user should see several LEDs turn on.

4.2 PC Software Installation

1. Download the ZIP file to the PC's root directory, normally C:\.
2. Extract to C:\
3. Double-click the icon to launch the GUI (It is acceptable to drag the icon to the desktop)

4.3 Connecting to the Board to the PC

The Rabbit board can interface with a PC either through a direct connection to the PC or if configured properly through a local area network. The latter option requires the user to configure the Rabbit's IP address so as to properly reside on the user's network.

The IP address of the board should be written on the Rabbit network interface daughter board card. The default value should be 10.9.70.193. Use this IP address to initially access the board for operation or to change its IP address.

4.3.1 Changing the IP Address of the Board

1. Determine and write down the new unique IP address you wish to change the board to.
2. Directly connect an Ethernet cable from a PC to the Rabbit board.
   NOTE: Some older PCs do not support auto-crossover on the Ethernet connection so a cross-over cable may be needed.
3. Launch a DOS command window by clicking on the Start->Run button and typing "cmd".
4. Within the DOS command window type "Telnet."
5. In Telnet, connect to the Rabbit board's address using the open command by typing "open^10.9.70. XXX".
6. 10.9.70.xxx where xxx is the value on your board from the factory (typically 193).
7. You should have a prompt and be able to type help to get a list of commands available on the Rabbit.
   a) If you are unable to connect, then most likely you will need to change the IP address of the connected PC to have the first 3 octets similar to the board by following the subsequent steps.
   b) On the PC under Windows -> Control Panel ->Network Connections -> Local Area Connection, right mouse-click for properties. Under the General tab highlight Internet Protocol (TCP/IP) and click on Properties. From there enter the new PC IP address such as 10.9.70.yyy where yyy is a unique value and NOT the same as the Rabbit board. Once complete, return to step 4.
8. Command the board to change its IP address to the new one by typing into Telnet now connected to the board the command: set ip <new IP address> <Enter> where <new IP address> is in the form xxx. xxx.xxx.xxx. Once you hit <Enter> the IP address will be changed and the Rabbit will save the value and reboot which may take approximately 1 minute. The Telnet session will disconnect from the board.
9. Change your PC IP address to the same IP network as the Rabbit board.
10. Telnet to the Rabbit board.
11. Use the following commands to complete configuration of the Rabbit board:
    a) set netmask xxx.xxx.xxx.xxx
    b) set gateway xxx.xxx.xxx.xxx
    c) save env
12. Please record and inform Microsemi of the new IP address of the board when you return so that Microsemi can connect to and reconfigure the board.
13. Re-label the Rabbit board with the new IP.

4.4   Using the Control Software

4.4.1   CAT5 to SGMII with Clause 37 AutoNeg Enabled

Connect the VSC8584EV Rabbit microcontroller RJ-45 directly to the PC or through a network switch if properly configured. Apply 5 VDC to the EVB.

Launch the GUI by double-clicking the GUI shortcut located in C:\ViperGUI_4_67 or on the desktop if it has been moved there. The GUI connection window shown in the following figure should appear.

Figure 5 • GUI Connection Window

To make a connection to the EVB, click "Rabbit" and enter the IP address of the EVB, then click on "Connect." The display next to the IP address window should change to "Connected." If it does not, check the IP address, or your network configuration until connection with the EVB can be successfully established.

Double-click on "MII Registers" and the window shown in Figure 6 should appear:

Figure 6 • MII Registers GUI Window
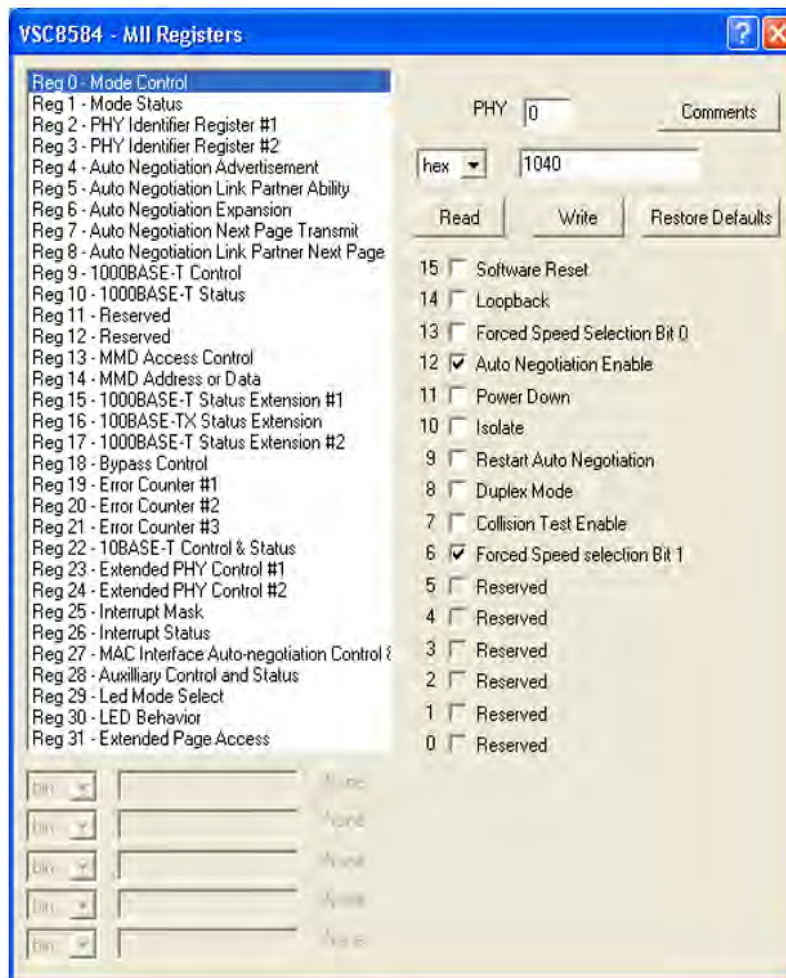
Be sure the device is up and running by reading MII Register 0. It should read back 0 × 1040. Reading back all 0's or all 1's indicates a problem. A checked box means the bit is set to "1," if unchecked it is "0."

4.4.2   Board Initialization and Running PGY Scripts

Once the evaluation board connectivity has been established and confirmed, the PHY should be initialized. Initialization can be accomplished by running an init-script sequence, such as performed by the pre- and post-reset functions of the PHY API standalone app.

While the init-script sequence may not required for specific operational modes, an init-script sequence is highly recommended to ensure correct performance over the greatest set of user scenarios for the PHY. After initialization is performed, refer to the PHY Datasheet section on Configuring of the PHY and PHY Interfaces for the desired application.

In order to execute an init-script, double-click on "Run PHY Script" within the GUI Connection Window to launch the Run PHY Script window as shown in Figure 7. This enables a user to load a script to configure the device rather than navigating through Registers pages. Click "Load" button, browse to a desired script file via the pop-up panel, finally click "Run" button. After execution is completed, you should see read-back values in decimal as shown in the following figure.

The script syntax is command, phy address (in decimal), register address (in decimal), and register content (in either hexadecimal or decimal).

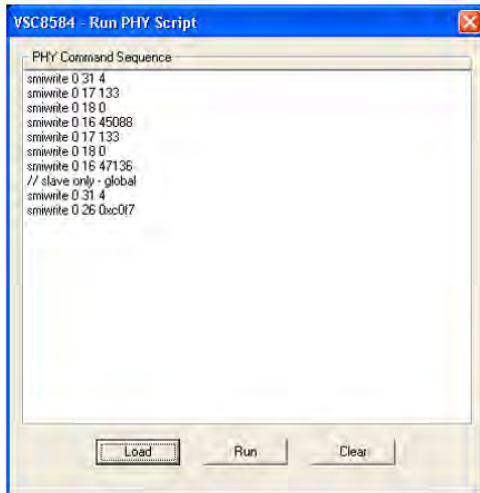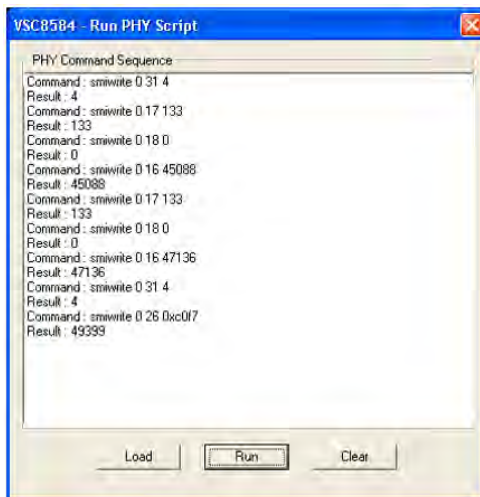**Figure 7 • Run PHY Script GUI Window (after script is loaded)**

Figure 8 • Run PHY Script GUI Window (after script is loaded)

4.4.3 Copper Media Operation (1000BASE-T)

A single register write and some external coax cables enables 1G Ethernet traffic to be received by the VSC8584 RJ-45 port, routed through the VSC8584 and externally via coax loopback cables through the SGMII interface and transmitted back to the traffic source on the same copper port. First configure the SerDes in SGMII mode by writing to Micro page 18'd. This is a global setting and does not need to be applied per port.

Steps for external SGMII loopback:

1. Set up the copper traffic source (i.e., IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45 Port 0.
3. Connect two matched coax cables, J1 - J4 and J2 - J5.
4. Write using the "Micro Page Registers" window: 18'd 0 × 80F0
5. When "Micro Page" 18'd is read back, bit 15 will clear.
6. Linkup bit is in MII Reg 1, bit 2 (MII 1.2), read twice to update.

Traffic should be the following:

Steps for SGMI forwarding port 0 ⟷ port 1:

1. Set up the Copper traffic source (i.e., IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45 Port 0.
3. Connect two matched coax cables as follows:
   J1 <TDIN0+> to J6 <RXDOUT1+>
   J2 <TDIN0-> to J7 <RXDOUT1→
   J5 <RXDOUT0-> to J10 <TXDIN1→
   J4 <RXDOUT0+> to J9 <TXDIN1+>
4. Write using the "Micro Page Registers" window: 18'd 0 × 80F0.
5. When "Micro Page" 18'd is read back, bit 15 will clear.
6. Linkup bit is in MII Reg 1, bit 2 (MII 1.2), read twice to update

4.4.4 Fiber Media Operation (1000BASE-X)

Follow all steps in section 3.4.2 with fiber media connection to (IXIA) and add the following steps.

1. Write using the "Micro Page Registers" window: 18'd 0 × 8FC1. (Global)
2. When "Micro Page" 18'd is read back, bit 15 will clear.
3. Write "MII Register" (PHY 0) 23'd 0 × 0204 (Sets Media Mode)
4. Write "MII Register" (PHY0) 0'd 0 × 9040 (SW Reset for media mode setting to have effect)
5. Write "Extended MII Register" (PHY0) 19'd 0 × 0001 (Flip SIGDET polarity if necessary)
6. Write "MII Register" (PHY0) 0'd 0 × 0004 (Disable Auto Neg if necessary)

Traffic should be flowing.

4.4.5 Fiber Media Operation (100BASE-FX)

Follow all steps in section 3.4.2 with fiber media connection to (IXIA) and add the following steps.

1. Write using the "Micro Page Registers" window: 18'd 0x8FD1. (Global)
2. When "Micro Page" 18'd is read back, bit 15 will clear.
3. Write "MII Register" (PHY 0) 23'd 0x0304 (Sets Media Mode)
4. Write "MII Register" (PHY0) 0'd 0x9040 (SW Reset for media mode setting to have effect)
5. Write "Extended MII Register" (PHY0) 19'd 0x0001 (Flip SIGDET polarity if necessary)
6. Write "MII Register" (PHY0) 0'd 0x0004 (Disable Auto Neg if necessary)

Traffic should be flowing.

4.5 Useful Registers

4.5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. Refer to datasheet for configuration options.

A Good CRC packet counter is in ExtMII 18.13:0. A read of the register reads back the good CRC packets and then clears the register so the subsequent reads will be 0 if no traffic has been received. If traffic has been received since the last read, bit 15 will be set.

4.5.2 Copper PHY Error Counters

Idle errors = MII 10.7:0
RX errors = MII 19.7:0
False carrier = MII 20.7:0
Disconnects = MII 21.7:0
CRC errors = ExtMII 23.7:0

4.5.3 Fiber PHY Error Counters

Good RX CRC packets = Ext3MII 28.13:0
Bad RX CRC packets = Ext3MII 29.7:0
Good TX CRC packets = Ext3MII 21.13:0
Bad TX CRC packets = Ext3MII 22.7:0

4.5.4 Configuring 1588 Daisy-Chain SPI Time-Stamping

For Master VSC8584EV, run these instructions for each port 0-3, as indicated by the "phy" variable below:

smiwrite phy 31 4
smiwrite phy 17 133
smiwrite phy 18 0
smiwrite phy 16 45088
smiwrite phy 17 133
smiwrite phy 18 0
smiwrite phy 16 47136
smiwrite phy 31 0

Note: the accesses above can be pasted into a text file and loaded via the customer GUI "Run PHY Script" feature, after substituting the desired port number 0-3 for "phy" above.

For Slave VSC8584EV, run the same instructions listed above for Master VSC8584EV for each port 0-3. Then, run the following write only on port 0:

smiwrite 0 31 4
smiwrite 0 26 0 × c0f7
smiwrite 0 31 0

5   Additional Information

For any additional information or questions regarding the devices mentioned in this document, contact your local sales representative.