VSC8662 Datasheet
Dual Port 10/100/1000BASE-T PHY and 100BASE-FX/1000BASE-X SerDes with Recovered Clock Outputs

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Contents

Figures

Tables

1 Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.3

Revision 4.3 of this datasheet was published in November 2018. The following is a summary of the changes implemented in the datasheet:

- Illustrations for the SerDes MAC and SGMII MAC connections were updated to show the appropriate capacitance for MAC_TDP and MAC_TDN. For more information, see Figure 3, page 6 and Figure 4, page 7.
- Timeout values for the ActiPHY link status timeout control bits were corrected. For more information, see Table 36, page 66.
- Bit description for the SIGDET pin polarity (bit 0) was clarified that it is a sticky bit. For more information, see Table 44, page 72

1.2 Revision 4.2

Revision 4.2 of this datasheet was published in May 2014. The following is a summary of the changes implemented in the datasheet:

- SerDes MAC and media interface descriptions and graphics were updated to remove references to integrated AC decoupling capacitors in the receive path.
- Total jitter receive tolerance specification for SerDes MAC and media inputs were updated to remove minimum values.

1.3 Revision 4.1

Revision 4.1 of this datasheet was published in April 2011. In revision 4.1 of the document, the VSC8662XIC-03 part was added. VSC8662XIC-03 supports an operating temperature range of –40 °C ambient to 100 °C case.

1.4 Revision 4.0

Revision 4.0 of this datasheet was published in June 2010. There were no changes to the technical content of the document. The datasheet was updated to reflect that the product is now in full production.

1.5 Revision 2.0

Revision 2.0 of this datasheet was published in May 2010. This was the first publication of the document.

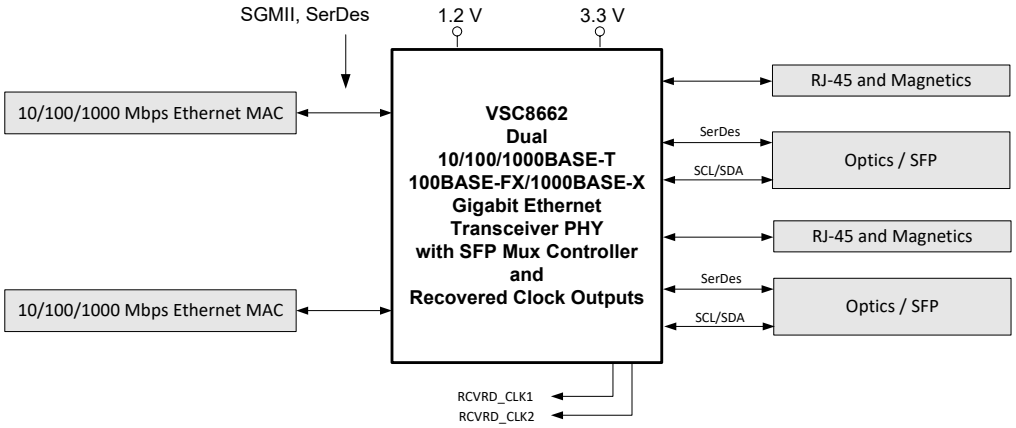
2 Overview

The VSC8662 device is a low-power, dual Gigabit Ethernet transceiver. It is designed for use in applications such as multiport switches and routers, where its compact ball grid array (BGA) packaging, low electromagnetic interference (EMI) line driver, and integrated line side termination resistors conserve both power and printed circuit board (PCB) space. Using the VSC8662 device in your design makes it possible to lower the component count without sacrificing capabilities or utility, resulting in more cost-effective production and deployment.

Vitesse's mixed signal and digital signal processing (DSP) architecture—a key operational feature of the VSC8662 device—assures robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 140 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environment and system electronic noise.

The following illustration shows a high-level, generic view of a VSC8662 application.

Figure 1 • **Typical Application**



2.1 Key Features

This section lists key aspects of the VSC8662 device functionality and design that distinguish it from similar products.

Low Power

- Low power consumption of 750 mW per port in 1000BASE-T mode and 242 mW in 1000BASE-X
- ActiPHY™ power management system with built-in intelligence and saving modes

Wide Range of Support

- Compliant with IEEE 802.3 specifications
- Support for >16 kB jumbo frames in all speeds with programmable synchronization FIFOs
- Supports Cisco SGMII v1.8 and 1000BASE-X MACs, IEEE 1149.1 JTAG boundary scan, and IEEE 1149.6 AC-JTAG

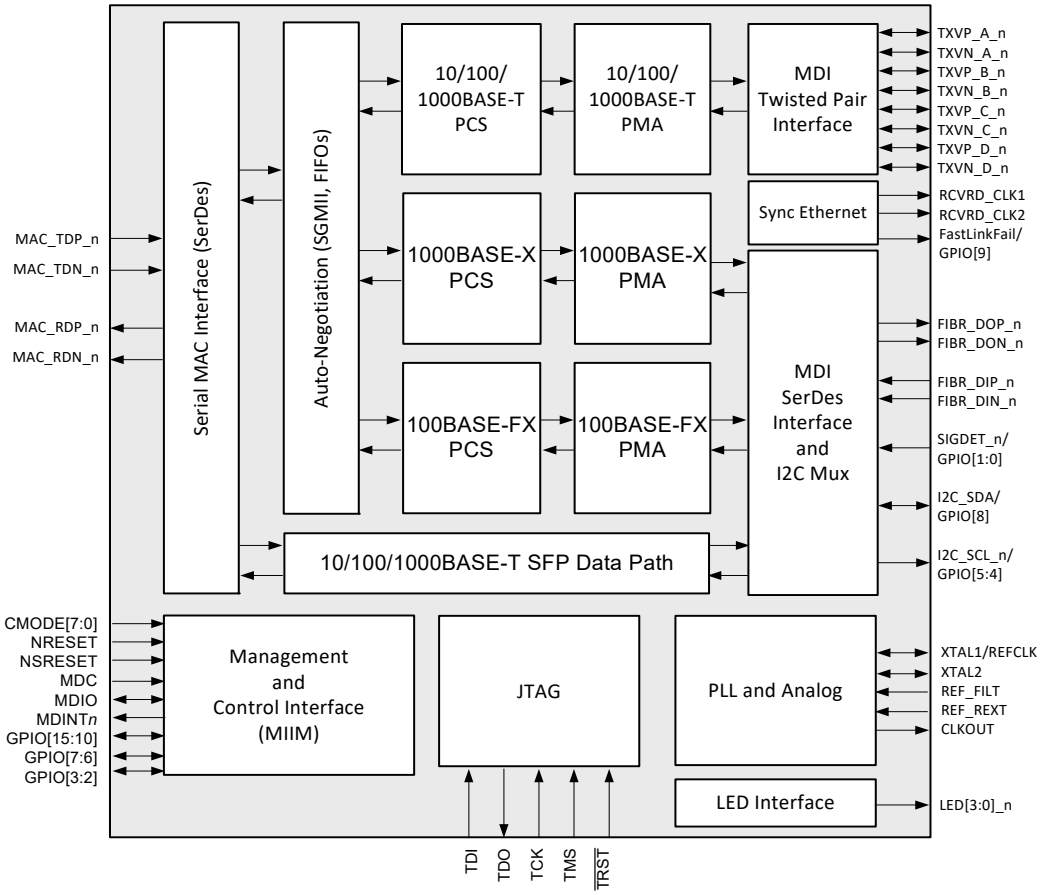
Flexibility

- Integrated dual two-wire serial multiplexer to control SFPs or PoE modules, eliminating the need for an external two-wire serial device for the control and status of SFP or PoE modules
- VeriPHY® cable diagnostics suite provides extensive network cable information such as cable length, termination status, and open/short fault location
- Patented, low EMI line driver with integrated line side termination resistors
- Four programmable direct drive LEDs per port with on-chip filtering and bi-color LED support
- Serial LED interface option
- Advanced SerDes features to ensure robust performance on longer signal traces, such as backplanes
- Extensive test features (including near end, far end, and connector loopback, and Ethernet packet generator with CRC error counter) to decrease time-to-market

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8662 device.

Figure 2 • **VSC8662 Block Diagram**



3 Functional Descriptions

This section provides detailed information about how the VSC8662 device works, what configurations and operational features are available, and how to test its function. It includes descriptions of the various device interfaces and how to set them up.

With the information in this section, you can better determine which device setup parameters you must access to configure the VSC8662 device to work in your application. There are two ways to configure the VSC8662 device. You can access and set its internal memory registers or use a combination of the device CMODE pins and its registers.

For information about the VSC8662 device registers, see Configuration, page 46.

For information about the device CMODE pins, see CMODE, page 84.

3.1 Operating Modes

With respect to its function in your design, the VSC8662 device acts as the interface between a media access controller (MAC) and either Category 5 (Cat5) media, 100BASE-FX fiber media, or 1000BASE-X fiber media. The VSC8662 device can also act as a MAC-to-MAC pass-through device to support triple-speed copper SFPs.

Depending on the speed of data throughput required in your application, the MAC may be either a SerDes or an SGMII device, and can also be configured to support twisted pair Cat5 cabling, 100BASE-FX/1000BASE-X fiber optic cabling, or copper small form factor pluggable (SFP) devices.

As shown in the following table, the operating mode you choose when setting up the VSC8662 device is a function of which type of MAC is to be connected, which data throughput speeds are required in the application, and the type of Cat5 media support required.

Table 1 • **Operating Mode vs. Speed**

VSC8662 Mode	10/100/1000BASE-T Support	1000BASE-X Fiber Optic Support	100BASE-FX Fiber Optic Support	10/100/1000BASE-T Copper SFP Support
SerDes MAC-to-Cat5 Link Partner	1000BASE-T only			
SGMII MAC-to-Cat5 Link Partner	Yes			
SerDes MAC-to-1000 Mbps SerDes with Auto-Negotiation		Yes		1000BASE-T only
SGMII MAC-to-1000 Mbps SerDes with Auto-Negotiation		Yes		1000BASE-T only
SerDes MAC-to-1000 Mbps SerDes with Pass-Through		Yes(1)		1000BASE-T only(1)
SGMII MAC-to-SGMII with Pass-Through		Yes(1)	Yes(1)	Yes(1)
SGMII MAC-to-100BASE-FX			Yes	
SerDes MAC with automatic media sense (AMS) and 1000 Mbps SerDes with Auto-Negotiation	1000BASE-T only	Yes		1000BASE-T only
SGMII MAC with AMS and 1000 Mbps SerDes with Auto-Negotiation	Yes	Yes		1000BASE-T only
SGMII MAC with AMS and 100BASE-FX	Yes		Yes	

Table 1 • **Operating Mode vs. Speed *(continued)***

VSC8662 Mode	10/100/1000BASE-T Support	1000BASE-X Fiber Optic Support	100BASE-FX Fiber Optic Support	10/100/1000BASE-T Copper SFP Support
SerDes MAC with AMS and Pass-Through	1000BASE-T only	Yes(1)		1000BASE-T only(1)
SGMII MAC with AMS and Pass-Through	Yes	Yes(1)	Yes(1)	Yes(1)

1. Because the device acts as a pass-through, the MAC must be capable of supporting this media.

3.2 SerDes MAC Interface

The VSC8662 SerDes MAC interface performs data serialization and deserialization functions using an integrated SerDes block. The interface operates at 1.25 Gbps speed, providing full-duplex and half-duplex 1000 Mbps bandwidth for SerDes mode and 10/100/1000 Mbps bandwidth for SGMII mode.

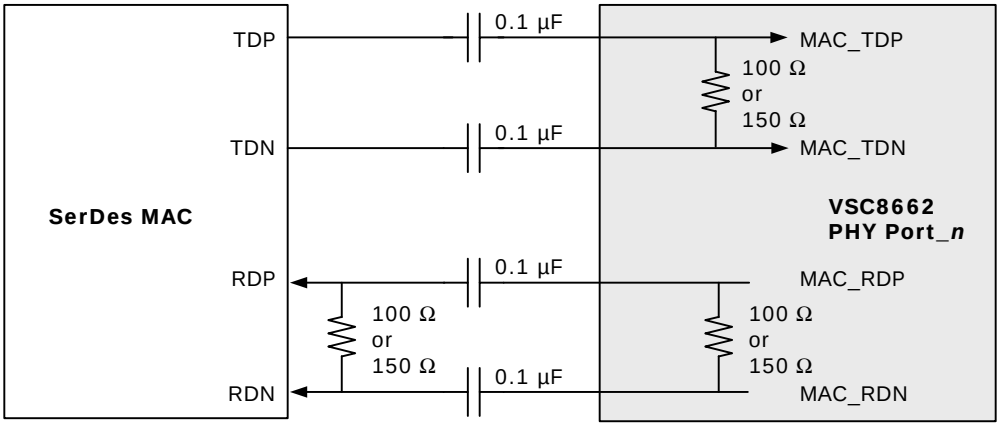
The SerDes MAC block has the termination resistor integrated into the device.

3.2.1 SerDes MAC

When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8662 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported. To configure the device for SerDes MAC mode set register 23, bit 12 = 1. This device also supports 1000BASE-X clause 37 MAC-side auto-negotiation and is enabled through register 23, bit 13. To configure the rest of the device for 1000 Mbps only operation, select the 1000BASE-T-only by disabling the 10/100BT advertisements in register 4 or using CMODE7, bit 1:0 to advertise 1000 Mbps only.

The following illustration shows a typical connection of the VSC8662 device to a SerDes MAC.

Figure 3 • **SerDes MAC Interface**



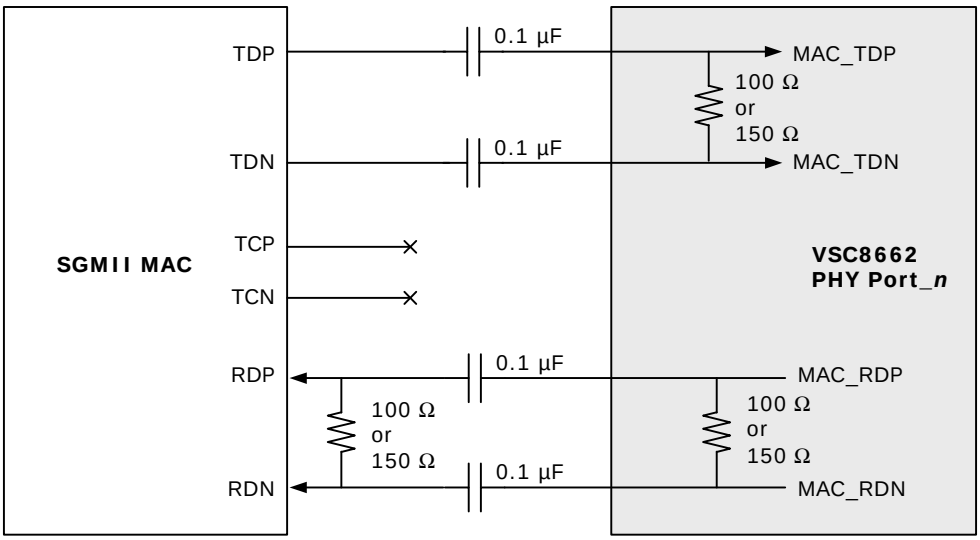
3.2.2 SGMII MAC

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8662 device can be connected to an SGMII-compatible MAC. To configure the device for SGMII MAC mode, set register 23, bit 12 = 0. This device also supports SGMII MAC-side auto-negotiation and is enabled through register 23, bit 13.

By default, the SGMII version supported is 1.7. Version 1.8 is also supported by setting register 20E, bit 15 = 1.

The following illustration shows a typical connection of the VSC8662 device to an SGMII-compatible MAC.

Figure 4 • **SGMII MAC Interface**



3.3 SerDes Media Interface

The VSC8662 device SerDes media interface performs data serialization and deserialization functions using an integrated SerDes block in the SerDes media interface. The interface operates at 1.25 Gbps speed, providing full-duplex and half-duplex for 10/100/1000 Mbps bandwidth that can connect directly to 100BASE-FX/1000BASE-X-compliant optical devices as well as to 10/100/1000BASE-T copper SFP devices. The interface can be operated in three SerDes modes:

- SerDes Media with PCS Auto-Negotiation
- SerDes Pass-Through mode
- SGMII to MAC-to-100BASE-FX mode

The SerDes media block has the termination resistor integrated into the device.

3.3.1 SerDes Media with PCS Auto-Negotiation

The SerDes with Media Interface PCS Auto-Negotiation mode supports IEEE standard 802.3, clauses 36 and 37, which describe 1000BASE-X fiber auto-negotiation. In this mode, control and status of the SerDes media is displayed in the VSC8662 device registers 0 through 15 in a manner similar to what is described in the IEEE standard 802.3, clause 28. In this mode, connected copper SFPs can only operate at 1000BASE-T speed. A link in this mode is established using auto-negotiation (enabled or disabled) between the PHY and the link partner. To configure the PHY in this mode, set register 23, bits 10:8 = 010. To configure 1000BASE-X auto-negotiation for this mode, set Register 0, bit 12.

Registers 0 through 15 per clause 37 are mapped over the clause 28 register when the PHY connects to a fiber link partner. Consequently, the registers used to control copper per clause 28 have the same function as clause 37 when a fiber link partner is present.

For information about how the VSC8662 LEDs operate in this mode, see LED Behavior, page 19.

3.3.2 SerDes Pass-Through Mode

SerDes with Pass-Through mode is a feature that links a fiber module or copper SFP directly to the SerDes interface of the MAC through the VSC8662 device. For example, to support 10/100/1000 copper SFPs, the MAC must be able to operate in SGMII mode. Because the MAC controls the establishment of the link, PHY registers 0 through 15 do not indicate link information when in SerDes Pass-Through mode. To configure the PHY in this mode, set register 23, bits 10:8 = 001. Also, to establish the link, assert the SIGDET pin.

All relevant LED modes are supported except for Collision, Duplex, and Auto-negotiation Fault. This means that a triple-speed copper SFPs link up and data type can be indicated by the PHY's LEDs.

3.3.3 SGMII MAC-to-100BASE-FX Mode

The VSC8662 can support the 100BASE-FX communication speed to connect to fiber modules, such as GBICs and SFPs.

This capability is facilitated by using the connections on the SerDes pins when connected to a MAC through SGMII only. SGMII is required as it can transmit in 100 Mbps, whereas the SerDes MAC can only transmit 1000 Mbps. Ethernet Package Generator (EPG), cyclical redundancy checking (CRC) counters, and loopback modes are supported in the 100BASE-FX over SGMII mode. For information about how the VSC8662 LEDs operate in this mode, see LED Behavior, page 19. To configure the PHY in this mode, set register 23, bits 10:8 = 011.

3.3.4 Unidirectional Transport for Fiber Media

In addition, the VSC8662 device supports 802.3ah for unidirectional transport across its 1000BASE-X and 100BASE-FX fiber media. This feature enables transmission across fiber media, regardless of whether the PHY has determined that a valid link has been established (register 1, bit 2). The only valid operating modes for unidirectional fiber mode are 100BASE-FX or 1000BASE-X fiber media (set in register 23). SerDes pass-through mode is unidirectional by default.

To enable this feature, set register 0, bit 5 to 1. For status of the unidirectional ability, read register 1, bit 7.

Note Auto-media sense will not work with this feature. In addition, because unidirectional fiber media needs auto-negotiation disabled, this means that SGMII auto-negotiation must also be disabled (register 23, bit 13 = 0), and full-duplex mode must be enabled (register 0, bit 8 = 1).

3.4 Advanced SerDes Features

The VSC8662 device is equipped with advanced SerDes features that allow for a robust SerDes link performance.

3.4.1 SerDes Receiver Equalization

To achieve better SerDes performance on longer signal traces (such as backplanes), the VSC8662 device has a built-in SerDes receiver equalization circuit. When enabled, the SerDes MAC receiver is capable of decoding a given receive signal with greater sensitivity, thereby achieving longer circuit lengths. This feature is found in register 17E.

3.4.2 SerDes Transmitter Amplitude Control

To achieve better SerDes performance on longer signal traces (such as backplanes), the VSC8662 device has a built-in SerDes transmitter amplitude control. The SerDes MAC transmitter is capable of adjustment by the user to achieve the optimal transmitted signal. This feature is found in register 17E.

3.4.3 SerDes Link Integrity Information

The VSC8662 device has included several link control and status register bits to help a customer debug and monitor their SerDes link integrity during operation. These capabilities are found in registers 27 and 28E.

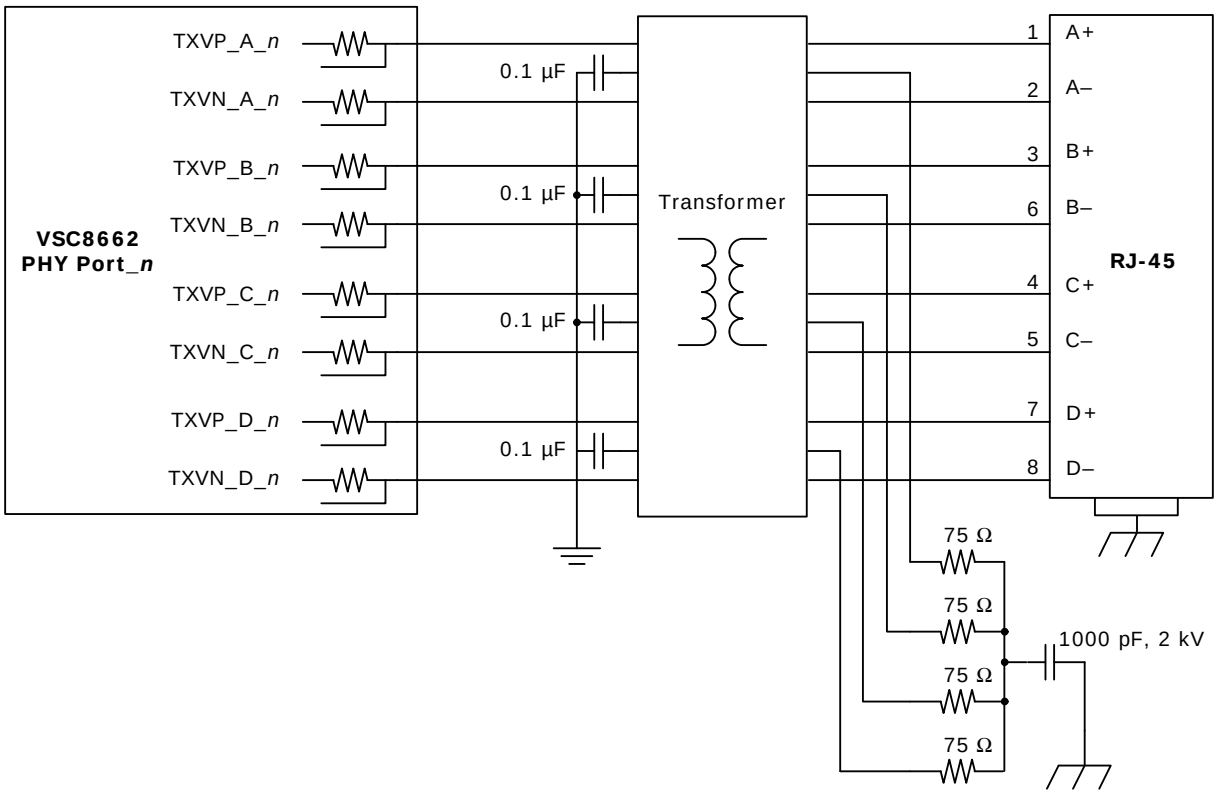
3.5 Cat5 Twisted Pair Media Interface

The VSC8662 device twisted pair interface is compliant with the IEEE standard 802.3-2002.

3.5.1 Voltage-Mode Line Driver

Unlike many other gigabit PHYs, the VSC8662 device uses a patented voltage-mode line driver that allows it to fully integrate the series termination resistors (required to connect the PHY's Cat5 interface to an external 1:1 transformer). Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 5 • **Cat5 Media Interface**



3.5.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8662 device supports twisted pair auto-negotiation as defined by clause 28 of the IEEE standard 802.3-2002. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-T. Auto-negotiation also allows a connected MAC to communicate with its link partner MAC through the VSC8662 device using optional “next pages,” which set attributes that may not otherwise be defined by the IEEE standard.

If the Cat5 link partner does not support auto-negotiation, the VSC8662 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation can be disabled in register 0, bit 12. If auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode. Note that while 10BASE-T and 100BASE-T do not require auto-negotiation, clause 40 has defined 1000BASE-T to require auto-negotiation. For more information about configuring auto-negotiation, see IEEE Standard and Main Registers, page 48.

3.5.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8662 device includes a robust automatic crossover detection feature for all three speeds on the twisted-pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with clause 40 of the IEEE standard 802.3-2002.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. You can change the default settings using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note The VSC8662 device can be configured to perform HP Auto-MDIX even when auto-negotiation is disabled (setting register 0.12 to 0) and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 2 • **Supported MDI Pair Combinations**

RJ-45 Pin Pairings				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

3.5.4 Manual MDI/MDI-X Setting

As an alternative to HP Auto-MDIX detection, you can force the PHY to be MDI or MDI-X using register 19E, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the MDI/MDI-X setting to be based on register 18, bits 7 and 5.

3.5.5 Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8662 device provides an automatic link speed “downshift” option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T.

This is useful in setting up in networks using older cable installations that may include only pairs A and B and not pairs C and D.

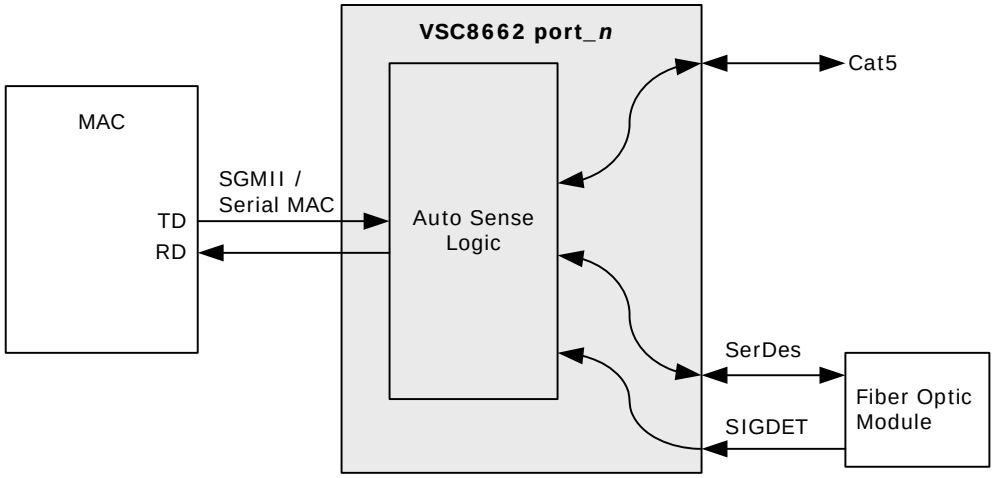
You can configure and monitor link speed downshifting using register bits 20E.4:1. For more information, see Extended PHY Control Set 1, page 61.

3.6 Automatic Media-Sense (AMS) Interface Mode

This mode can automatically set the media interface to Cat5 mode or to SerDes mode. The active media mode chosen is based on the automatic media-sense (AMS) preferences set in the device register 23, bit 11.

The following illustration shows a block diagram of the AMS functionality in the VSC8662 device.

Figure 6 • **Automatic Media Sense Block Diagram**



When both SerDes and Cat5 media interfaces attempt to establish a link, the preferred media interface overrides a link-up of the non-preferred media interface. For example, if the preference is set for SerDes mode and Cat5 media establishes a link, then Cat5 becomes the active media interface. However, after the SerDes media interface establishes a link, the Cat5 interface drops its link because the preference was set for SerDes mode. In this scenario, the SerDes preference determines the active media source until the SerDes link is lost. Also, Cat5 media cannot link up unless there is no SerDes media link established.

The following table lists the available AMS preferences.

Table 3 • **AMS Media Preferences**

Preference Setting	Cat5 Linked, Fiber Not Linked	SerDes Linked, Cat5 Not Linked	Cat5 Linked, SerDes Attempts to Link	SerDes Linked, Cat5 Attempts to Link	Both Cat5 and SerDes Attempt to Link
SerDes	Cat5	SerDes	SerDes	SerDes	SerDes
Cat5	Cat5	SerDes	Cat5	Cat5	Cat5

The status of the media mode selected by the AMS can be read from device register 20E, bits 7:6. It indicates whether copper media, SerDes media, or no media is selected.

Each PHY has three auto-media sense modes. The difference between the modes is based on the SerDes media modes:

- SerDes with PCS Auto-Negotiation (register 23, bit 10:8 = 110)
- SerDes with Pass-Through (register 23, bit 10:8 = 101)
- 100BASE-FX (register 23, bit 10:8 = 111)

For more information about SerDes media mode functionality with AMS enabled, see SerDes Media Interface, page 7.

For AMS with SerDes auto-negotiation and also 100BASE-FX, the status and control of both the Cat5 and the SerDes media can be made using registers 0 through 15. For AMS with SerDes pass-through, only the Cat5 interface can have its interface control and status monitored. The SerDes media must then be controlled and monitored within the MAC.

3.7 Transformerless Ethernet

The Cat5 media interface supports 10/100/1000BT Ethernet for backplane applications such as those specified by the PICMG™ 2.16 and ATCA™ 3.0 specifications for eight-pin channels. With proper AC coupling, the typical Cat5 transformer can be removed and replaced with capacitors.

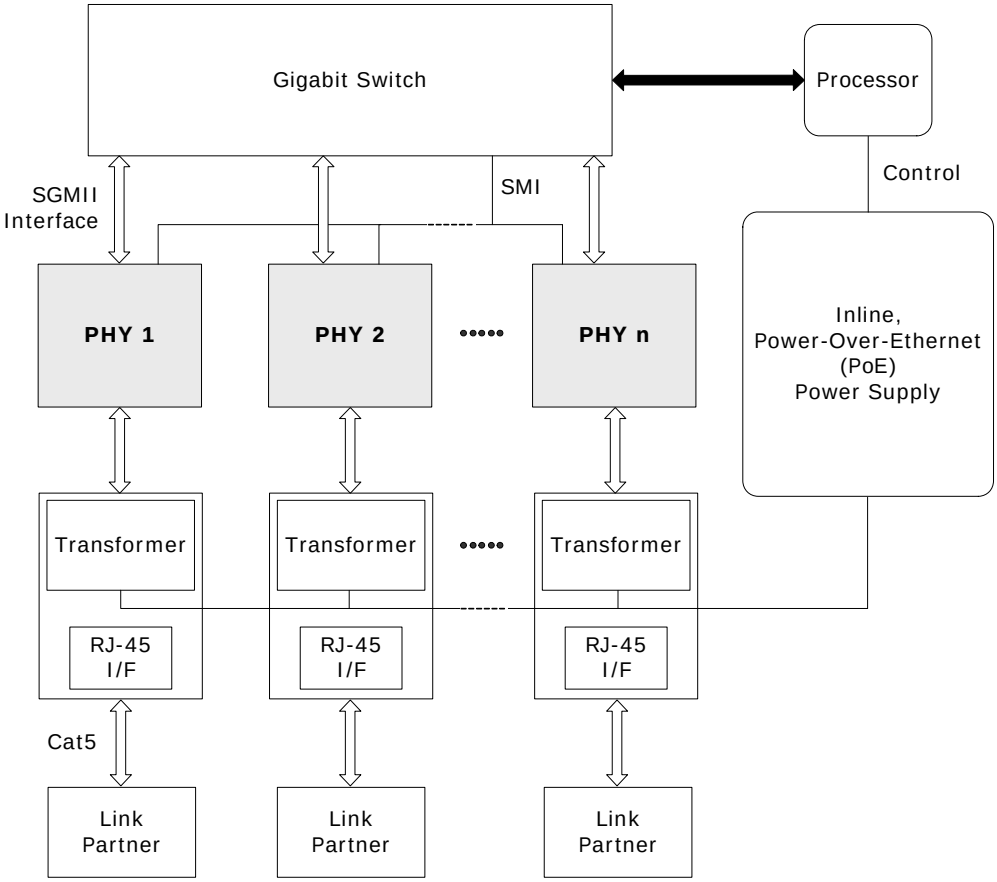
3.8 Ethernet Inline Powered Devices

The VSC8662 device can detect legacy inline powered devices in Ethernet network applications. Its inline powered detection capability can be part of a system that allows for IP-phone and other devices such as wireless access points to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a Private Branch Exchange (PBX) office switch over the telephone cabling. This can eliminate the need for an IP-phone to have an external power supply. It also enables the inline powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or some other uninterruptable power source).

For more information about legacy inline powered device detection, visit the Cisco Web site at www.cisco.com.

The following illustration shows an example of this type of application.

Figure 7 • **Inline Powered Ethernet Switch Diagram**



The following procedure describes the process that an Ethernet switch must perform in order to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power.

1. Enable the inline powered device detection mode on each VSC8662 PHY using its serial management interface. Set register bit 23E.10 to 1.
2. Ensure that the VSC8662 device Auto-Negotiation Enable bit (register 0.12) is also set to 1. In the application, the device sends a special Fast Link Pulse (FLP) signal to the LP. Reading register bit 23E.9:8 returns 00 during the search for devices that require Power-over-Ethernet (PoE).
3. The VSC8662 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered-down state. This is reported when VSC8662 device register bit 23E.9:8 reads back 01. It can also be verified as an inline power detection interrupt by reading VSC8662 device register bit 26.9, which should be a 1, and which is

subsequently cleared and the interrupt de-asserted after the read. If an LP device does not loop back the FLP after a specific time, VSC8662 device register bit 23E.9:8 automatically resets to 10.

4. If the VSC8662 PHY reports that the LP needs PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection if the VSC8662 device register bit 23E.9:8 automatically resets to 10, and then automatically changes to its normal auto-negotiation process. A link is then auto-negotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when VSC8662 device register bit 1.2 reads 0), the inline power should be disabled to the inline powered device external to the PHY. The VSC8662 PHY disables its normal auto-negotiation process and re-enables its inline powered device detection mode.

3.9 IEEE 802.3af PoE Support

The VSC8662 device is also compatible with switch designs that are intended for use in systems that supply power to Data Terminal Equipment (DTE) by means of the MDI or twisted pair cable, as described in clause 33 of the IEEE standard 802.3af.

3.10 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY™ power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY “wakes up” at a programmable interval and attempts to “wake-up” the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY™ power management mode in the VSC8662 device is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

There are three operating states possible when ActiPHY™ mode is enabled:

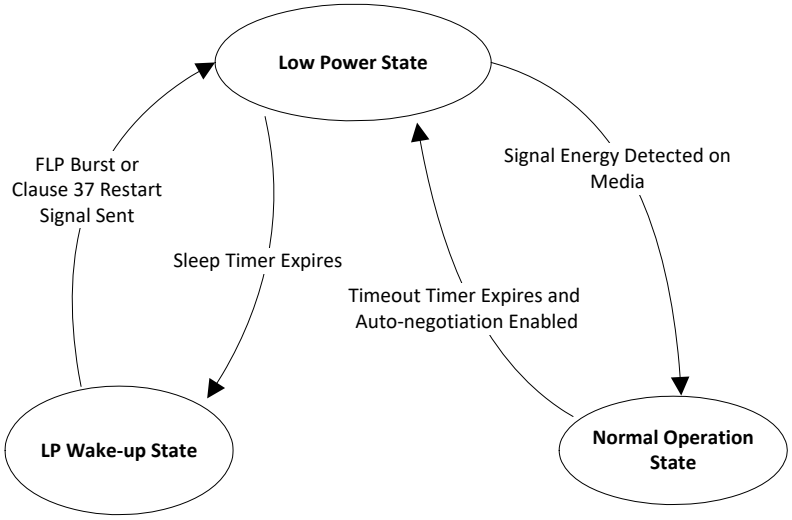
- Low power state
- LP wake-up state
- Normal operating state (link up state)

The VSC8662 device switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described. If auto-negotiation is disabled and the link is forced to use 10BT or 100BTX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 8 • **ActiPHY State Diagram**



3.10.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT*n*)
- CLKOUT

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY transitions from the low power state to the LP wake-up state periodically based on the programmable sleep timer (register bits 20E.14:13). The actual sleep time duration is randomized from –80 milliseconds (ms) to +60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

3.10.2 Link Partner Wake-up State

In this state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E.12:11.

In this state, the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT*n*)
- CLKOUT

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.10.3 Normal Operating State

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

3.11 Media Recovered Clock Outputs

For Synchronous Ethernet applications, the VSC8662 includes two recovered clock output pins: RCVRD_CLK1 (F16) and RCVRD_CLK2 (G16), which are controlled by registers 23G and 24G, respectively. These pins are synchronized to the clock of the active media link.

To enable recovered clock output, set register 23G or 24G, bit 15, to 1. (By default, the RCVRD_CLK1 and RCVRD_CLK2 pins are disabled and held low, including when NRESET or NSRESET is asserted.) Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 125 MHz), and squelch conditions. For more information about disabling the recovered clock, see Disabling Recovered Clock Output, page 100.

3.11.1 Clock Selection Settings

On each pin, the recovered clock can come from the following sources, as set by registers 23G or 24G, bits 1:0:

- Fiber SerDes media
- Copper media
- Copper transmitter TCLK output (RCVRD_CLK1 only)
- Local XTAL1/REFCLK input coming into the device

Note 1 When using the Auto-Media Sense feature, the recovered clock output cannot automatically change between each active media. Changing the media source must be managed through the recovered clock register settings.

Note 2 The 10BASE-T and 1000BASE-T master are not effective modes for Synchronous Ethernet clock recovery. In the case of 10BASE-T master mode, the receiver does not produce a reliable continuous clock source. In the case of 1000BASE-T master mode, the clock is based on the VSC8662 REFCLK pin, which is a local clock.

3.11.2 Clock Output Squelch

Under certain conditions, the PHY outputs a clock based on the XTAL1/REFCLK pin, such as when there is no link present or during auto-negotiation. To prevent an undesirable clock from appearing on the recovered clock pins, the VSC8662 squelches (that is, inhibits) the clock output based on any of the following criteria:

- No link is detected (the link status register 1, bit 2 = 0).
- The link is found to be unstable using the fast link failure detection feature (GPIO9 pin is asserted high).
- The active link is in 10BASE-T or in 1000BASE-T master mode. These modes produce unreliable recovered clock sources.

Use register 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature.

3.12 Fast Link Failure Indication

To aid Synchronous Ethernet applications, the VSC8662 can indicate the onset of a link failure in less than 1 ms. By comparison, the IEEE 802.3 standard establishes a delay up to 750 ms before indicating that a 1000BASE-T link is no longer present. Having a fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper and fiber media speeds.

The GPIO9 pin serves as the main indicator for a fast link failure. To enable fast link failure indication, set register 19E, bit 4 to 1 (0 is the default). Set the applicable PHY port in register 19G, bits 1:0. When a link on the selected port is failing, the GPIO9 pin asserts high and remains high until the link is re-established or until register 19G.1:0 is changed to a PHY port with an established link.

The fast link failure indication is also available on the serial management interface interrupt pins (MDINT*n*) for each PHY port. To enable this function, set register 25, bit 7 to 1. The MDINT pins assert if register 26, bit 7 is set to 1, and the pins clear once register 26 is read.

Note For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that will analyze the integrity of the link and, at the indication of failure, will assert.

3.13 Serial Management Interface

The VSC8662 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

For more information, see Extended Page Registers, page 69.

The SMI is a synchronous serial interface with bidirectional data on the MDIO pin that is clocked on the rising edge of the MDC pin. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external, 2 kΩ pull-up resistor is required on the MDIO pin.

3.13.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The following illustrations show the SMI frame format for the read operation and write operation.

Figure 9 • **SMI Read Frame**

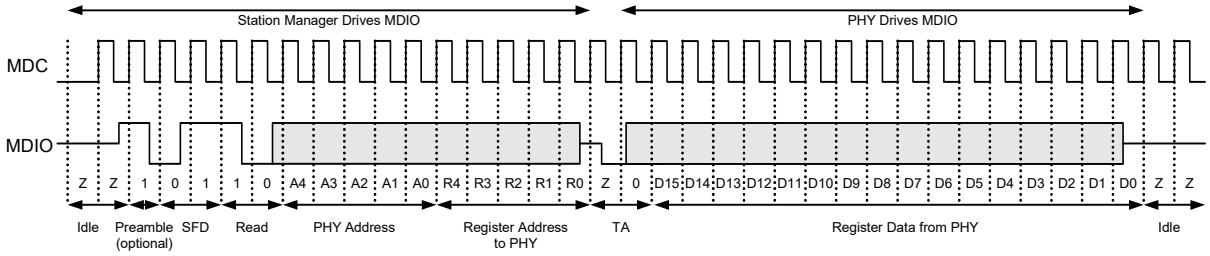
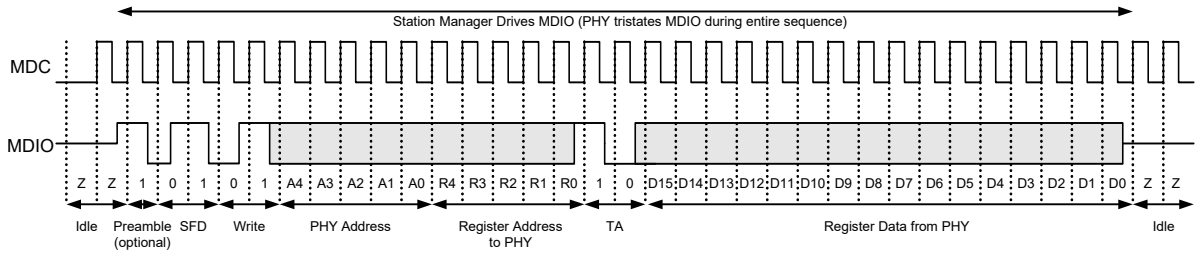


Figure 10 • **SMI Write Frame**



The following provides additional information about the terms used in Figure 9 and Figure 10.

Idle During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.

Preamble By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least one bit; otherwise, it may be of an arbitrary length.

Start of Frame (SFD) A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.

Read or Write Opcode A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.

PHY Address The VSC8662 device responds to a message frame only when the received PHY address matches its physical address. The physical address is five bits long (4:0). Bits 4:2 are set by the CMODE pins. Bit 1 is always 0 and bit 0 represents the PHY of the device being addressed. Note that this reserves PHY addresses 0–3, but only 0 and 1 should be used.

Register Address The next five bits are the register address.

Turnaround The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8662 device drives the second TA bit, a logical 0.

Data The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.

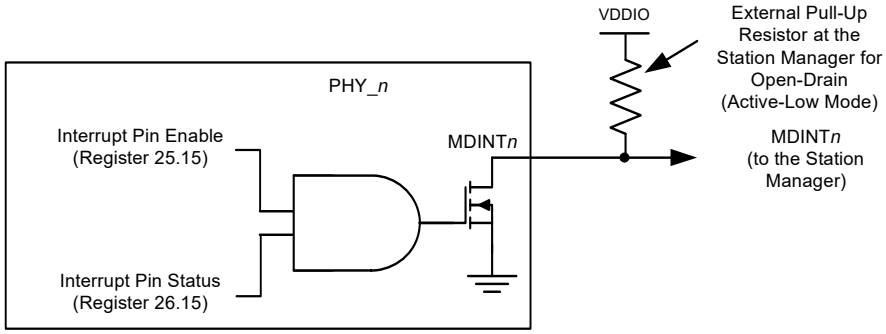
Idle The sequence is repeated.

3.13.2 SMI Interrupts

The SMI also includes an output interrupt signal, MDINT*n*, for signaling the station manager when certain events occur in the PHY. A separate MDINT*n* pin is included for each VSC8662 device PHY.

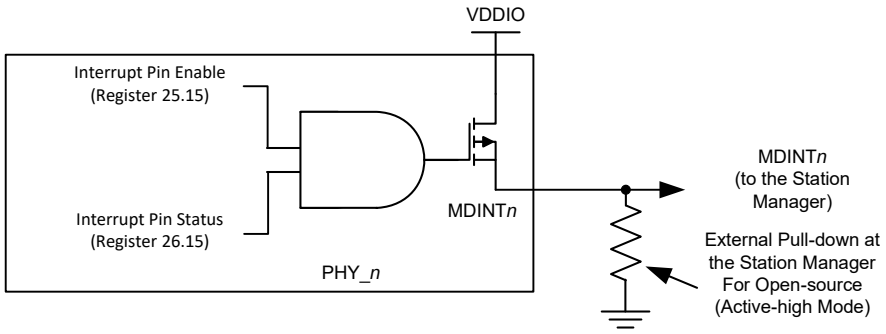
Each MDINT*n* pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 11 • **MDINT*n* Configured as an Open-Drain (Active-Low) Pin**



Alternatively, each MDINT*n* pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

Figure 12 • **MDINT*n* Configured as an Open-Source (Active-High) Pin**



If only one interrupt pin is required, each MDINT*n* pin can be tied together to a single pull-up or pull-down resistor in a wired-OR configuration.

When a PHY generates an interrupt, the MDINT*n* pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII register 25.15) is set.

3.14 LED Interface

The VSC8662 device drives up to four LEDs directly for each PHY port. All LED outputs are active-low and are driven using 3.3 V from the VDD33 power supply. The pins, mainly used to sink the current of the cathode side of an LED when active, can also supply power to the anode portion of LEDs when not in the active state. This allows for two LED pins to be used to drive a multi-status, bi-colored LED.

3.14.1 LED Modes

Each LED pin can be configured to display different status information. Set the LED mode either by using register 29 or the CMODE pin setting. For additional operating flexibility, LED output functions can be set on a per-port basis.

The modes in the following table are equivalent to the setting used in register 29 to configure each LED pin. For all LED states, 1 = pin held high (de-asserted), 0 = pin held low (asserted), and the blink/pulse-stretch is dependent on the LED behavior setting in register 30.

Table 4 • **LED Mode and Function Summary**

Mode	Function Name	LED State and Description
0	Link/Activity(1)	1 = No link in any speed on any media interface. 0 = Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 = No link in 1000BASE-T or 1000BASE-X. 0 = Valid 1000BASE-T or 1000BASE-X link. Blink or pulse-stretch = Valid 1000BASE-T or 1000BASE-X link with activity present.
2	Link100/Activity	1 = No link in 100BASE-TX or 100BASE-FX. 0 = Valid 100BASE-TX or 100BASE-FX link. Blink or pulse-stretch = Valid 100BASE-TX or 100BASE-FX link with activity present.
3	Link10/Activity	1 = No link in 10BASE-T. 0 = Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1 = No link in 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T. 0 = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1 = No link in 10BASE-T, 1000BASE-X, or 1000BASE-T. 0 = Valid 10BASE-T, 1000BASE-X, or 1000BASET-T link. Blink or pulse-stretch = Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link with activity present.
6	Link10/100/Activity	1 = No link in 10BASE-T, 100BASE-FX, or 100BASE-TX. 0 = Valid 10BASE-T or 100BASE-TX, 100BASE-FX, link. Blink or pulse-stretch = Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link with activity present.
7	Link100BASE-FX/ 1000BASE-X/Activity	1 = No link in 100BASE-FX or 1000BASE-X. 0 = Valid 100BASE-FX or 1000BASE-X link. Blink or pulse-stretch = Valid 100BASE-FX or 1000BASE-X link with activity present.
8	Duplex/Collision	1 = Link established in half-duplex mode, or no link established. 0 = Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1 = No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1 = No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present if register bit 30.14 is set to 1).

Table 4 • **LED Mode and Function Summary *(continued)***

Mode	Function Name	LED State and Description
11	100BASE-FX/ 1000BASE-X Fiber Activity	1 = No 100BASE-FX or 1000BASE-X activity present. Blink or pulse-stretch = 100BASE-FX or 1000BASE-X activity present (becomes RX activity present if register bit 30.14 is set to 1).
12	Auto-Negotiation Fault	1 = No auto-negotiation fault present. 0 = Auto-negotiation fault occurred.
13	Serial Mode	Serial stream = See Serial LED Mode, page 20. Only relevant on PHY port 0 and reserved in others.
14	Force LED Off	1 = De-asserts the LED(2).
15	Force LED On	0 = Asserts the LED(2).

1. Link/Activity can be configured to only display copper link and disable fiber link status by setting register bits 30.15 to 1.
2. Setting this suppresses the LED blink after reset.

3.14.2 Extended LED Modes

In addition to the LED modes in register 29, there is also additional LED modes that are enabled whenever any of the Register 19E bits 15 to 12 are set to 1. These extended modes are shown in Table 5, page 19. For example, LED0 = Mode 17 means that Register 19E bit 12 = 1 and Register 30 bits 3 to 0 = 0001.

Table 5 • **Extended LED Mode and Function Summary**

Mode	Function Name	LED State and Description
16	Link1000BASE-X Activity	1 = No link in 1000BASE-X. 0 = Valid 1000BASE-X link.
17	Link100BASE-FX Activity	1 = No link in 100BASE-FX. 0 = Valid 100BASE-FX link.
18	1000BASE-X Activity	1 = No 1000BASE-X activity present. Blink or pulse-stretch = 1000BASE-X activity present
19	100BASE-FX Activity	1 = No 100BASE-FX activity present. Blink or pulse-stretch = 100BASE-FX activity present
20	Force LED Off	1 = De-asserts the LED.
21	Force LED On	0 = Asserts the LED. LED Pulsing is disabled with this mode.

3.14.3 LED Behavior

Several LED behaviors can be programmed into the VSC8662 device. Use the settings in register 30 to program LED behavior, which includes the following:

LED Combine Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

LED Blink or Pulse-Stretch This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED

pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

Rate of LED Blink or Pulse-Stretch This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

LED Pulsing Enable To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

LED Blink After Reset The LEDs will blink for one second after power-up and after any time all resets have been de-asserted. This can be disabled through register 19E, bit 11 = 0.

Fiber LED Disable This bit controls whether the LEDs indicate the Fiber and Copper status (default) or the Copper status only.

3.14.4 Serial LED Mode

Optionally, the VSC8662 device can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to Serial LED mode. When the mode is enabled on PHY0, the device LED0_0 pin becomes the serial data pin and the LED1_0 pin becomes the serial clock pin. All other LED pins can still be configured normally. The Serial LED mode clocks the 48 LED status bits on the rising edge of the serial clock. Between each cycle of 48 bits, there is a 25 ms pause. To initialize synchronization, wait until after the first pause, after which the data becomes valid, before sampling the data on the falling edge of the serial clock. For more information about the LED clock and data timing relationship, see Figure 24, page 77.

The LED behavior settings (in device register 30) can also be used in Serial LED Mode. The controls are used on a per-PHY basis, where the LED combine and LED blink or pulse-stretch setting of LED0_*n* for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY.

The serial bitstream outputs, 1 through 48, of each LED signal are shown in the following table beginning with PHY port 0 and ending with 24 reserved bits. The individual signals can be clocked in the order shown.

Table 6 • **LED Serial Stream Order**

PHY0	PHY1		
Bit 1. Link/Activity	Bit 13. Link/Activity	Bit 25. Reserved	Bit 37. Reserved
Bit 2. Link1000/ Activity	Bit 14. Link1000/ Activity	Bit 26. Reserved	Bit 38. Reserved
Bit 3. Link100/ Activity	Bit 15. Link100/ Activity	Bit 27. Reserved	Bit 39. Reserved
Bit 4. Link10/ Activity	Bit 16. Link10/ Activity	Bit 28. Reserved	Bit 40. Reserved
Bit 5. Fiber Link/Activity	Bit 17. Fiber Link/Activity	Bit 29. Reserved	Bit 41. Reserved
Bit 6. Duplex/ Collision	Bit 18. Duplex/ Collision	Bit 30. Reserved	Bit 42. Reserved
Bit 7. Collision	Bit 19. Collision	Bit 31. Reserved	Bit 43. Reserved
Bit 8. Activity	Bit 20. Activity	Bit 32. Reserved	Bit 44. Reserved
Bit 9. Fiber Activity	Bit 21. Fiber Activity	Bit 33. Reserved	Bit 45. Reserved
Bit 10. TX Activity	Bit 22. TX Activity	Bit 34. Reserved	Bit 46. Reserved
Bit 11. RX Activity	Bit 23. RX Activity	Bit 35. Reserved	Bit 47. Reserved

Table 6 • **LED Serial Stream Order *(continued)***

PHY0	PHY1		
Bit 12. Auto-Negotiation Fault	Bit 24. Auto-Negotiation Fault	Bit 36. Reserved	Bit 48. Reserved

3.14.5 LED Port Swapping

For additional hardware configuration, the VSC8662 can have its LED ports swapped. This is useful feature to help simplify PCB layout design. Register 15G bit0 controls the LED port swapping mode based on the following table.

Table 7 • **LED Port Swapping Table**

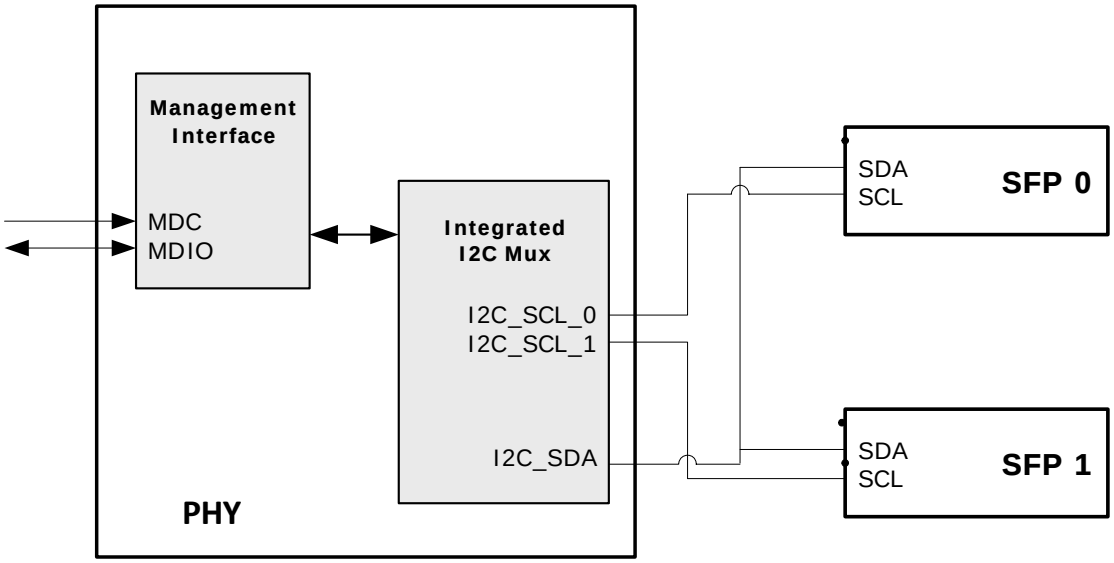
PHY	Mode 0 - default	Mode 1
Port 0	LEDs from Port 0	LEDs from Port 1
Port 1	LEDs from Port 1	LEDs from Port 0

3.15 Integrated Two-Wire Serial Multiplexer

The VSC8662 device includes an integrated dual two-wire serial multiplexer (mux), eliminating the need for an external two-wire serial device for the control and status of SFP or PoE modules. There are three two-wire serial controller pins: tour clocks and one shared data pin. Each SFP or PoE connects to their corresponding SCL clock pin and shares the SDA data pin, as shown in Figure 13, page 21.

For SFP modules, the VSC8662 device can also provide control for the module_detect and TX_DIS pins. To establish control of the SFP module_detect pins, use the VSC8662 GPIO[15:9] and GPIO[3:0] pins. For control of the SFP TX_DIS pins, use the VSC8662 LED pins in the force LED on and off modes.

Figure 13 • **Example of Using Two-Wire Serial Mux with SFP Control and Status**



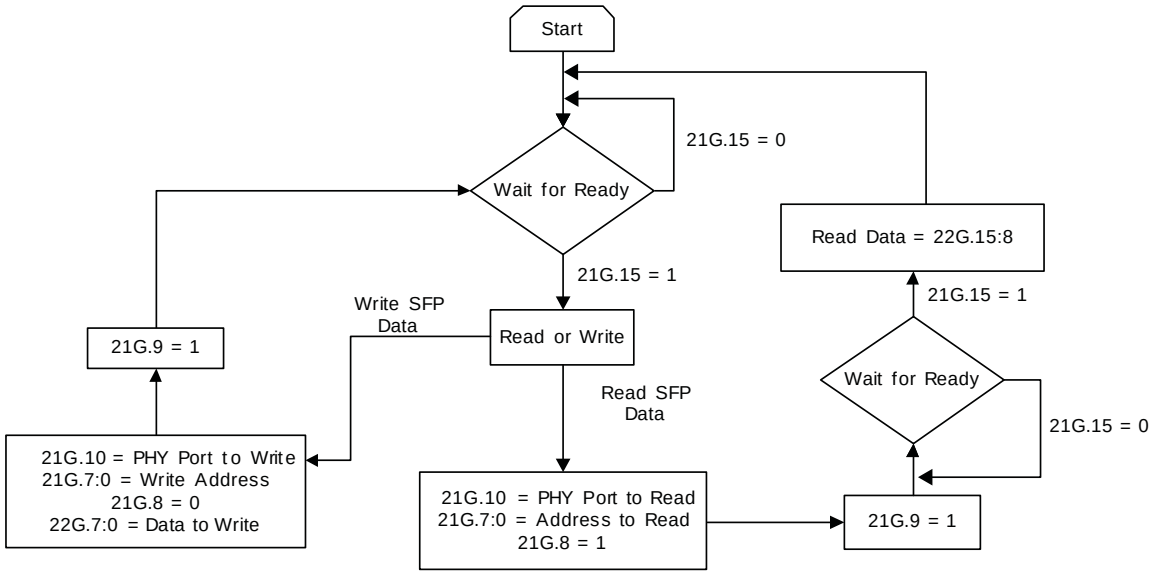
3.15.1 Read/Write Access Using the Two-Wire Serial Mux

The VSC8662 device using the integrated two-wire serial mux can read and write to an SFP or PoE module through the SCL and SDA pins. If the ability is required to write to the slave two-wire serial device, refer to the device's specific datasheet for more information. Also note that the VSC8662 device does not automatically increment the two-wire serial address; each desired address must be intentionally set.

Main control of the integrated two-wire serial mux is available through register 20G. The two-wire serial mux pins are enabled or disabled using register 20G.3:0 (by default, the pins are GPIO). Register 20G.15:9 sets the two-wire serial device address (the default is 0xA0). Using register 20G.5:4, the two-wire serial frequency can be changed from 100 kHz to other speeds, such as 50 kHz, 100 kHz (the default), 400 kHz, and 2 MHz.

Registers 21G and 22G provide status and control of the read/write process. The following illustration depicts the read and write register flow.

Figure 14 • **Two-Wire Serial Mux Read and Write Register Flow**



To read a value from a specific address of the two-wire serial slave device:

7. Read the VSC8662 device register bit 21G.15, and ensure that it is set.
8. Write the PHY port address to be read to register bit 21G.10.
9. Write the two-wire serial address to be read to register bits 21G.7:0.
10. Set both register bits 21G.8 and 21G.9 to 1.
11. When register bit 21G.15 changes to 1, read the 8-bit data value found at register bits 22G.15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the two-wire serial slave device:

12. Read the VSC8662 device register bit 21G.15 and ensure that it is set.
13. Write the PHY port address to be written to register bit 21G.10.
14. Write the address to be written to register bits 21G.7:0.
15. Set register bit 21G.8 to 0.
16. Set register bits 22G.7:0 with the 8-bit value to be written to the slave device.
17. Set register bit 21G.9 to 1.

To avoid collisions during read and write transactions on the two-wire serial bus, always wait until register bit 21G.15 changes to 1 before performing another two-wire serial read or write operation.

3.16 GPIO Pins

The VSC8662 device provides up to ten dedicated general-purpose input/output (GPIO) pins. In addition, the fast link failover indication pin, two device SIGDET pins, and three two-wire serial mux control pins can also be configured as GPIO pins, resulting in a total of 16 GPIO pins.

All device GPIO pins and their behavior are controlled using registers. For more information, see General-Purpose I/O Registers, page 78.

3.17 Testing Features

The VSC8662 device includes several testing features designed to make it easier to perform system-level debugging and in-system production testing. This section describes the available features.

3.17.1 Ethernet Packet Generator (EPG)

The device EPG can be used at each of the 10/100/1000BASE-T speed settings for Copper Cat5 media and fiber media to isolate problems between the MAC and the VSC8662 device, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.This feature is not used when the SerDes media is set to pass-through mode.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8662 device is connected to a live network.

To enable the VSC8662 device EPG feature, set the device register bit 29E.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. If it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E and 30E. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If register bit 29E.13 is set to 0, register bit 29E.14 is cleared automatically after 30,000,000 packets are transmitted.

3.17.2 CRC Counters

Two separate cyclical redundancy checking (CRC) counters are available on all PHYs in the VSC8662 device and resides between the FIFO and SerDes MAC interface. There is a 14-bit good CRC counter available in register bits 18E.13:0 and a separate 8-bit bad CRC counter available in register bits 23E.7:0.

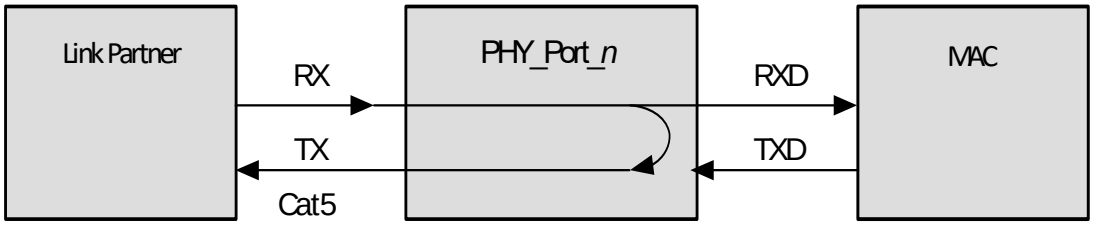
The device CRC counters operate in the 100BASE-FX/1000BASE-X over SerDes mode as well as in the 10/100/1000BASE-T mode testing as follows:

- After receiving a packet on the media interface, register bit 18E.15 is set and cleared after being read. The packet then is counted by either the good CRC counter or the bad CRC counter. Both CRC counters are also automatically cleared when read.
- The good CRC counter's highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000th packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

3.17.3 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

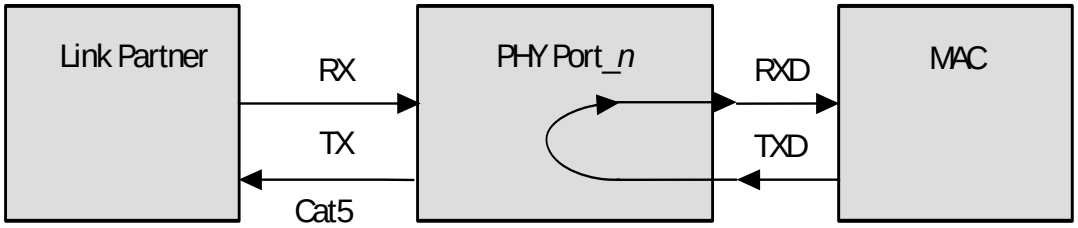
Figure 15 • **Far-End Loopback Diagram**



3.17.4 Near-End Loopback

When the near-end loopback testing feature is enabled (by setting the device register bit 0.14 to 1), data on the transmit data pins (TXD) is looped back in the PCS block, onto the device receive data pins (RXD), as shown in the following figure. When using this testing feature, no data is transmitted over the network.

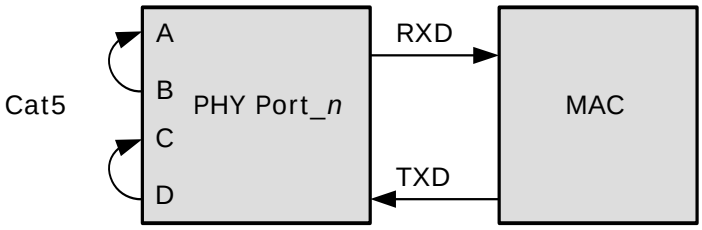
Figure 16 • **Near-End Loopback Diagram**



3.17.5 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in the following figure. The connector loopback feature functions at all available interface speeds.

Figure 17 • **Connector Loopback Diagram**



When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required. Execute the additional writes in the following order:

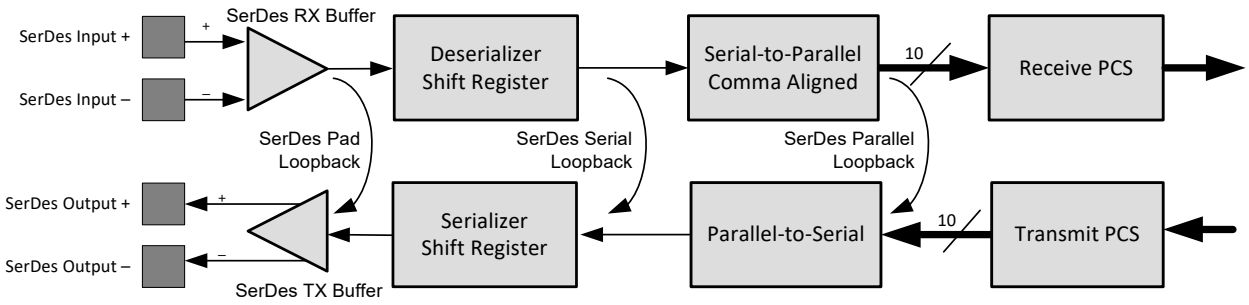
18. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
19. Disable pair swap correction. Set register bit 18.5 to 1.

3.17.6 SerDes Loopbacks

The SerDes loopback testing feature allows a user to ensure connectivity between the MAC or SerDes Link Partner and the PHY. There are several different SerDes loopbacks available, which can help debug SerDes link issues with a MAC/switch/ASIC or with a SerDes media link partner. In terms of clock reference, all three loopbacks are based on the clock from the link partner. You also have the option to not loopback the data and instead use the recovered clock instead of the clock based on REFCLK. This is useful for debugging the MAC transmitter clock's performance. Register 19E.10:8 sets the specific SerDes loopback for the media interface. To enable the media interface loopback, set register 19E.10 to

1. Register 19E.6:5 sets the specific SerDes loopback for the MAC interface. To enable the MAC interface loopback, set register 19E.7 to 1.

Figure 18 • **SerDes Loopbacks**



3.17.7 VeriPHY Cable Diagnostics

The VSC8662 device includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY® suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on the Cat5 twisted pair cabling.

Note If a link is established on the twisted pair interface in the 1000BASE-T mode, VeriPHY can run without disrupting the link or disrupting any data transfer. However, if a link is established in 100BASE-TX or 10BASE-T, VeriPHY causes the link to drop while the diagnostics are running. After diagnostics are finished, the link is re-established.

The following diagnostic functions are part of the VeriPHY suite:

- Detecting coupling between cable pairs
- Detecting cable pair termination
- Determining cable length

Coupling Between Cable Pairs Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause error conditions, such as anomalous coupling between cable pairs. All these conditions can prevent the device from establishing a link in any speed.

Cable Pair Termination Proper termination of Cat5 cable requires a 100 Ω differential impedance between the positive and negative cable terminals. The IEEE standard 802.3 allows for a termination of as high as 115 Ω or as low as 85 Ω. If the termination falls outside of this range, it is reported by the VeriPHY diagnostics as an anomalous termination. The diagnostics can also determine the presence of an open or shorted cable pair.

Cable Length When the Cat5 cable in an installation is properly terminated, VeriPHY reports the approximate cable length in meters.

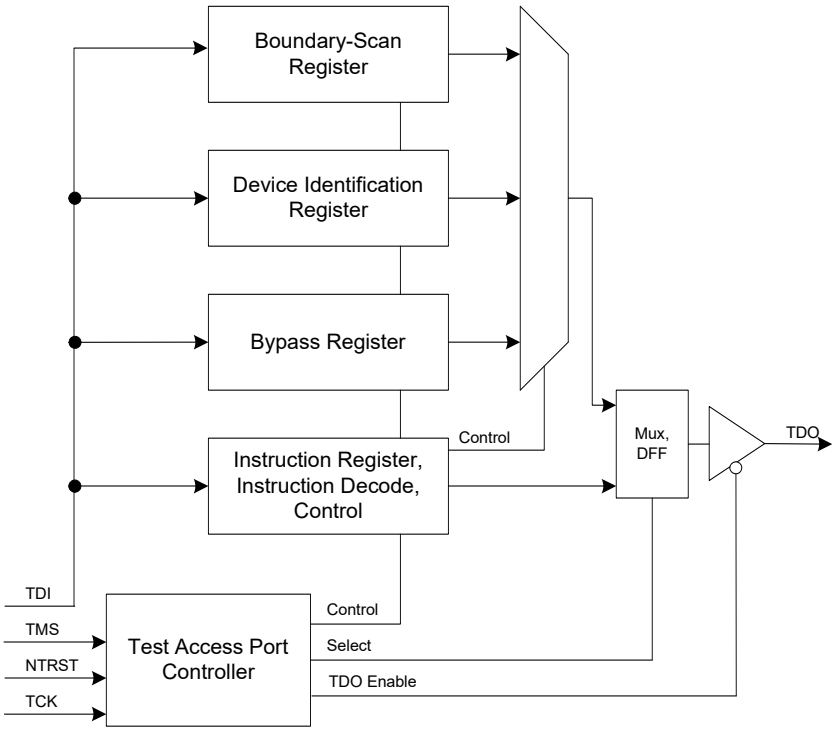
3.17.8 IEEE 1149.1 JTAG Boundary Scan

The VSC8662 device supports the Test Access Port (TAP) and Boundary Scan Architecture described in the IEEE standard 1149.1. The device includes an IEEE 1149.1-compliant test interface, often referred to as a “JTAG TAP Interface.”

The JTAG boundary scan logic on the VSC8662 device, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal NTRST.

The following illustration shows the TAP and Boundary Scan Architecture.

Figure 19 • **Test Access Port and Boundary Scan Architecture Diagram**



After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded either from a shift register (when a new instruction is shifted in) or, if there is no new instruction in the shift register, a default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

3.17.9 JTAG Instruction Codes

The VSC8662 device supports the following instruction codes:

EXTEST Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.

SAMPLE/PRELOAD Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following table provides information about the meaning of IDCODE binary values stored in the device JTAG registers.

Table 8 • **JTAG Device Identification Register Description**

Description	Device Version Number	Model Number	Manufacturing Identity	LSB
Bit field	31 through 28	27 through 12	11 through 1	0
Binary value	00000	1000 0110 0110 0100	001 1001 1000	1

CLAMP Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.

HIGHZ Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

BYPASS The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

The following table provides more information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8662. For more information about these IEEE specifications, visit the IEEE Web site at www.IEEE.org.

Table 9 • **JTAG Interface Instruction Codes**

Instruction	Code	Selected Register	Register Width	IEEE 1149.1 Specification	IEEE 1149.6 Specification
EXTEST	0000	Boundary-Scan	161	Mandatory	
SAMPLE/PRELOAD	0001	Boundary-Scan	161	Mandatory	
IDCODE	0110	Device Identification	32	Optional	
CLAMP	0010	Bypass Register	1	Optional	
HIGHZ	0011	Bypass Register	1	Optional	
BYPASS	1111	Bypass Register	1	Mandatory	
EXTEST_PULSE	0100	Boundary-Scan Register	161		Mandatory
EXTEST_TRAIN	0101	Boundary-Scan Register	161		Mandatory
RESERVED	0111, 1000 through 1110				

3.17.10 Boundary Scan Register Cell Order

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Vitesse Web site at www.vitesse.com.

3.17.11 IEEE 1149.6 AC-JTAG Boundary Scan Interface

The IEEE 1149.6 AC-JTAG solution integrated on all SerDes ports of the VSC8662 device extends the capability of IEEE 1149.1 boundary scan for robust board-level testing. This interface is backward-compatible to the IEEE 1149.1 standard.

4 Configuration

The VSC8662 device can be configured using two different methods:

- Setting internal memory registers using the management interface
- Setting a combination of CMODE pins and registers

4.1 Registers

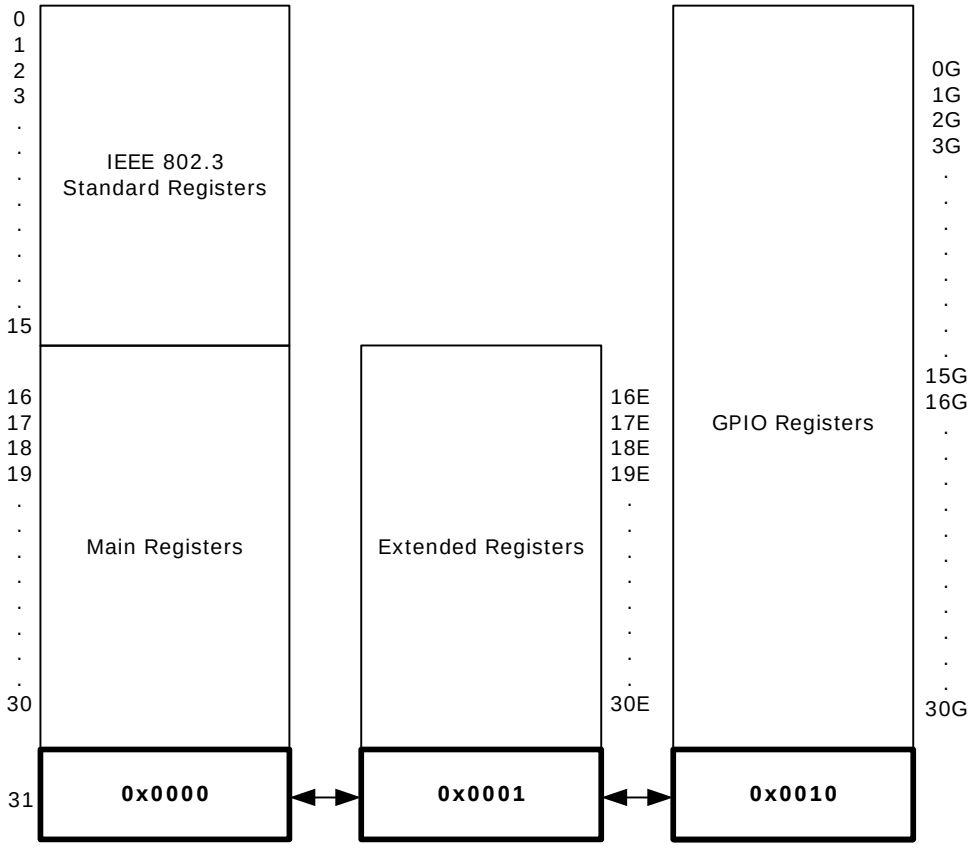
This section provides information about how to configure the VSC8662 device using its internal memory registers and the management interface. For information about configuring the device using the CMODE pins, see CMODE, page 63.

The VSC8662 device uses three types of registers:

- IEEE standard and main device registers with addresses from 0 to 31
- Extended registers with addresses from 16E through 30E
- General-purpose input and output (GPIO) registers with addresses from 0G to 30G

The following illustration shows the relationship between the device registers and their address spaces.

Figure 20 • **Register Space Diagram**



4.1.1 Reserved Registers

For main registers 16 through 31, extended registers 16E through 30E, and GPIO registers 0G through 30G, any bits marked as “Reserved” should be processed as read only and their states as undefined.

4.1.2 Reserved Bits

In writing to registers with reserved bits, use a “read-modify-then-write” technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.2 IEEE Standard and Main Registers

In the VSC8662 device, the page space of the standard registers consists of the IEEE standard registers and the Vitesse standard registers. The following table lists the names of the registers associated with the addresses as dictated by the IEEE standard.

Table 10 • **IEEE 802.3 Standard Registers**

Register Address	Register Name
0	Mode control
1	Mode status
2	PHY identifier 1
3	PHY identifier 2
4	Auto-negotiation advertisement
5	Auto-negotiation link partner ability
6	Auto-negotiation expansion
7	Auto-negotiation next-page transmit
8	Auto-negotiation link partner next-page receive
9	1000BASE-T control
10	1000BASE-T status
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	1000BASE-T status extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 11 • **Main Registers**

Register Address	Register Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2
18	Bypass control
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended control and status
23	Extended PHY control 1
24	Extended PHY control 2

Table 11 • **Main Registers *(continued)***

Register Address	Register Name
25	Interrupt mask
26	Interrupt status
27	MAC interface auto-negotiation control and status
28	Auxiliary control and status
29	LED mode select
30	LED behavior
31	Extended register page access

4.2.1 Mode Control

The device register at memory address 0 controls several aspects of VSC8662 functionality. The following table shows the available bit settings in this register and what they control.

Table 12 • **Mode Control, Address 0 (0x00)**

Bit	Name	Access	Description	Default
15	Software reset	R/W	This is a self-clearing bit that restores all serial management interface (SMI) registers to their default state, except for sticky and super sticky bits. 1 = Reset asserted. 0 = Reset de-asserted. You must wait 4 µs after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1 = Loopback enabled. 0 = Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bit 8 of this register).	0
13	LSB for speed selection	R/W	See bit 6 below.	0
12	Auto-negotiation enable	R/W	1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	1
11	Power-down	R/W	1 = Power-down enabled.	0
10	Isolate	R/W	1 = Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart auto-negotiation	R/W	This is a self-clearing bit. 1 = Restart auto-negotiation on media interface.	0
8	Duplex	R/W	1 = Full-duplex. 0 = Half-duplex.	0
7	Collision test enable	R/W	1 = Collision test enabled.	0
6, 13	Forced speed selection	R/W	MSB = bit 6, LSB = bit 13. 00 = 10 Mbps. 01 = 100 Mbps. 10 = 1000 Mbps. 11 = Reserved.	10

Table 12 • **Mode Control, Address 0 (0x00) *(continued)***

Bit	Name	Access	Description	Default
5	Unidirectional enable	R/W	When bit 0.12 = 1 or bit 0.8 = 0, this bit is ignored. When bit 0.12 = 0 and bit 0.8 = 1, the behavior is as follows: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established.	0
0	Reserved			00000

Note: Bit 5 is only applicable to 100BASE-FX and 1000BASE-X fiber media.

4.2.2 Mode Status

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

Table 13 • **Mode Status, Address 1 (0x01)**

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1 = 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1 = 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1 = 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1 = 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1 = 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1 = 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1 = 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1 = Extended status information present in register 15.	1
7	Unidirectional ability	RO	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established.	1
6	Preamble suppression capability	RO	1 = MF preamble may be suppressed. 0 = MF always required.	1

Table 13 • **Mode Status, Address 1 (0x01) *(continued)***

Bit	Name	Access	Description	Default
5	Auto-negotiation complete	RO	1 = Auto-negotiation complete.	0
4	Remote fault	RO	This bit latches high. 1 = Far-end fault detected.	0
3	Auto-negotiation capability	RO	1 = Auto-negotiation capable.	1
2	Link status	RO	This bit latches low. 1 = Link is up.	0
1	Jabber detect	RO	This bit latches high. 1 = Jabber condition detected.	0
0	Extended capability	RO	1 = Extended register capable.	1

Note: Bit 7 is only applicable to 100BASE-FX and 1000BASE-X fiber media

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8662 device are used to provide information associated with aspects of the device identification. The following tables list the readouts you can expect.

Table 14 • **Identifier 1, Address 2 (0x02)**

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0x0007

Table 15 • **Identifier 2, Address 3 (0x03)**

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	0x0001
9:4	Vitesse model number	RO	VSC8662 (0×26)	100110
3:0	Device revision number	RO		0000

4.2.4 Auto-Negotiation Advertisement

The bits in address 4 in the main registers space control the VSC8662 device ability to notify other devices of the status of its auto-negotiation feature. The following table shows the available settings and readouts.

Table 16 • **Device Auto-Negotiation Advertisement, Address 4 (0x04)**

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1 = Request enabled	0
14	Reserved	RO		0
13	Transmit remote fault	R/W	1 = Enabled	0
12	Reserved	R/W		0
11	Advertise asymmetric pause	R/W	1 = Advertises asymmetric pause	CMODE

Table 16 • **Device Auto-Negotiation Advertisement, Address 4 (0x04) *(continued)***

Bit	Name	Access	Description	Default
10	Advertise symmetric pause	R/W	1 = Advertises symmetric pause	CMODE
9	Advertise 100BASE-T4	R/W	1 = Advertises 100BASE-T4	0
8	Advertise 100BASE-TX FDX	R/W	1 = Advertise 100BASE-TX FDX	CMODE
7	Advertise 100BASE-TX HDX	R/W	1 = Advertises 100BASE-TX HDX	CMODE
6	Advertise 10BASE-T FDX	R/W	1 = Advertises 10BASE-T FDX	CMODE
5	Advertise 10BASE-T HDX	R/W	1 = Advertises 10BASE-T HDX	CMODE
4:0	Advertise selector	R/W		00001

4.2.5 Link Partner Auto-Negotiation Capability

The bits in main register 5 enable you to determine if the Cat5 link partner (LP) used with the VSC8662 device is compatible with the auto-negotiation functionality.

Table 17 • **Auto-Negotiation Link Partner Ability, Address 5 (0x05)**

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1 = Requested	0
14	LP acknowledge	RO	1 = Acknowledge	0
13	LP remote fault	RO	1 = Remote fault	0
12	Reserved	RO		0
11	LP advertise asymmetric pause	RO	1 = Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1 = Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1 = Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1 = Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1 = Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1 = Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1 = Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

4.2.6 Auto-Negotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP auto-negotiation functioning. The following table shows the available settings and readouts.

Table 18 • **Auto-Negotiation Expansion, Address 6 (0x06)**

Bit	Name	Access	Description	Default
15:5	Reserved	RO		00000000000
4	Parallel detection fault	RO	This bit latches high. 1 = Parallel detection fault.	0
3	LP next page capable	RO	1 = LP is next page capable.	0
2	Local PHY next page capable	RO	1 = Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1 = New page is received.	0
0	LP is auto-negotiation capable	RO	1 = LP is capable of auto-negotiation.	0

4.2.7 Transmit Auto-Negotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an auto-negotiation sequence. The following table shows the settings available.

Table 19 • **Auto-Negotiation Next Page Transmit, Address 7 (0x07)**

Bit	Name	Access	Description	Default
15	Next page	R/W	1 = More pages follow	0
14	Reserved	RO		0
13	Message page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Complies with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	Message /unformatted code	R/W		00000000001

4.2.8 Auto-Negotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP auto-negotiation. The following table shows the possible readouts.

Table 20 • **Auto-Negotiation LP Next Page Receive, Address 8 (0x08)**

Bit	Name	Access	Description	Default
15	LP next page	RO	1 = More pages follow	0
14	Acknowledge	RO	1 = LP acknowledge	0
13	LP message page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge 2	RO	1 = LP complies with request	0

Table 20 • **Auto-Negotiation LP Next Page Receive, Address 8 (0x08) *(continued)***

Bit	Name	Access	Description	Default
11	LP toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	LP message /unformatted code	RO		00000000000

4.2.9 1000BASE-T Control

The VSC8662 device's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 21 • **1000BASE-T Control, Address 9 (0x09)**

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000 = Normal. 001 = Mode 1: Transmit waveform test. 010 = Mode 2: Transmit jitter test as master. 011 = Mode 3: Transmit jitter test as slave. 100 = Mode 4: Transmitter distortion test. 101 to 111 = Reserved: Operation not defined.	000
12	Master/slave manual configuration	R/W	1 = Master/slave manual configuration enabled.	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1 = Configure PHY as master during negotiation. 0 = Configure PHY as slave during negotiation.	0
10	Port type	R/W	1 = Multi-port device. 0 = Single-port device.	1
9	1000BASE-T FDX capability	R/W	1 = PHY is 1000BASE-T FDX capable.	CMODE
8	1000BASE-T HDX capability	R/W	1 = PHY is 1000BASE-T HDX capable.	CMODE
7:0	Reserved	R/W		0x00

Note: Transmitter Test mode (bits 15:13) operates in the manner described in IEEE standard 802.3, section 40.6.1.1.2. When using any of the Transmitter Test modes, the Auto-Media Sense functionality must be disabled. For more information, see Extended PHY Control Set 1, page 40.

4.2.10 1000BASE-T Status

The bits in register 10 of the main register space allow you to read the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 22 • **1000BASE-T Status, Address 10 (0x0A)**

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0

Table 22 • **1000BASE-T Status, Address 10 (0x0A) *(continued)***

Bit	Name	Access	Description	Default
14	Master/slave configuration resolution	RO	1 = Local PHY configuration resolved to master. 0 = Local PHY configuration resolved to slave.	1
13	Local receiver status	RO	1 = Local receiver is operating normally.	0
12	Remote receiver status	RO	1 = Remote receiver OK.	0
11	LP 1000BASE-T FDX capability	RO	1 = LP 1000BASE-T FDX capable.	0
10	LP 1000BASE-T HDX capability	RO	1 = LP 1000BASE-T HDX capable.	0
9:8	Reserved	RO		00
7:0	Idle error count	RO	This is a self-clearing bit.	0x00

4.2.11 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 23 • **1000BASE-T Status Extension 1, Address 15 (0x0F)**

Bit	Name	Access	Description	Default
15	1000BASE-X FDX capability	RO	1 = PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1 = PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1 = PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1 = PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO		0x000

4.2.12 100BASE-TX Status Extension

Register 16 in the main registers page space of the VSC8662 device provides additional information about the status of the device's 100BASE-TX operation.

Table 24 • **100BASE-TX Status Extension, Address 16 (0x10)**

Bit	Name	Access	Description	Default
15	100BASE-TX Descrambler	RO	1 = Descrambler locked.	0
14	100BASE-TX lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0
13	100BASE-TX disconnect state	RO	This is a self-clearing bit. 1 = PHY 100BASE-TX link disconnect detected.	0
12	100BASE-TX current link status	RO	1 = PHY 100BASE-TX link active.	0

Table 24 • **100BASE-TX Status Extension, Address 16 (0x10) *(continued)***

Bit	Name	Access	Description	Default
11	100BASE-TX receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	100BASE-TX transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0
9	100BASE-TX SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	100BASE-TX ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7:0	Reserved	RO		

4.2.13 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 24, page 36.

Table 25 • **1000BASE-T Status Extension 2, Address 17 (0x11)**

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1 = Descrambler locked.	0
14	1000BASE-T lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0
13	1000BASE-T disconnect state	RO	This is a self-clearing bit. 1 = PHY 1000BASE-T link disconnect detected.	0
12	1000BASE-T current link status	RO	1 = PHY 1000BASE-T link active.	0
11	1000BASE-T receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	1000BASE-T transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0
9	1000BASE-T SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	1000BASE-T ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7	1000BASE-T carrier extension error	RO	This is a self-clearing bit. 1 = Carrier extension error detected.	0
6	Non-compliant BCM5400 detected	RO	1 = Non-compliant BCM5400 link partner detected.	0
5	MDI crossover error	RO	1 = MDI crossover error was detected.	0
4:0	Reserved	RO		

4.2.14 Bypass Control

The bits in the Bypass Control register in the VSC8662 device control aspects of functionality in effect when the device is disabled so that traffic can bypass it in your design. The following table shows the settings available.

Table 26 • **Bypass Control, Address 18 (0x12)**

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1 = PHY transmitter disabled.	0
14	4B5B encoder/decoder	R/W	1 = Bypass 4B/5B encoder/decoder.	0
13	Scrambler	R/W	1 = Bypass scrambler.	0
12	De-scrambler	R/W	1 = Bypass de-scrambler.	0
11	PCS receive	R/W	1 = Bypass PCS receiver.	0
10	PCS transmit	R/W	1 = Bypass PSC transmit.	0
9	LFI timer	R/W	1 = Bypass Link Fail Inhibit (LFI) timer.	0
8	Reserved	RO		
7	HP Auto MDI/MDI-X at forced 10/100	R/W	This is a sticky bit. 1 = Disable Auto MDI/MDI-X at forced 10/100 speeds.	1
6	Non-compliant BCM5400 detect disable	R/W	This is a sticky bit. 1 = Disable non-compliant BCM5400 detection.	0
5	Disable pair swap correction	R/W	This is a sticky bit. 1 = Disable the automatic pair swap correction.	0
4	Disable polarity correction	R/W	This is a sticky bit. 1 = Disable polarity inversion correction on each subchannel.	0
3	Parallel detect control	R/W	This is a sticky bit. 1 = Do not ignore advertised ability. 0 = Ignore advertised ability.	1
2	Pulse shaping filter	R/W	1 = Disable pulse shaping filter.	0
1	Disable automatic 1000BASE-T next page exchange	R/W	This is a sticky bit. 1 = Disable automatic 1000BASE-T next page exchanges.	0
0	CLKOUT output enable	R/W	This is a sticky bit. 1 = Enable clock output pin.	CMODE

Note: If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

4.2.15 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 27 • **Extended Control and Status, Address 19 (0x13)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO		

Table 27 • **Extended Control and Status, Address 19 (0x13) *(continued)***

Bit	Name	Access	Description	Default
7:0	100BASE-TX/ 1000BASE-T receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.16 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 28 • **Extended Control and Status, Address 20 (0x14)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO		
7:0	100BASE-TX/ 1000BASE-T false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.17 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 29 • **Extended Control and Status, Address 21 (0x15)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO		
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

4.2.18 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 30 • **Extended Control and Status, Address 22 (0x16)**

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	This is a sticky bit. 1 = Bypass link integrity test. 0 = Enable link integrity test.	0
14	Jabber detect disable	R/W	This is a sticky bit. 1 = Disable jabber detect.	0
13	Disable 10BASE-T echo	R/W	This is a sticky bit. 1 = Disable 10BASE-T echo.	1
12	Disable SQE mode	R/W	This is a sticky bit. 1 = Disable SQE mode.	1
11:10	10BASE-T squelch control	R/W	This is a sticky bit. 00 = Normal squelch. 01 = Low squelch. 10 = High squelch. 11 = Reserved.	00

Table 30 • **Extended Control and Status, Address 22 (0x16) *(continued)***

Bit	Name	Access	Description	Default
9	Sticky reset enable	R/W	This is a super-sticky bit. 1 = Enabled.	1
8	EOF Error	RO	This bit is self-clearing. 1 = EOF error detected.	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1 = 10BASE-T link disconnect detected.	0
6	10BASE-T link status	RO	1 = 10BASE-T link active.	0
5:3	Reserved	RO		
2:1	CRS control	R/W	Carrier sense control. The effect of each setting depends on whether it is half-duplex or full-duplex operation. For half-duplex operation: 00 = Receiving + transmitting. 01 = Receiving + transmitting. 10 = Receiving. 11 = Receiving. For full-duplex operation: 00 = Receiving. 01 = No carrier sensing. 10 = Receiving. 11 = No carrier sensing.	00
0	SMI broadcast write	R/W	This is a sticky bit. 1 = Enabled.	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which may improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and may improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0 through 31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY_0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

4.2.19 Extended PHY Control Set 1

The bits in the extended control set control the MAC auto-negotiation function, the SerDes functions, and report SGMII alignment errors. The following table shows the settings available.

Table 31 • **Extended PHY Control 1, Address 23 (0x17)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO		

Table 31 • **Extended PHY Control 1, Address 23 (0x17)** ***(continued)***

Bit	Name	Access	Description	Default
13	MAC interface auto-negotiation	R/W	This is a super-sticky bit. 1 = Enabled.	CMODE
12	MAC interface mode	R/W	This is a super-sticky bit. 1 = 1000BASE-X. 0 = SGMII.	0
11	AMS preference	R/W	This is a super-sticky bit. 1 = Cat5 copper preferred. 0 = SerDes fiber/SFP preferred.	0
10:8	Media operating mode	R/W	This is a super-sticky bit. 000 = Cat5 copper only. 001 = SerDes fiber/SFP pass-through mode only. No auto-negotiation performed in the PHY. 010 = 1000BASE-X fiber/SFP media only with auto-negotiation performed by the PHY. 011 = 100BASE-FX fiber/SFP on the fiber media pins only. 101 = Auto-Media Sense with Cat5 media or SerDes fiber/SFP pass-through mode. 110 = Auto-Media Sense with Cat5 media or 1000BASE-X fiber/SFP media with auto-negotiation performed by PHY. 111 = Auto-Media Sense with Cat5 media or 100BASE-FX fiber/SFP media. 100 = Reserved.	CMODE
7:6	Force AMS override	R/W	00 = Normal auto-media selection (AMS). 01 = Force AMS to select SerDes media only. 10 = Force AMS to select copper media only. 11 = Reserved.	00
5:4	Reserved	RO		
3	Far-end loopback mode	R/W	1 = Enabled.	0
2	Reserved	RO		
1	SGMII alignment error status	RO	This is a self-clearing bit. 1 = Alignment error detected since last read.	0
0	Reserved	RO		

Note: After configuring bits 13:8 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. If bits 13:8 are read before the software reset has taken place, then the bits only indicate the actual operating mode and not the pending operating mode.

4.2.20 Extended PHY Control Set 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 32 • **Extended PHY Control 2, Address 24 (0x18)**

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	This is a sticky bit. 011 = +5 Edge rate (slowest). 010 = +4 Edge rate. 001 = +3 Edge rate. 000 = +2 Edge rate. 111 = +1 Edge rate. 110 = Default edge rate. 101 = –1 Edge rate. 100 = –2 Edge rate (fastest).	110
12	PICMG 2.16 reduced power mode	R/W	This is a sticky bit. 1 = Enabled.	0
11:9	Reserved	RO		
8:7	SGMII input preamble	R/W	This is a sticky bit. 00 = No SGMII preamble required. 01 = One-byte SGMII preamble required. 10 = Two-byte SGMII preamble required. 11 = Reserved.	00
6	SGMII output preamble	R/W	This is a sticky bit. 0 = No SGMII preamble. 1 = Two-byte SGMII preamble.	1
5:4	Jumbo packet mode	R/W	This is a sticky bit. 00 = Normal IEEE 1.5 kB packet length. 01 = 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock). 10 = 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock). 11 = Reserved.	00
3:1	100BASE-TX transmitter amplitude control	R/W	011 = +3 Amplitude setting (largest). 010 = +2 Amplitude setting. 001 = +1 Amplitude setting. 000 = Default amplitude. 111 = –1 Amplitude setting. 110 = –2 Amplitude setting. 101 = –3 Amplitude setting. 100 = –4 Amplitude setting (smallest).	000
0	1000BASE-T connector loopback	R/W	1 = Enabled.	0

Note: When bits 5:4 are set to Jumbo Packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher Jumbo packet length.

4.2.21 Interrupt Mask

The bits in register 25 control the device interrupt mask. The following table shows the settings available.

Table 33 • **Interrupt Mask, Address 25 (0x19)**

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	This is a sticky bit. 1 = Enabled.	0
14	Speed state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
13	Link state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
12	FDX state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
11	Auto-negotiation error mask	R/W	This is a sticky bit. 1 = Enabled.	0
10	Auto-negotiation complete mask	R/W	This is a sticky bit. 1 = Enabled.	0
9	Inline powered device (PoE) detect mask	R/W	This is a sticky bit. 1 = Enabled.	0
8	Symbol error interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0
7	Fast link failure interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0
6	TX FIFO over/underflow interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0
5	RX FIFO over/underflow interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0
4	AMS media changed mask	R/W	This is a sticky bit. 1 = Enabled.	0
3	False-carrier interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0
2	Link speed downshift detect mask	R/W	This is a sticky bit. 1 = Enabled.	0
1	Master/Slave resolution error mask	R/W	This is a sticky bit. 1 = Enabled.	0
0	RX_ER interrupt mask	R/W	This is a sticky bit. 1 = Enabled.	0

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupt pendings that will cause bit 25.15 to be set.

4.2.22 Interrupt Status

The status of interrupts already written to the device are available for reading from register 26 in the main registers space. The following table shows the readouts you can expect.

Table 34 • **Interrupt Status, Address 26 (0x1A)**

Bit	Name	Access	Description	Default
15	Interrupt status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
14	Speed state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
13	Link state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
12	FDX state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
11	Auto-negotiation error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
10	Auto-negotiation complete status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
9	Inline powered device detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
8	Symbol error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
7	Fast link failure detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
6	TX FIFO over/underflow detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
5	RX FIFO over/underflow detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
4	AMS media changed status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
3	False-carrier interrupt status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
2	Link speed downshift detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
1	Master/Slave resolution error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
0	RX_ER interrupt status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.7, register 19E bit 4 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link-partner's data transmission.

4.2.23 MAC Interface Auto-Negotiation Control and Status

Device auto-negotiation for the MAC interface is controlled in register 27. The same register is used to check the status of those parameters. The following table shows the settings available.

Table 35 • **MAC Auto-Negotiation Control and Status, Address 27 (0x1B)**

Bit	Name	Access	Description	Default
15	MAC or media interlock	R/W	This is a sticky bit. 1 = MAC interface disabled when media link down. 0 = MAC interface not suppressed by media link status.	0
14	MAC or media restart auto-negotiation interlock	R/W	This is a sticky bit. 1 = MAC interface restarts its auto-negotiation if the media link changes. 0 = MAC interface does not automatically change if media link changes.	0
13	MAC interface auto-negotiation auto-sense	R/W	This is a sticky bit. 1 = If MAC auto-negotiation is enabled, this allows the MAC interface to be able to link to MACs with auto-negotiation enabled and disabled. 0 = Normal MAC auto-negotiation behavior.	0
12	MAC interface auto-negotiation restart	R/W	This is a self-clearing bit. 1 = Restart auto-negotiation.	0
11	MAC link partner restart request	RO	This is a self-clearing bit. Indicates a restart auto-negotiation request from a MAC link partner has occurred.	0
10	Reserved	RO		
9:8	Remote fault detected from MAC	RO	Corresponds to the remote fault bits sent by the MAC during auto-negotiation.	00
7	Asymmetric pause advertised by the MAC	RO	Corresponds to the asymmetric pause bit sent by the MAC during auto-negotiation.	0
6	Symmetric pause advertised by the MAC	RO	Corresponds to the symmetric pause bit sent by the MAC during auto-negotiation.	0
5	Full-duplex advertised by the MAC	RO	Corresponds to the full-duplex bit sent by the MAC during auto-negotiation.	0
4	Half-duplex advertised by the MAC	RO	Corresponds to the half-duplex bit sent by the MAC during auto-negotiation.	0
3	MAC auto-negotiation capable	RO	1 = MAC is auto-negotiation capable.	0
2	MAC interface link status	RO	1 = The MAC interface is actively linked.	0

Table 35 • **MAC Auto-Negotiation Control and Status, Address 27 (0x1B) *(continued)***

Bit	Name	Access	Description	Default
1	MAC interface auto-negotiation complete	RO	1 = The MAC interface auto-negotiation is complete.	0
0	MAC interface signal detect	RO	1 = The MAC interface internal signal detect is asserted.	0

4.2.24 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the readouts you can expect.

Table 36 • **Auxiliary Control and Status, Address 28 (0x1C)**

Bit	Name	Access	Description	Default
15	Auto-negotiation complete	RO	Duplicate of bit 1.5.	0
14	Auto-negotiation disabled	RO	Inverted duplicate of bit 0.12.	0
13	MDI/MDI-X crossover indication	RO	1 = MDI/MDI-X crossover performed internally.	0
12	CD pair swap	RO	1 = CD pairs are swapped.	0
11	A polarity inversion	RO	1 = Polarity swap on pair A.	0
10	B polarity inversion	RO	1 = Polarity swap on pair B.	0
9	C polarity inversion	RO	1 = Polarity swap on pair C.	0
8	D polarity inversion	RO	1 = Polarity swap on pair D.	0
7	ActiPHY link status time-out control [1]	R/W	This is a sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds. 01: 3.3 seconds. 10: 4.3 seconds. 11: 5.3 seconds.	CMODE
6	ActiPHY mode enable	R/W	This is a sticky bit. 1 = Enabled.	0
5	FDX status	RO	1 = Full-duplex. 0 = Half-duplex.	00
4:3	Speed status	RO	00 = Speed is 10BASE-T. 01 = Speed is 100BASE-TX or 100BASE-FX. 10 = Speed is 1000BASE-T or 1000BASE-X. 11 = Reserved.	0

Table 36 • **Auxiliary Control and Status, Address 28 (0x1C) *(continued)***

Bit	Name	Access	Description	Default
2	ActiPHY link status time-out control [0]	R/W	This is a sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 2.3 seconds. 01: 3.3 seconds. 10: 4.3 seconds. 11: 5.3 seconds.	0
1:0	Media mode status	RO	00 = No media selected. 01 = Copper media selected. 10 = SerDes media selected. 11 = Reserved.	00

4.2.25 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information you need to access the functionality of each of the outputs. For information about the LED modes referenced in the table, see Table 4, page 18.In addition, if enabling the Extended LED mode bits in Register 19E bits 15 to 12, then also refer to Table 5, page 19.

Table 37 • **LED Mode Select, Address 29 (0x1D)**

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
11:8	LED2 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
7:4	LED1 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE
3:0	LED0 mode select	R/W	This is a sticky bit. Select from LED modes 0 through 15.	CMODE

4.2.26 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 38 • **LED Behavior, Address 30 (0x1E)**

Bit	Name	Access	Description	Default
15	Copper and fiber LED combine disable	R/W	This is a sticky bit. 0 = Combine enabled (Copper/Fiber on Link/LinkXXXX(1)/Activity LED). 1 = Disable combination (Link/LinkXXXX/Activity LED indicates copper only).	0

Table 38 • **LED Behavior, Address 30 (0x1E)** ***(continued)***

Bit	Name	Access	Description	Default
14	Activity output select	R/W	This is a sticky bit. 1 = Activity LED becomes TX_Activity and fiber activity LED becomes RX_Activity. 0 = TX and RX activity both displayed on activity LEDs.	0
13	Reserved	RO		
12	LED pulsing enable	R/W	This is a sticky bit. 0 = Normal operation. 1 = LEDs pulse with a 5-kHz, 20% duty cycle when active.	0
11:10	LED blink/ pulse-stretch rate	R/W	This is a sticky bit. 00 = 2.5-Hz blink rate / 400 ms pulse-stretch. 01 = 5-Hz blink rate / 200 ms pulse-stretch. 10 = 10-Hz blink rate / 100 ms pulse-stretch. 11 = 20-Hz blink rate / 50 ms pulse-stretch. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.	CMODE
9	Reserved	RO		
8	LED3 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
7	LED2 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
6	LED1 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
5	LED0 pulse-stretch/ blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	CMODE
4	Reserved	RO		
3	LED3 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE
2	LED2 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE

Table 38 • **LED Behavior, Address 30 (0x1E) *(continued)***

Bit	Name	Access	Description	Default
1	LED1 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE
0	LED0 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (link/activity, duplex/collision). 1 = Disable combination (link only, duplex only).	CMODE

1. Link10, Link100, Link1000, Link10/100, Link100/1000, Link1000BASE-X, or Link1000BASE-FX.

Note: Bits 29.11:10 are controlled only by port 0 and affect the behavior of all ports.

4.3 Extended Page Registers

To provide functionality beyond the IEEE802.3-specified 32 registers and main device registers, the VSC8662 device includes an extended set of registers that provide an additional 15 register spaces.

To access the extended page registers (16E through 30E), enable extended register access by writing 0x0001 to register 31. For more information, see Table 40, page 50.

When extended page register access is enabled, reads and writes to registers 16 through 30 affect the extended registers 16E through 30E instead of those same registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page space. These registers are accessible only when the device register 31 is set to 0x0001.

Table 39 • **Extended Registers Page Space**

Register Address	Register Name
16E	SerDes Media control
17E	SerDes MAC/Media control
18E	CRC good counter
19E	SerDes loopback and SIGDET control
20E	Extended PHY control 3 (ActiPHY)
21E	Reserved
22E	Reserved
23E	Extended PHY control 4 (PoE and CRC error counter)
24E	VeriPHY 1
25E	VeriPHY 2
26E	VeriPHY 3
27E	Reserved
28E	SerDes MAC/media status
29E	Ethernet packet generator (EPG) 1
30E	EPG 2

4.3.1 Extended Page Access

The register at address 31 controls the access to both the extended and GPIO registers for the VSC8662 device. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 40 • **Extended Page Access, Address 31 (0x1F)**

Bit	Name	Access	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000 = Register 16 through 30 accesses main register space 0x0001 = Register 16 through 30 accesses extended register space 0x0010 = Register 0 through 30 accesses GPIO register space	0x0000

4.3.2 SerDes Media Control

Register 16E, which is accessible only when extended register access is enabled, controls the SerDes media interface. The following table shows the settings available.

Table 41 • **SerDes Media Auto-Negotiation Control/Status, Address 16E (0x10)**

Bit	Name	Access	Description	Default
15:14	Transmit remote fault	R/W	Remote fault indication sent to link partner (LP).	00
13:12	Link partner (LP) remote fault	RO	Remote fault bits sent by LP during auto-negotiation.	00
11	Parallel detect	R/W	1 = Enables parallel detect of auto-negotiation enabled and disabled devices.	0
10	SerDes media signal detect	RO	Signal detect indication on media interface.	0
9	Allow 1000BASE-X link-up	R/W	This is a sticky bit. 1 = Allows 1000BASE-X fiber media link-up capability. 0 = Suppress 1000BASE-X fiber media link-up capability.	1
8	Allow 100BASE-FX link-up	R/W	This is a sticky bit. 1 = Allows 100BASE-FX fiber media link-up capability. 0 = Suppress 100BASE-FX fiber media link-up capability.	1
7	SerDes media LP restart request	RO	This is a self-clearing bit. 1 = A restart auto-negotiation request from a SerDes media link partner has occurred.	0
6	Far end fault detected in 100BASE-FX	RO	This is a self-clearing bit. 1 = Far end fault in 100BASE-FX detected.	0
5:0	Reserved	RO		

4.3.3 SerDes MAC/Media Control

Register 17E, which is accessible only when extended register access is enabled, controls the transmitter and receiver of the device SerDes MAC/Media. The following table shows the settings available.

Table 42 • **SerDes MAC Control, Address 17E (0x11)**

Bit	Name	Access	Description	Default
15:10	Reserved	RO		
9	SerDes media receiver equalization	R/W	1 = Receiver equalization enabled.	0
8	SerDes MAC receiver equalization	R/W	1 = Receiver equalization enabled.	0
7:5	SerDes media output swing control	R/W	This is a sticky bit. 000 = 400 mV (peak-to-peak). 001 = 600 mV (peak-to-peak). 010 = 800 mV (peak-to-peak). 011 = 1000 mV (peak-to-peak). 100 = 1200 mV (peak-to-peak). 101 = 1400 mV (peak-to-peak). 110 and 111 = Reserved.	100
4:2	SerDes MAC output swing control	R/W	This is a sticky bit. 000 = 400 mV (peak-to-peak). 001 = 600 mV (peak-to-peak). 010 = 800 mV (peak-to-peak). 011 = 1000 mV (peak-to-peak). 100 = 1200 mV (peak-to-peak). 101 = 1400 mV (peak-to-peak). 110 and 111 = Reserved.	100
1	SerDes MAC hysteresis	R/W	1 = Disabled.	0
0	SerDes media hysteresis	R/W	1 = Disabled.	0

4.3.4 CRC Good Counter

Register 18E makes it possible to read the contents of the CRC good counter; the number of CRC routines that have executed successfully. The following table shows the readouts you can expect.

Table 43 • **CRC Good Counter, Address 18E (0x12)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	This is a self-clearing bit. 1 = Packet received since last read.	0
14	Reserved	RO		
13:0	CRC good counter contents	RO	This is a self-clearing bit. Counter containing the number of packets with valid CRCs; this counter does not saturate and will roll over.	0x000

4.3.5 SerDes Loopback and SIGDET Control

Register 19E controls the SerDes loopback and SIGDET pin polarity, as well as the extended LED modes. The following table shows the settings available.

Table 44 • **SerDes Loopback and SIGDET Control, Address 19E (0x13)**

Bit	Name	Access	Description	Default
15	LED3 Extended Mode	R/W	1 = See Extended LED Modes, page 19 for more information.	0
14	LED2 Extended Mode	R/W	1 = See Extended LED Modes, page 19 for more information.	0
13	LED1 Extended Mode	R/W	1 = See Extended LED Modes, page 19 for more information.	0
12	LED0 Extended Mode	R/W	1 = See Extended LED Modes, page 19 for more information.	0
11	LED Reset Blink Suppress	R/W	1 = Blink LEDs after reset de-asserted. 0 = Suppress LED blink after reset de-asserted. **Note:** There is a design guideline related to this feature. For more information, see Enabling LED Blinking After Reset, page 96.	CMODE
10	SerDes media loopback enable	R/W	1 = Enables SerDes media loopback based on SerDes media loopback mode setting. If this bit is set, the loopback controls for far-end loopback (register 23.3) and isolate (register 0.10) are disabled. 0 = Normal SerDes operation.	0
9:8	SerDes media loopback mode	R/W	00 = Pad loopback. 01 = SerDes serial loopback. 10 = SerDes parallel loopback. 11 = Normal data operation, but with recovered clock as SerDes transmit clock.	00
7	SerDes MAC loopback enable	R/W	1 = Enables SerDes MAC loopback based on the SerDes MAC loopback mode setting. If this bit is set, the loopback controls for far-end loopback (register 23.3) and isolate (Register 0.10) are disabled. 0 = Normal SerDes operation.	0
6:5	SerDes MAC loopback mode	R/W	00 = Pad loopback. 01 = SerDes serial loopback. 10 = SerDes parallel loopback. 11 = Normal data operation, but with recovered clock as SerDes transmit clock.	00
4	Fast link failure indication	R/W	1 = Enabled. 0 = Disabled. GPIO9 pin becomes general purpose I/O.	0
3:2	Force MDI crossover	R/W	00 = Normal MDI/MDI-X operation. 01 = Reserved. 10 = Copper media forced to MDI. 11 = Copper media forced MDI-X.	00

Table 44 • **SerDes Loopback and SIGDET Control, Address 19E (0x13) *(continued)***

Bit	Name	Access	Description	Default
1	Reserved	RO		
0	SIGDET pin polarity	R/W	This is a sticky bit. 1 = Active low. 0 = Active high.	CMODE

4.3.6 ActiPHY Control

Register 20E controls the device ActiPHY sleep timer, its wake-up timer, the frequency of the CLKOUT signal, and its link speed downshifting feature. The following table shows the settings available.

Table 45 • **Extended PHY Control 3, Address 20E (0x14)**

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1 = Disable carrier extension in SGMII 1000BASE-T copper links. Also, adjust SGMII MAC support from v1.7 (default) to v1.8.	0
14:13	ActiPHY sleep timer	R/W	This is a sticky bit. 00 = 1 second. 01 = 2 seconds. 10 = 3 seconds. 11 = 4 seconds.	01
12:11	ActiPHY wake-up timer	R/W	This is a sticky bit. 00 = 160 ms. 01 = 400 ms. 10 = 800 ms. 11 = 2 seconds.	11
10	Reserved	RO		
9	PHY address reversal	R/W	1 = Enabled.	CMODE
8	CLKOUT frequency	R/W	This is a sticky bit. 1 = 156.25 MHz. 0 = 125 MHz.	CMODE
7:6	Media mode status	RO	00 = No media selected. 01 = Copper media selected. 10 = SerDes media selected. 11 = Reserved.	00
5	Enable 10BASE-T no preamble mode	R/W	This is a sticky bit. 1 = 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it.	0
4	Enable link speed auto-downshift feature	R/W	This is a sticky bit. 1 = Enable auto link speed downshift from 1000BASE-T.	CMODE

Table 45 • **Extended PHY Control 3, Address 20E (0x14) *(continued)***

Bit	Name	Access	Description	Default
3:2	Link speed auto-downshift control	R/W	This is a sticky bit. 00 = Downshift after 2 failed 1000BASE-T auto-negotiation attempts. 01 = Downshift after 3 failed 1000BASE-T auto-negotiation attempts. 10 = Downshift after 4 failed 1000BASE-T auto-negotiation attempts. 11 = Downshift after 5 failed 1000BASE-T auto-negotiation attempts.	01
1	Link speed auto-downshift status	RO	0 = No downshift. 1 = Downshift is required or has occurred.	0
0	Reserved	RO		

Note: Bit 8 is valid only on PHY_0.

4.3.7 PoE and Miscellaneous Functionality

The register at address 23E controls various aspects of inline powering and the CRC error counter in the VSC8662.

Table 46 • **Extended PHY Control 4, Address 23E (0x17)**

Bit	Name	Access	Description	Default
15:11	PHY address	RO	PHY address; latched on reset.	CMODE
10	Inline powered device detection	R/W	This is a sticky bit. 1 = Enabled.	0
9:8	Inline powered device detection status	RO	00 = Searching for devices. 01 = Device found; requires inline power. 10 = Device found; does not require inline power. 11 = Reserved.	00
7:0	CRC error counter	RO	This is a self-clearing bit. CRC error counter for the Ethernet packet generator. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

Note: Bits 9:8 are only valid if bit 10 is set.

4.3.8 VeriPHY Control 1

Register 24E in the extended register space provides control over the device VeriPHY diagnostics features. There are three separate VeriPHY control registers. The following table shows the settings available and describes the readouts you can expect.

Table 47 • **VeriPHY Control Register 1, Address 24E (0x18)**

Bit	Name	Access	Description	Default
15	VeriPHY trigger	R/W	This is a self-clearing bit. 1 = Triggers the VeriPHY algorithm and clears when VeriPHY has completed. Settings in registers 24E through 26E become valid after this bit clears.	0

Table 47 • **VeriPHY Control Register 1, Address 24E (0x18) *(continued)***

Bit	Name	Access	Description	Default
14	VeriPHY valid	RO	1 = VeriPHY results in registers 24E through 26E are valid.	0
13:8	Pair A (1-2) distance	RO	Loop length or distance to anomaly for pair A (1-2).	0x00
7:6	Reserved	RO		
5:0	Pair B (3-6) distance	RO	Loop length or distance to anomaly for pair B (3-6).	0x00

Note: The resolution of the 6-bit length field is 3 meters.

4.3.9 VeriPHY Control 2

The register at address 25E consists of the second of the three device registers that provide control over VeriPHY diagnostics features. The following table shows the readouts you can expect.

Table 48 • **VeriPHY Control Register 2, Address 25E (0x19)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO		
13:8	Pair C (4-5) distance	RO	Loop length or distance to anomaly for pair C (4 and 5)	0x00
7:6	Reserved	RO		
5:0	Pair D (7-8) distance	RO	Loop length or distance to anomaly for pair D (7 and 8)	0x00

Note: The resolution of the 6-bit length field is 3 meters.

4.3.10 VeriPHY Control 3

The register at address 26E consists of the third of the three device registers that provide control over VeriPHY diagnostics features. Specifically, this register provides information about the termination status (fault condition) for all four link partner pairs. The following table shows the readouts you can expect.

Table 49 • **VeriPHY Control Register 3, Address 26E (0x1A)**

Bit	Name	Access	Description	Default
15:12	Pair A (1 and 2) termination status	RO	Termination fault for pair A (1 and 2)	0x00
11:8	Pair B (3 and 6) termination status	RO	Termination fault for pair B (3 and 4)	0x00
7:4	Pair C (4 and 5) termination status	RO	Termination fault for pair C (4 and 5)	0x00
3:0	Pair D (7 and 8) termination status	RO	Termination fault for pair D (7 and 8)	0x00

The following table shows the meanings for the various fault codes.

Table 50 • **VeriPHY Control Register 3 Fault Codes**

Code	Denotes
0000	Correctly terminated pair

Table 50 • **VeriPHY Control Register 3 Fault Codes *(continued)***

Code	Denotes
0001	Open pair
0010	Shorted pair
0100	Abnormal termination
1000	Cross-pair short to pair A
1001	Cross-pair short to pair B
1010	Cross-pair short to pair C
1011	Cross-pair short to pair D
1100	Abnormal cross-pair coupling with pair A
1101	Abnormal cross-pair coupling with pair B
1110	Abnormal cross-pair coupling with pair C
1111	Abnormal cross-pair coupling with pair D

4.3.11 SerDes MAC/Media Status

Register 28E in the extended register space provides access to the status of the SerDes MAC/Media. The following table shows the status available.

Table 51 • **SerDes MAC Status, Address 28E (0x1C)**

Bit	Name	Access	Description	Default
15:12	Reserved	RO		0000
11	MAC sync status fail	RO	This is a self-clearing bit. 1 = MAC Clause 36 synchronization state machine enters the LOSS_OF_SYNC state.	0
10	MAC cgbad	RO	This is a self-clearing bit. 1 = Clause 36 cgbad variable is true.	0
9	MAC phase lock loss	RO	This is a self-clearing bit. 1 = A comma re-alignment occurred.	0
8	MAC RxPLL lock loss	RO	This is a self-clearing bit. 1 = RxPLL loss of lock occurred.	0
7:4	Reserved	RO		
3	SerDes media sync status fail	RO	This is a self-clearing bit. 1 = SerDes Media Clause 36 synchronization state machine enters the LOSS_OF_SYNC state.	0
2	SerDes media cgbad	RO	This is a self-clearing bit. 1 = Clause 36 cgbad variable is true.	0
1	SerDes media phase lock loss	RO	This is a self-clearing bit. 1 = A comma re-alignment occurred.	0
0	SerDes media RxPLL lock loss	RO	This is a self-clearing bit. 1 = RxPLL loss of lock occurred.	0

4.3.12 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two, separate EPG control registers. The following table shows the setting available in the first register.

Table 52 • **EPG Control Register 1, Address 29E (0x1D)**

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1 = Enable EPG	0
14	EPG run or stop	R/W	1 = Run EPG	0
13	Transmission duration	R/W	1 = Continuous (sends in 10,000-packet increments) 0 = Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (Jumbo packet)	0
10	Inter-packet gap	R/W	1 = 8,192 ns 0 = 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte destination address	0000
1	Payload type	R/W	1 = Randomly generated payload pattern 0 = Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8662 device is connected to a live network.
- Bit 29E.13 (Continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The six-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The six-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.13 Ethernet Packet Generator Control 2

The register at address 30E consists of the second of bits that provide access to and control over various aspects of the EPG testing feature. For information about the first set of EPG control bits, see Table 52, page 57. The following table shows the settings available.

Table 53 • **EPG Control Register 2, Address 30E (0x1E)**

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E is set to 1), that bit (29E.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 General-Purpose I/O Registers

Accessing the GPIO page register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the GPIO page register space.

To restore main register page access, write 0x0000 to register 31.

The following table lists the addresses and register names in the GPIO register page space. These registers are accessible only when the device register 31 is set to 0x0010.

Table 54 • **General-Purpose Registers Page Space**

Register Address	Register Name
0G through 12G	Reserved
13G	SIGDET vs. GPIO control
14G	Reserved
15G	GPIO input
16G	GPIO output
17G	GPIO output enable
18G	Reserved
19G	Fast link fail control
20G	I2C mux control 1
21G	I2C mux control 2
22G	I2C mux data read/write
23G	Recovered clock 1
24G	Recovered clock 2
25G	LED port swapping
26G through 30G	Reserved

4.4.1 Reserved GPIO Address Space

The bits in registers 0G to 12G, and 14G of the GPIO register page space are reserved.

4.4.2 SIGDET vs. GPIO Control

The SIGDET control register configures GPIO pins 3:0 to be either SIGDET pins for each port or to be GPIO pins. The following table shows the values that can be written.

Table 55 • **SIGDET vs. GPIO Control, Address 13G (0x0D)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO		
7:4	Reserved	R/W		
3:2	SIGDET1 control	R/W	00 = Normal SIGDET operation 01, 10 = Reserved 11 = Controlled by MII registers 15G to 17G	00

Table 55 • **SIGDET vs. GPIO Control, Address 13G (0x0D) *(continued)***

Bit	Name	Access	Description	Default
1:0	SIGDET0 control	R/W	00 = Normal SIGDET operation 01, 10 = Reserved 11 = Controlled by MII registers 15G to 17G	00

4.4.3 GPIO Input

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

Table 56 • **GPIO Input, Address 15G (0x0F)**

Bit	Name	Access	Description	Default
15:0	GPIO [15:0] input	RO	Data read from the GPIO pins	0x00

4.4.4 GPIO Output

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

Table 57 • **GPIO Output, Address 16G (0x10)**

Bit	Name	Access	Description	Default
15:0	GPIO [15:0] output	R/W	Data written to the GPIO pins	0x00

4.4.5 GPIO Pin Configuration

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

Table 58 • **GPIO Input/Output Configuration, Address 17G (0x11)**

Bit	Name	Access	Description	Default
15:0	GPIO [15:0] input or output enable	R/W	1 = Pin is configured as an output. 0 = Pin is configured as an input.	0x00

4.4.6 Fast Link Fail Control

Register 19G in the GPIO register space controls the output of the fast link failure. The following table shows the settings available for the GPIO9 pin when enabled by register 19E, bit 4.

Table 59 • **GPIO Input/Output Configuration, Address 19G (0x13)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO		
0	Fast link failure port setting	R/W	0 = PHY0 1 = PHY1	00

4.4.7 Two-Wire Serial Mux Control 1

The following table shows the settings available to control the integrated two-wire serial mux.

Table 60 • **Two-Wire Serial Mux Control 1, Address 20G (0x14)**

Bit	Name	Access	Description	Default
15:9	I2C device address	R/W	Top 7 bits of the 8-bit address sent out on the two wire serial stream. The bottom bit is the read/write signal, which is controlled by register 21G, bit 8. SFPs use 0xA0.	0xA0
8:6	Reserved	RO		
5:4	I2C SCL clock frequency	R/W	00 = 50 kHz. 01 = 100 kHz. 10 = 400 kHz. 11 = 2 MHz.	01
3:2	Reserved	R/W		
1	I2C mux port 1 enable	R/W	1 = Enabled. 0 = I2C disabled. Becomes GPIO pin.	0
0	I2C mux port 0 enable	R/W	1 = Enabled. 0 = I2C disabled. Becomes GPIO pin.	0

4.4.8 Two-Wire Serial Mux Control 2

Register 21G is used to control the two-wire serial mux for status and control of two-wire serial slave devices.

Table 61 • **Two-Wire Serial Mux Interface Status and Control, Address 21G (0x15)**

Bit	Name	Access	Description	Default
15	I2C mux ready	RO	1 = I2C mux is ready for read or write.	1
14:12	Reserved	RO		
11	Reserved	R/W		
10	PHY port Address	R/W	Specific VSC8662 PHY port being addressed.	0
9	Enable I2C mux access	R/W	This is a self-clearing bit. 1 = Execute read or write through the I2C mux based on the settings of register bit 21G.8.	0
8	I2C mux read or write	R/W	1 = Read from I2C mux. 0 = Write to I2C mux.	1
7:0	I2C mux address	R/W	Sets the address of the I2C mux used to direct read or write operations.	0x00

4.4.9 Two-Wire Serial Mux Data Read/Write

Register 22G in the extended register space enables access to the two-wire serial mux.

Table 62 • **Two-Wire Serial Mux Data Read/Write, Address 22G (0x16)**

Bit	Name	Access	Description	Default
15:8	I2C mux read data	RO	8-bit data read from I2C mux; requires setting both register 21G.9 and 21G.8 to 1.	0x00
7:0	I2C mux write data	R/W	8-bit data to be written to I2C mux.	0x00

4.4.10 Recovered Clock 1

The following table shows the settings available to control the RCVRD_CLK1 pin.

Table 63 • **Recovered Clock 1, Address 23G (0x17)**

Bit	Name	Access	Description	Default
15	RCVRD_CLK1 enable	R/W	1 = Enabled 0 = Disabled **Note:** There is a design guideline related to this feature. For more information, see Disabling Recovered Clock Output, page 100.	0
14	Reserved	RO		
13	Reserved	R/W		
12	PHY clockout select	R/W	0 = PHY0 1 = PHY1	00
11:9	Reserved	RO		
8	Clock frequency	R/W	0 = 25 MHz 1 = 125 MHz	0
7:6	Reserved	RO		
5:4	Clock squelch	R/W	See Table 65, page 62	00
3:2	Reserved	RO		
1:0	Clock select	R/W	00 = SerDes media 01 = Copper media 10 = Transmitter TCLK output 11 = Local XTAL1/REFCLK input	00

4.4.11 Recovered Clock 2

The following table shows the settings available to control the RCVRD_CLK2 pin.

Table 64 • **Recovered Clock 2, Address 24G (0x18)**

Bit	Name	Access	Description	Default
15	RCVRD_CLK2 enable	R/W	1 = Enabled 0 = Disabled **Note:** There is a design guideline related to this feature. For more information, see Disabling Recovered Clock Output, page 100.	0
14	Reserved	RO		
13	Reserved	R/W		
12	PHY clockout select	R/W	0 = PHY0 1 = PHY1	0
11:9	Reserved	RO		
8	Clock frequency	R/W	0 = 25 MHz 1 = 125 MHz	0
7:6	Reserved	RO		
5:4	Clock squelch	R/W	See Table 65, page 62	00
3:2	Reserved	RO		
1:0	Clock select	R/W	00 = SerDes media 01 = Copper media 10 = Reserved 11 = Local XTAL1/REFCLK input	00

The following table shows the clock squelch modes that can be programmed into the RCVRD_CLK1 and RCVRD_CLK2 pins.

Table 65 • **Available Clock Squelch Settings**

Bit Setting	Clock Squelch Setting
00	Squelch recovered clock pin to low when: • No link is detected (the link status register 1, bit 2 = 0). • A fast link failure is detected (GPIO9 pin is asserted high). • Active link is in 10BASE-T or 1000BASE-T master mode (unreliable recovered clock).
01	Squelch recovered clock pin to low when: • No link is detected (the link status register 1, bit 2 = 0). • A fast link failure is detected (GPIO9 pin is asserted high).
10	Squelch recovered clock pin to low when: No link is detected (the link status register 1, bit 2 = 0).
11	Squelch disabled. **Note:** Random clocks may appear on the clock out pin during auto-negotiation and when the link is not active. As a result, the clock might transition to the REFCLK input instead of the recovered clock.

4.4.12 LED Port Swapping

The following table shows the settings to swap the PHY port LEDs.

Table 66 • **LED Port Swapping, Address 25G (0x19)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO		
1	Reserved	R/W		
0	LED port swapping	R/W	See Table 7, page 21	0

4.5 CMODE

The information in this section provides a detailed description of the methods you can use to configure the VSC8662 device using its CMODE pins. It includes descriptions of the registers that work together with the CMODE pins to control the device function.

There are eight configuration mode (CMODE) pins on the VSC8662 device. For more information about the CMODE pin locations, see Miscellaneous Pins, page 82. Each of the CMODE pins maps to four configuration bits, which means that each pin controls 16 possible settings for the device.

4.5.1 CMODE Pins and Related Functions

The following table lists the pin numbers and device functionality that are controlled by each configuration bit.

Table 67 • **CMODE Configuration Pins and Device Functions**

CMODE Pin	Bit 3 (MSB) Control	Bit 2 Controls	Bit 1 Controls	Bit 0 (LSB) Controls
7	Reserved Always set to logic 0	Link speed downshift	Speed and duplex [1]	Speed and duplex [0]
6	MAC auto-negotiation	ActiPHY	Advertise asymmetric pause	Advertise symmetric pause
5	Media interface [2]	Reserved Always set to logic 0	CLKOUT speed 125 MHz or 156.25 MHz selection	CLKOUT enable
4	Media interface [1]	SIGDET polarity	PHY address reversal	LED fiber/copper combine
3	Media interface [0]	LED3 combine or separate	LED3 [1]	LED3 [0]
2	PHY address [4]	LED2 combine or separate	LED2 [1]	LED2 [0]
1	PHY address [3]	LED1 combine or separate	LED1 [1]	LED1 [0]
0	PHY address [2]	LED0 combine or separate	LED0 [1]	LED0 [0]

4.5.2 Functions and Related CMODE Pins

The following table lists the pin and bit settings according to the device function and CMODE pin used to configure them.

Table 68 • **Device Functions and Associated CMODE Pins**

Function	Sets MII Register	CMODE Pin	Bit	Description
Link speed downshift	Register 20E, bit 4	7	2	0 = Link only according to the auto-negotiation resolution. 1 = Enable link speed downshift feature.
Speed and duplex	Register 4, bits 8:5 and register 9, bits 9:8	7	1 and 0	00 = 10/100/1000BASE-T FDX/HDX. 1000BASE-X/100BASE-FX FDX/HDX. 01 = 10/100/1000BASE-T FDX; 10/100BASE-T HDX. 1000BASE-X FDX; 100BASE-FX HDX/FDX. 10 = 1000BASE-T FDX only. 11 = 10/100BASE-T FDX/HDX.
MAC auto-negotiation	Register 23, bit 13	6	3	0 = Disabled. 1 = Enabled.
ActiPHY	Register 28, bit 6	6	2	0 = Disabled. 1 = Enabled.
Advertise asymmetric pause	Register 4, bit 11	6	1	0 = Not advertised. 1 = Advertised.
Advertise symmetric pause	Register 4, bit 10	6	0	0 = Not advertised. 1 = Advertised.
Media interface [2:0]	Register 23, bits 10:8	5, 4, 3	3	000 = Cat5 copper only. 001 = SerDes Fiber/SFP Pass-Through mode only. No auto-negotiation performed in the PHY. 010 = 1000BASE-X Fiber/SFP mode only with auto-negotiation performed by the PHY. 011 = 100BASE-X Fiber/SFP mode on the fiber media pins only. 101 = Auto-media sense with Cat5 media or SerDes Fiber/SFP Pass-Through mode. 110 = Auto-media sense with Cat5 media or 1000BASE-X Fiber/SFP mode with auto-negotiation performed by PHY. 111 = Auto-media sense with Cat5 media or 100BASE-FX Fiber/SFP mode. 100 = Reserved.
CLKOUT speed	Register 20E, bit 8	5	1	0 = 125 MHz 1 = 156.25 MHz
CLKOUT enable	Register 18, bit 0	5	0	0 = Disabled. 1 = Enabled.
SIGDET polarity	Register 19E, bit 0	4	2	0 = Active high. 1 = Active low.
Address reversal		4	1	0 = Normal functioning. PHY address 0:1 = Port 0:1. 1 = Reversed functioning. PHY address 1:0 = Port 0:1.
LED fiber/copper combine	Register 30, bit 15	4	0	0 = Combine enabled (Copper/Fiber on Link/LinkXXXX(1)/Activity LED). 1 = Disable combination (Link/LinkXXXX/Activity LED indicates copper only).

Table 68 • **Device Functions and Associated CMODE Pins *(continued)***

Function	Sets MII Register	CMODE Pin	Bit	Description
LED_3, LED_2, LED_1, and LED_0 combine or separate	Register 30, bits 3:0	3, 2, 1, and 0	2	0 = Link, Link10, Link100, Link1000, Link10/100, Link10/1000, Link100/1000. LEDs blink or flash when activity is present. Also, a duplex LED blinks or flashes when collision is present. 1 = Link, Link10, Link100, Link1000, Link10/100, Link10/1000, Link100/1000. LEDs indicate status only. Also, a duplex LED indicates a duplex status only.
PHY address [4:2]		2, 1, 0	3	Sets the three MSBs of the PHY address.
LED_3 indication function	Register 29, bits 15:12	3	1 and 0	00 = Duplex or collision. 01 = Link100 or activity. 10 = Activity. 11 = Fiber_Link/Fiber_Activity.
LED_2 indication function	Register 29, bits 11:8	2	1 and 0	00 = Link or activity. 01 = Duplex or collision. 10 = Fiber_Activity. 11 = Link10 or activity.
LED_1 indication function	Register 29, bits 7:4	1	1 and 0	00 = Link100 or activity. 01 = Link100/1000 or activity. 10 = Link 10/100 or activity. 11 = Fiber_Link/Fiber_Activity.
LED_0 indication function	Register 29, bits 3:0	0	1 and 0	00 = Link1000 or activity. 01 = Link100/1000 or activity. 10 = Activity. 11 = Link or activity.

1. Link10, Link100, Link1000, Link10/100, Link100/1000, Link1000BASE-X, or Link1000BASE-FX.

Note: The MAC auto-negotiation, LED_0, LED_1, LED_2, and LED_3 settings available using the CMODE pins and configuration bits is limited. For full functionality, use the registers. For more information about using the registers for these and other functions, see Registers, page 28.

4.5.3 CMODE Resistor Values

To affect an aspect of the VSC8662 device configuration, find the parameter in Table 67, page 63 or in Table 68, page 64, and connect the associated pin to the resistor specified in the following table. This sets the bits as shown.

Table 69 • **CMODE Resistor Values and Resultant Bit Settings**

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VSS	0	0	0	0	0
VSS	2.26 kΩ	0	0	0	1
VSS	4.02 kΩ	0	0	1	0
VSS	5.90 kΩ	0	0	1	1
VSS	8.25 kΩ	0	1	0	0
VSS	12.1 kΩ	0	1	0	1
VSS	16.9 kΩ	0	1	1	0

Table 69 • **CMODE Resistor Values and Resultant Bit Settings *(continued)***

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VSS	22.6 kΩ	0	1	1	1
VDD33	0	1	0	0	0
VDD33	2.26 kΩ	1	0	0	1
VDD33	4.02 kΩ	1	0	1	0
VDD33	5.90 kΩ	1	0	1	1
VDD33	8.25 kΩ	1	1	0	0
VDD33	12.1 kΩ	1	1	0	1
VDD33	16.9 kΩ	1	1	1	0
VDD33	22.6 kΩ	1	1	1	1

Using resistors with the CMODE pins can be optional in designs that access the device's MDC/MDIO pins. In designs that do this, all configurations otherwise affected on the device by using the CMODE pins can be changed using the regular device register settings, and all the CMODE pins can be pulled to VSS (ground). However, in this case, the PHYADDR [4:2] and the PHYADD_REVERSAL settings still require CMODE configuration. This configuration can be set by connecting these pins to either the VDD33 or VSS pins.

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8662 device. It includes information on the various timing functions of the device.

5.1 DC Characteristics

In addition to any parameter-specific conditions, the specifications listed in the following tables may be considered valid only in the environment characterized by the specifications listed as recommended operating conditions for the VSC8662 device. For more information about the recommended operating conditions, see Operating Conditions, page 77.

5.1.1 VDDIO at 3.3 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 3.3 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 70 • **DC Characteristics for Pins Referenced to VDDIO at 3.3 V**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4 mA
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.1.2 VDDIO at 2.5 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 2.5 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 71 • **DC Characteristics for Pins Referenced to VDDIO at 2.5 V**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0	2.8	V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 1.0 mA

Table 71 • **DC Characteristics for Pins Referenced to VDDIO at 2.5 V *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input high voltage	V_{IH}	1.7	3.0	V	
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current	I_{ILEAK}	–32	32	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–32	32	µA	Internal resistor included
Output low current drive strength	I_{OL}		6	mA	
Output high current drive strength	I_{OH}	–6		mA	

5.1.3 VDDIO at 1.8 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 1.8 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 72 • **DC Characteristics for Pins Referenced to VDDIO at 1.8 V**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	1.4	2.1	V	I_{OH} = –0.5 mA
Output low voltage	V_{OL}		0.3	V	I_{OL} = 0.5 mA
Input high voltage	V_{IH}	1.2	2.1	V	
Input low voltage	V_{IL}		0.6	V	
Input leakage current	I_{ILEAK}	–23	23	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–23	23	µA	Internal resistor included
Output low current drive strength	I_{OL}		4.0	mA	
Output high current drive strength	I_{OH}	–4.0		mA	

5.1.4 VDD33 at 3.3 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 3.3 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 73 • **DC Characteristics for Pins Referenced to VDD33 at 3.30 V**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4 mA

Table 73 • **DC Characteristics for Pins Referenced to VDD33 at 3.30 V *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.1.5 DC Characteristics for MAC and SerDes Media Outputs

For more information about the MAC output pins, see SerDes MAC Interface, page 84. For more information about the SerDes media output pins, see SerDes Media Interface, page 85. For more information about the AC characteristics, see AC Characteristics for MAC and SerDes Media Outputs, page 73.

Table 74 • **DC Characteristics for MAC_RDP/N_*n* and FIBR_DOP/N_*n* Pins**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Frequency lock time	T_{LOCK}		500		µs	
Output differential voltage	V_{ODIFF}	700	1000	1200	mV	Measured peak-to-peak. Based on 100 Ω differential load.
Output common-mode voltage	V_{OCM}	480	540	610	mV	V_{DD12A} = 1.20 V.
Output low current drive strength	I_{OL}			8	mA	
Output high current drive strength	I_{OH}	–8			mA	
Output driver impedance per pin	Z_O		50		Ω	

5.1.6 DC Characteristics for MAC and SerDes Media Inputs

For more information about the MAC input pins, see SerDes MAC Interface, page 84. For more information about the SerDes media input pins, see SerDes Media Interface, page 85. For more information about the AC characteristics, see AC Characteristics for MAC and SerDes Media Inputs, page 73.

Table 75 • **DC Characteristics for MAC_TDP/N_*n* and FIBR_DIP/N_*n* Pins**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input differential voltage	V_{IDIFF}	120	2400	mV	Measured peak-to-peak. Based on 100 Ω differential load.
Input common mode voltage	V_{ICM}	0.4	1.3	V	V_{DD12A} = 1.20 V.

5.1.7 LED Pins

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 3.3 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 76 • **DC Characteristics for LED[3:0]_*n* Pins**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4.0 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4.0 mA
Output leakage current	I_{OLEAK}	–10	10	µA	
Output low current drive strength	I_{OL}		8.0	mA	
Output high current drive strength	I_{OH}	–8.0		mA	

5.1.8 JTAG Pins

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when:

- V_{DDIO} is 3.3 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V

Table 77 • **DC Characteristics for JTAG Pins**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –1.5 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 1.5 mA
Input high voltage	V_{IH}	2.1	3.6	V	
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–42	42	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–42	42	µA	Internal resistor included
Output low current drive strength	I_{OL}		8	mA	
Output high current drive strength	I_{OH}	–8		mA	

5.2 Current Consumption

There are three sets of current consumption values:

- Typical current consumption
- Current consumption in SerDes/SGMII to 1000BASE-X mode
- Current consumption in SerDes/SGMII to 100BASE-FX mode or SerDes pass-through mode

The typical current consumption values are based on nominal voltages with all ports operating at 1000BASE-T speeds with full-duplex enabled and a 64-bit random data pattern at 100% utilization.

Table 78 • **Typical Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		3.19	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33} at 3.3 V	I_{VDD33}	228		mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	390		mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	224		mA

If all ports are running in SerDes/SGMII to 1000BASE-X mode, the current consumption values are shown in the following table.

Table 79 • **Current Consumption in SerDes/SGMII to 1000BASE-X Mode**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption(1)	P_D		0.57	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33} at 3.3 V	I_{VDD33}	38		mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	58		mA
Current with V_{DD12A} at 1.2V	I_{VDD12A}	238		mA

1. Worst-case power only applies if the 1000BASE-X media operating mode is set by CMODE configuration. When any Cat5 media operating mode is selected using CMODE, the worst-case power consumption in the preceding table applies. For information, see Table 78, page 71.

If all ports are running in SerDes/SGMII to 100BASE-FX mode or SerDes pass-through mode, the current consumption values are as shown in the following table.

Table 80 • **Consumption in SerDes/SGMII to 100BASE-FX or SerDes Pass-Through Mode**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption(1)	P_D		0.59	W
Current with V_{DDIO} at 1.8 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 2.5 V	I_{VDDIO}	1		mA
Current with V_{DDIO} at 3.3 V	I_{VDDIO}	1		mA
Current with V_{DD33}	I_{VDD33}	34		mA
Current with V_{DD12}	I_{VDD12}	49		mA
Current with V_{DD12A}	I_{VDD12A}	202		mA

1. Worst-case power only applies if the 100BASE-FX media operating mode is set by CMODE configuration. When any Cat5 media operating mode is selected using CMODE, the worst-case power consumption listed earlier in this section applies. For information, see Table 78, page 71.

5.3 AC Characteristics

The AC specifications are grouped according to specific device pins and associated timing characteristics.

5.3.1 Reference Clock Input

The following table shows the specifications for the reference clock input frequency including various frequencies, duty cycle, and accuracy.

Table 81 • **AC Characteristics for REFCLK Input**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Frequency with 25 MHz input	f_{CLK25}		25		MHz	
Frequency with 125 MHz input	f_{CLK125}		125		MHz	
Frequency accuracy	f_{TOL}			100	ppm	
Duty cycle	$\%_{DUTY}$	40		60	%	
RMS jitter tolerance(1)	J_{TOL}			145 42 42 55	ps ps ps ps	1 kHz 10 kHz 200 kHz 10 MHz
Rise time with 25 MHz input (20% to 80%)	t_{R25}			4	ns	
Rise time with 125 MHz input (20% to 80%)	t_{R125}			1	ns	
Fall time with 25 MHz input (20% to 80%)	t_{R25}			4	ns	
Fall time with 125 MHz input (20% to 80%)	t_{F125}			1	ns	

1. Sinusoidal jitter, with BER 10^{-12} divided by 14.1.

If using the 25 MHz crystal clock input option, the additional specifications in the following table are required.

Table 82 • **AC Characteristics for REFCLK Input with 25 MHz Clock Input**

Parameter	Minimum	Typical	Maximum	Unit
Crystal parallel load capacitance	18		20	pF
Crystal equivalent series resistance		10	30	Ω
Crystal accuracy			50	ppm

5.3.2 Clock Output

The specifications in the following table show the AC characteristics for the clock output of the VSC8662 device.

Table 83 • **AC Characteristics for the CLKOUT Pin**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
CLKOUT frequency	f_{CLK125} $f_{CLK156.25}$		125.00 156.25		MHz	125 MHz output clock 156.25 MHz output clock

Table 83 • **AC Characteristics for the CLKOUT Pin *(continued)***

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
CLKOUT cycle time	t_{CYC}		8.0 6.4		ns	125 MHz output clock 156.25 MHz output clock
Frequency stability	$f_{STABILITY}$			100	ppm	
Duty cycle	$\%_{DUTY}$	40	50	60	%	
Clock rise and fall times (20% to 80%)	t_R and t_F			425	ps	
Total jitter	J_{CLK}		100	150	ps	Measured peak-to-peak

5.3.3 Recovered Clock Outputs

The specifications in the following table show the AC characteristics for the recovered clock outputs of the VSC8662 device.

Table 84 • **AC Characteristics for the RCVRD_CLK Pins**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
RCVRD_CLK frequency	$f_{RCLK125}$		125.00 25.00		MHz	125 MHz output clock 25 MHz output clock
RCVRD_CLK cycle time	t_{RCYC}		8.0 40		ns	125 MHz output clock 25 MHz output clock
Frequency stability	$f_{STABILITY}$			50	ppm	
Duty cycle	$\%_{DUTY}$	45	50	55	%	
Clock rise and fall times (20% to 80%)	t_R and t_F			600	ps	
Total jitter for 1000BASE-T	J_{CLK}		325	400	ps	Measured peak-to-peak
Total jitter for SerDes	J_{CLK}		200	250	ps	Measured peak-to-peak

5.3.4 AC Characteristics for MAC and SerDes Media Outputs

For more information about the MAC output pins, see SerDes MAC Interface, page 84. For more information about the SerDes media output pins, see SerDes Media Interface, page 85. For more information about the DC characteristics, see DC Characteristics for MAC and SerDes Media Outputs, page 69.

Table 85 • **AC Characteristics for MAC_RDP/N_*n* and FIBR_DOP/N_*n* Pins**

Parameter	Symbol	Typical	Maximum	Unit	Condition
Output rise time and fall time (20% to 80%)	t_r , t_f		300	ps	
Total output jitter	T_J	185	260	ps	Measured peak-to-peak. Uses K28.5 test pattern. Bit error rate (BER) = 10^{-12}.

5.3.5 AC Characteristics for MAC and SerDes Media Inputs

For more information about the MAC input pins, see SerDes MAC Interface, page 84. For more information about the SerDes media input pins, see SerDes Media Interface, page 85. For more

information about the DC characteristics, see DC Characteristics for MAC and SerDes Media Inputs, page 69.

Table 86 • **AC Characteristics for MAC_TDP/N_*n* and FIBR_DIP/N_*n* Pins**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Total receive jitter tolerance	J_{RX}Total		610	ps	Measured peak-to-peak. 1000BASE-X mode.
	J_{RX}Total		6500	ps	Measured peak-to-peak. 100BASE-FX mode.

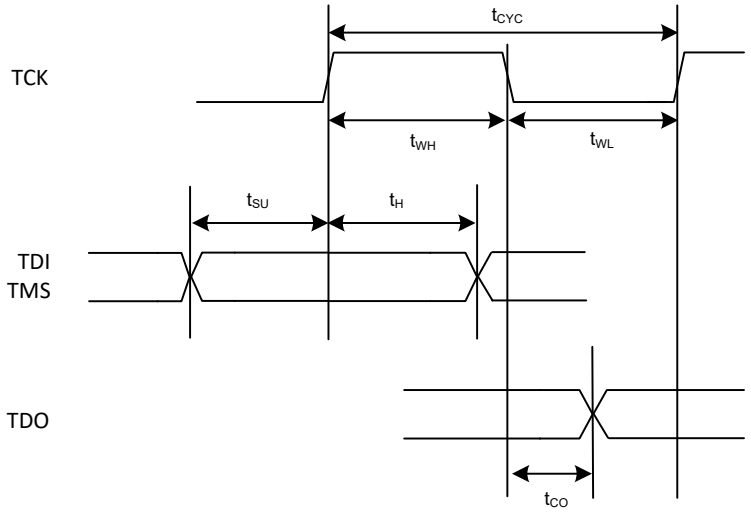
5.3.6 JTAG Interface

The following table lists the characteristics for the JTAG testing feature. The illustration provides a diagram of the timing.

Table 87 • **AC Characteristics for the JTAG Interface**

Parameter	Symbol	Minimum	Maximum	Unit
TCK frequency	f_{CLK}		10	MHz
TCK cycle time	t_{CYC}	100		ns
TCK time high	t_{WH}	45		ns
TCK time low	t_{WL}	45		ns
Setup time to TCK rising	t_{SU}	10		ns
Hold time from TCK rising	t_H	10		ns
TCK to TDO valid	t_{CO}		15	ns

Figure 21 • **JTAG Interface Timing**



5.3.7 SMI Interface

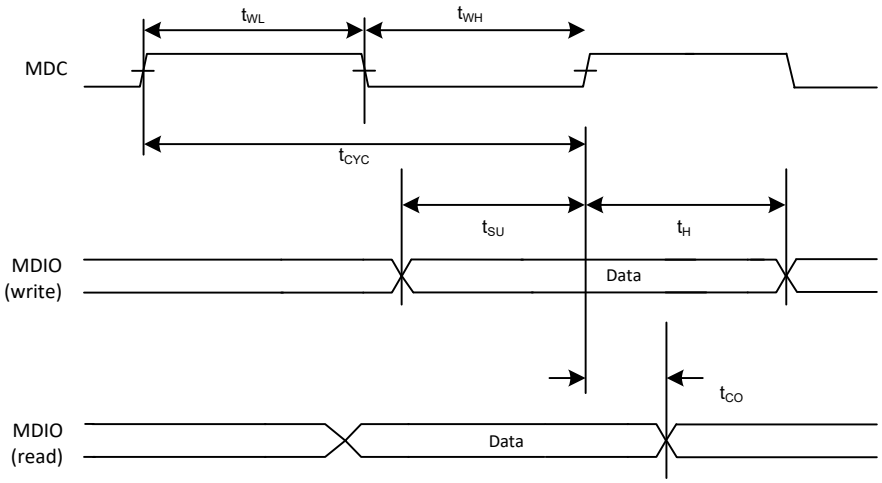
Use the information in the following table when incorporating the VSC8662 device SMI interface into your own design. The illustration provides information about SMI interface timing.

Table 88 • **AC Characteristics for the SMI Interface**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}		2.5	12.5	MHz	
MDC cycle time	t_{CYC}	80	400		ns	
MDC time high	t_{WH}	20	50		ns	
MDC time low	t_{WL}	20	50		ns	
Setup to MDC rising	t_{SU}	10			ns	
Hold from MDC rising	t_H	10			ns	
MDC rise time	t_R	100 t_{CYC} × 10%(1)			ns	For MDC = 0 – 1 MHz For MDC = 1 MHz – f_{CLK}(MAX)
MDC fall time	t_F	100 t_{CYC} × 10%(1)				
MDC to MDIO valid	t_{CO}		10	300	ns	Time-dependant on the value of the external pull-up resistor on the MDIO pin

1. For f_{CLK} above 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 22 • **SMI Interface Timing**



5.3.8 Device Reset

The following specifications apply to the device reset functionality. The illustration shows the reset timing.

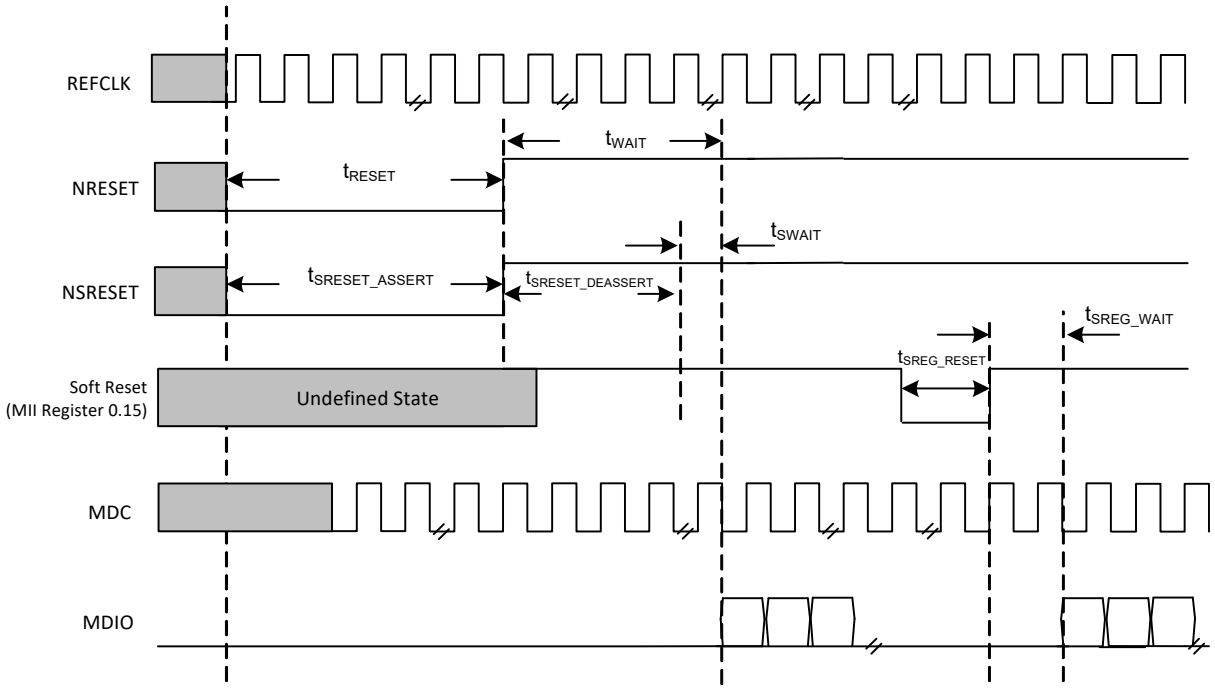
Table 89 • **AC Characteristics for Device Reset**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
NRESET assertion time	t_{RESET}	100		ns	
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	20		ms ms	

Table 89 • **AC Characteristics for Device Reset *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Soft reset (pin) assertion	t_{SRESET_ASSERT}	4		ms	
Soft reset (pin) de-assertion	$t_{SRESET\_DEASSERT}$	4		ms	
Wait time between soft reset pin de-assert and access of the SMI interface	t_{SWAIT}	4 300		µs µs	Registers 22.9 = 1 Registers 22.9 = 0
Soft reset MII register 0.15 assertion	t_{SREG_RESET}	100		ns	
Wait time between Soft Reset (MII Register 0.15) de-assert and access to the SMI interface	t_{SREG_WAIT}	4 300		µs µs	Registers 22.9 = 1 Registers 22.9 = 0

Figure 23 • **Reset Timing**



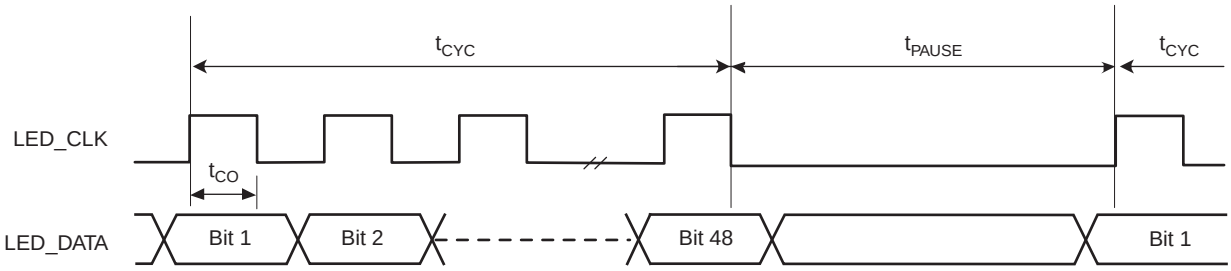
5.3.9 Serial LEDs

The following table provides specifications for the device serial LEDs. The illustration shows the LED timing. For information about initial synchronization requirements, see Serial LED Mode, page 20

Table 90 • **AC Characteristics for Serial LEDs**

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	1		µs
Pause between LED bit sequences	t_{PAUSE}	25		ms
LED_CLK to LED_DATA	t_{CO}		1	ns

Figure 24 • **Serial LED Timing**



5.4 Operating Conditions

The following table shows the recommended operating conditions for the VSC8662 device.

Table 91 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for V_{DDIO} at 1.8 V	V_{DDIO}	1.70	1.80	1.90	V
Power supply voltage for V_{DDIO} at 2.5 V	V_{DDIO}	2.37	2.50	2.63	V
Power supply voltage for V_{DDIO} at 3.3 V	V_{DDIO}	3.13	3.30	3.47	V
Power supply voltage for V_{DD33}	V_{DD33}	3.13	3.30	3.47	V
Power supply voltage for V_{DD12}	V_{DD12}	1.14	1.20	1.26	V
Power supply voltage for V_{DD12A}	V_{DD12A}	1.14	1.20	1.26	V
VSC8662 operating temperature(1)	T	0		90	°C
VSC8662-03 operating temperature(1)	T	–40		100	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

5.5 Stress Ratings

This section contains the stress ratings for the VSC8662 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 92 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
DC input voltage on V_{DDIO} supply pin	V_{DDIO}	–0.5	4.0	V
DC input voltage on V_{DD33} supply pin	V_{DD33}	–0.5	4.0	V
DC input voltage on V_{DD12} supply pin	V_{DD12}	–0.5	1.4	V
DC input voltage on V_{DD12A} supply pin	V_{DD12A}	–0.5	1.4	V
DC input voltage on JTAG 5 V-tolerant pins	V_{DD}(5 V)	–0.5	5.5	V
DC input voltage on any non-supply pin	V_{DD}(PIN)	–0.5	V_{DD} + 0.5	V
Storage temperature	T_S	–65	150	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–500	500	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8662 device has 256 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

6.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8662 device. For clarity, the device is shown in two halves, the top left and top right.

Figure 25 • **Pin Diagram, Top Left**

	1	2	3	4	5	6	7	8
A	NC	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
B	VSS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
C	XTAL2	VDD33	VSS	VDD33	VSS	VDD33	VDD12A	VDD12A
D	XTAL1/REFCLK	OSCEN	REF_FILT	REF_REXT	VSS	VSS	VSS	VSS
E	PLLMODE	TMS	NTRST	VDD33	VDD12	VSS	VSS	VSS
F	TDO	TDI	TCK	VSS	VDD12	VSS	VSS	VSS
G	LED0_0	LED1_0	LED2_0	LED3_0	VDD12	VSS	VSS	VSS
H	LED0_1	LED1_1	LED2_1	LED3_1	VDD12	VSS	VSS	VSS
J	RESERVED	RESERVED	RESERVED	RESERVED	VDD12	VSS	VSS	VSS
K	RESERVED	RESERVED	RESERVED	RESERVED	VDD12	VSS	VSS	VSS
L	RESERVED	RESERVED	NSRESET	VSS	VDD12	VSS	VSS	VSS
M	RESERVED	MDINT0	NRESET	VDDIO	VDD12	VSS	VSS	VSS
N	RESERVED	MDIO	MDINT1	RESERVED	VDD12	VSS	VSS	VSS
P	RESERVED	MDC	VDDIO	VSS	VDD33	VDD12A	VDD12A	VDD12A
R	VSS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
T	NC	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Figure 26 • **Pin Diagram, Top Right**

9	10	11	12	13	14	15	16	
RESERVED	TXVPA_1	TXVPB_1	TXVPC_1	TXVPD_1	TXVPA_0	TXVPB_0	NC	A
RESERVED	TXVNA_1	TXVNB_1	TXVNC_1	TXVND_1	TXVNA_0	TXVNB_0	VSS	B
VDD12A	RESERVED	VDD33	VSS	VDD12A	VDD33	TXVNC_0	TXVPC_0	C
VSS	VSS	VSS	VSS	RESERVED	CMODE5	TXVND_0	TXVPD_0	D
VSS	VSS	VSS	VDD12	RESERVED	CMODE4	CMODE6	CMODE7	E
VSS	VSS	VSS	VDD12	RESERVED	CMODE2	CMODE3	RCVRD_CLK1	F
VSS	VSS	VSS	VDD12	CMODE0	CMODE1	CLKOUT	RCVRD_CLK2	G
VSS	VSS	VSS	VDD12	VDD33	GPIO13	THERMDC	THERMDA	H
VSS	VSS	VSS	VDD12	VSS	GPIO12	GPIO14	GPIO15	J
VSS	VSS	VSS	VDD12	GPIO8/I2C_SDA	GPIO9/FastLinkFail	GPIO10	GPIO11	K
VSS	VSS	VSS	VDD12	GPIO4/I2C_SCL_0	GPIO5/I2C_SCL_1	GPIO6	GPIO7	L
VSS	VSS	VSS	VDD12	VDD33	GPIO1/SIGDET1	GPIO2	GPIO3	M
VSS	VSS	VSS	VDD12	VSS	GPIO0/SIGDET0	TDP_0	TDN_0	N
VDD12A	VDD12A	VDD12A	VDD33	VDD33	VSS	RDP_0	RDN_0	P
RESERVED	FIBR_DOP_1	FIBR_DIP_1	RDP_1	TDP_1	FIBR_DOP_0	FIBR_DIP_0	VSS	R
RESERVED	FIBR_DON_1	FIBR_DIN_1	RDN_1	TDN_1	FIBR_DON_0	FIBR_DIN_0	NC	T

6.2 Pin Identifications

This section contains the pin descriptions for the VSC8662 device. The following table provides notations for definitions of the various pin types.

Table 93 • **Pin Type Symbols**

Symbol	Pin Type	Description
I	Input	Input with no on-chip pull-up or pull-down resistor.
I_{PU}	Input with pull-up	Input with on-chip pull-up resistor to VDDIO.
I_{PD}	Input with pull-down	Input with on-chip pull-down resistor to VSS.
I_{DIFF}	Input differential	Input differential signal pair
I_{PU}/O	Bidirectional with pull-up	Input and output signal with on-chip pull-up resistor to VDDIO or VDD33.
O	Output	Output signal.
O_{PU}	Output with pull-up	Output with on-chip pull-up resistor to VDDIO.
OD	Open drain	Open drain output.
OS	Open source	Open source output.
O_{DIFF}	Output differential	Output differential signal pair.

Table 93 • **Pin Type Symbols *(continued)***

Symbol	Pin Type	Description
A_{DIFF}	Analog differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog bias	Analog bias pin.
I_A	Analog input	Analog input for sensing variable voltage levels.
I_{PU5V}	Input with pull-up	Input with on-chip pull-up resistor to VDD33. These pins are 5 V tolerant.
O_{CRYST}	Crystal output	Crystal clock output pin. If not used, leave unconnected.
NC	No connect	No connect pins must be left floating.

6.3 Pins by Function

This section contains the functional pin descriptions for the VSC8662 device.

6.3.1 GPIO

The following table shows the pins associated with the device GPIO and SIGDET.

Table 94 • **GPIO Pins**

Name	Pin	Type	Description
GPIO15	J16	I_{PU}/O	General purpose input/output (GPIO). Ten dedicated GPIO pins are provided. Additionally, the fast link fail, two SIGDET pins, and three I2C controller pins can be configured to become GPIO pins if not used.
GPIO14	J15		
GPIO13	H14		
GPIO12	J14		
GPIO11	K16		
GPIO10	K15		
GPIO9/FastLinkFail	K14		
GPIO8/I2C_SDA	K13		
GPIO7	L16		
GPIO6	L15		
GPIO5/I2C_SCL_1	L14		
GPIO4/I2C_SCL_0	L13		
GPIO3	M16		
GPIO2	M15		
GPIO1/SIGDET_1	M14		
GPIO0/SIGDET_0	N14		

6.3.2 JTAG

The following table lists the pins associated with the device JTAG testing facility.

Table 95 • **JTAG Pins**

Name	Pin	Type	Description
NTRST	E3	I_{PU5V}	JTAG reset. When JTAG test operation is not in use, then tie this pin to VSS (ground) with a pull-down resistor for normal operation.
TCK	F3	I_{PU5V}	JTAG test clock input.
TDI	F2	I_{PU5V}	JTAG test serial data input.
TDO	F1	O_{PU}	JTAG test serial data output.
TMS	E2	I_{PU5V}	JTAG test mode select.

6.3.3 Miscellaneous Pins

The following table lists pins not associated with a particular interface or facility on the device.

Table 96 • **Miscellaneous Pins**

Name	Pin	Type	Description
CLKOUT	G15	O	Clock output can be enabled or disabled. It outputs a reference clock frequency of 125 MHz. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
CMODE7 CMODE6 CMODE5 CMODE4 CMODE3 CMODE2 CMODE1 CMODE0	E16 E15 D14 E14 F15 F14 G14 G13	I_A	Configuration mode (CMODE) pins. For more information, see CMODE, page 84.
LED3_[1:0] LED2_[1:0] LED1_[1:0] LED0_[1:0]	H4, G4 H3, G3 H2, G2 H1, G1	O	LED direct-drive outputs. All LEDs pins are active-low. A serial LED stream can also be implemented. For more information about LED operation, see LED Mode Select, page 67. **Note:** LEDbit_port, where port = PHY port number and bit = the particular LED for the port.
OSCEN	D2	I_{PD}	Oscillator enable. This pin is sampled on the rising edge of NRESET. If high, then the on-chip oscillator circuit is enabled. If low (or left floating), the oscillator circuit is disabled and the device must be supplied with a 25 MHz or 125 MHz reference clock to the REFCLK pin
PLLMODE	E1	I_{PD}	PLL mode input select. Sampled on power-up or reset. If PLLMODE is low, then REFCLK must be 25 MHz. If PLLMODE is high, then REFCLK must be 125 MHz. If using a crystal, PLLMODE must be pulled low.
RCVRD_CLK2 RCVRD_CLK1	G16 F16	O	Clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz based on the selected active recovered media programmed for this pin. This pin is not active when NRESET or NSRESET is asserted. When disabled, the pin is held low.
REF_FILT	D3	A_{BIAS}	Reference filter connects to an external 1 µF capacitor to analog ground.
REF_REXT	D4	A_{BIAS}	Reference external connects to an external 2 kΩ (1%) resistor to analog ground.

Table 96 • **Miscellaneous Pins *(continued)***

Name	Pin	Type	Description
RESERVED	A2, A3, A4, A5, A6, A7, A8, A9, B2, B3, B4, B5, B6, B7, B8, B9, C10, D13, E13, F13, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2, M1, N1, N4, P1, R2, R3, R4, R5, R6, R7, R8, R9, T2, T3, T4, T5, T6, T7, T8, T9	NC	Leave these pins unconnected (floating).
NC	A1, A16, T1, T16	NC	These pins are no connects. Do not connect them together or to ground. Leave these pins unconnected (floating).
THERMDA	H16	I_A	Thermal diode anode (p-junction).
THERMDC	H15	I_A	Thermal diode cathode (n-junction). Connected internally to VSS
XTAL1/REFCLK	D1	I	Crystal oscillator input. If OSCEN = high then a 25 MHz parallel resonant crystal with ±50 ppm frequency tolerance should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL1 pin to ground. Reference clock input. If OSCEN=low, the clock input frequency can either be 25 MHz (PLLMODE=0) or 125 MHZ (PLLMODE is high).
XTAL2	C1	O_{CRYST}	Crystal oscillator output. The crystal should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL2 pin to ground. If not using a crystal oscillator, this output pin can be left floating if driving XTAL1/REFCLK with a reference clock.

6.3.4 Power Supply

The following table lists the device power supply pins.

Table 97 • **Power Supply Pins**

Name	Pin	Type	Description
VDD12A	C7, C8, C9, C13, P6, P7, P8, P9, P10, P11	1.2 V	1.2 V analog power requiring additional PCB power supply filtering
VDD33	C2, C4, C6, C11, C14, E4, H13, M13, P5, P12, P13	3.3 V	General 3.3 V power supply
VDD12	E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5, M12, N5, N12	1.2 V	Internal digital logic
VDDIO	P3, M4	3.3 V 2.5 V 1.8 V	I/O power supply

Table 97 • **Power Supply Pins *(continued)***

Name	Pin	Type	Description
VSS	B1, B16, C3, C5, C12, D5, D6, D7, D8, D9, D10, D11, D12, E6, E7, E8, E9, E10, E11, F4, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, J13, K6, K7, K8, K9, K10, K11, L4, L6, L7, L8, L9, L10, L11, M6, M7, M8, M9, M10, M11, N6, N7, N8, N9, N10, N11, N13, P4, P14, R1, R16	0 V	General device ground

Although certain function pins may not be used for a specific application, all power supply pins must be connected to their respective voltage input.

Table 98 • **Power Supply and Associated Function Pins**

Pin	Nominal Voltage	Associated Functional Pins
VDD33	3.3 V	LED[3:0]_n, GPIO[15:0], JTAG (5), XTAL1, XTAL2, CMODE, TXVP_n, TXVN_n, REF_FILT, REF_REXT, RCVRD_CLK1, RCVRD_CLK2, CLKOUT
VDDIO	1.8 V, 2.5 V, 3.3 V	MDC, MDIO, MDINT*n*, nRESET
VDD12A	1.2 V	MAC_RDP/N_n, MAC_TDP/N_n
VDD12	1.2 V	N/A (Internal Core Voltage)

6.3.5 SerDes MAC Interface

The following table shows the pins associated with the device SerDes MAC interface.

Table 99 • **SerDes MAC Interface Pins**

Name	Pin	Type	Description
RDP_1 RDP_0 RDN_1 RDN_0	R12 P15 T12 P16	O_{DIFF}	SerDes MAC receiver output pair.
TDP_1 TDP_0 TDN_1 TDN_0	R13 N15 T13 N16	I_{DIFF}	SerDes MAC transmitter input pair.

6.3.6 SerDes Media Interface

The following table shows the pins associated with the device SerDes media interface.

Table 100 • **SerDes Media Interface Pins**

Signal Name	Pin	Type	Description
FIBR_DIP_1 FIBR_DIP_0 FIBR_DIN_1 FIBR_DIN_0	R11 R15 T11 T15	I_{DIFF}	SerDes media receiver input pair.
FIBR_DOP_1 FIBR_DOP_0 FIBR_DON_1 FIBR_DON_0	R10 R14 T10 T14	O_{DIFF}	SerDes media transmitter output pair.

6.3.7 Serial Management Interface

The following table lists the device pins associated with the device serial management interface (SMI). Note that the pins in this table are referenced to VDDIO and can be set to a 1.8 V, 2.5 V, or 3.3 V power supply.

Table 101 • **SMI Pins**

Name	Pin	Type	Description
MDC	P2	I_{PU}	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	N2	OD	Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.
MDINT1 MDINT0	N3 M2	OS/OD	Management interrupt signal. Upon reset the device will configure these pins as active-low (open drain) or active-high (open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.
NRESET	M3	I_{PU}	Device reset. Active low input that powers down the device and sets all register bits to their default state.
NSRESET	L3	I_{PU}	Device soft reset. Active low input that powers down the device. Although, the device is powered down any register bits that are sticky will retain their value.

6.4 Twisted Pair Interface

The following table lists the device pins associated with the device two-wire, twisted pair interface.

Table 102 • **Twisted Pair Interface Pins**

Name	Pin	Type	Description
TXVPA_1 TXVPA_0	A10 A14	A_{DIFF}	TX/RX channel A positive signal
TXVNA_1 TXVNA_0	B10 B14	A_{DIFF}	TX/RX channel A negative signal
TXVPB_1 TXVPB_0	A11 A15	A_{DIFF}	TX/RX channel B positive signal
TXVNB_1 TXVNB_0	B11 B15	A_{DIFF}	TX/RX channel B negative signal
TXVPC_1 TXVPC_0	A12 C16	A_{DIFF}	TX/RX channel C positive signal
TXVNC_1 TXVNC_0	B12 C15	A_{DIFF}	TX/RX channel C negative signal
TXVPD_1 TXVPD_0	A13 D16	A_{DIFF}	TX/RX channel D positive signal
TXVND_1 TXVND_0	B13 D15	A_{DIFF}	TX/RX channel D negative signal

6.5 Pins by Number

This section provides a numeric list of the VSC8662 device pins.

A1	NC	C7	VDD12A	E13	RESERVED
A2	RESERVED	C8	VDD12A	E14	CMODE4
A3	RESERVED	C9	VDD12A	E15	CMODE6
A4	RESERVED	C10	RESERVED	E16	CMODE7
A5	RESERVED	C11	VDD33	F1	TDO
A6	RESERVED	C12	VSS	F2	TDI
A7	RESERVED	C13	VDD12A	F3	TCK
A8	RESERVED	C14	VDD33	F4	VSS
A9	RESERVED	C15	TXVNC_0	F5	VDD12
A10	TXVPA_1	C16	TXVPC_0	F6	VSS
A11	TXVPB_1	D1	XTAL1/REFCLK	F7	VSS
A12	TXVPC_1	D2	OSCEN	F8	VSS
A13	TXVPD_1	D3	REF_FILT	F9	VSS
A14	TXVPA_0	D4	REF_REXT	F10	VSS
A15	TXVPB_0	D5	VSS	F11	VSS
A16	NC	D6	VSS	F12	VDD12
B1	VSS	D7	VSS	F13	RESERVED
B2	RESERVED	D8	VSS	F14	CMODE2
B3	RESERVED	D9	VSS	F15	CMODE3
B4	RESERVED	D10	VSS	F16	RCVRD_CLK1
B5	RESERVED	D11	VSS	G1	LED0_0
B6	RESERVED	D12	VSS	G2	LED1_0
B7	RESERVED	D13	RESERVED	G3	LED2_0
B8	RESERVED	D14	CMODE5	G4	LED3_0
B9	RESERVED	D15	TXVND_0	G5	VDD12
B10	TXVNA_1	D16	TXVPD_0	G6	VSS
B11	TXVNB_1	E1	PLLMODE	G7	VSS
B12	TXVNC_1	E2	TMS	G8	VSS
B13	TXVND_1	E3	NTRST	G9	VSS
B14	TXVNA_0	E4	VDD33	G10	VSS
B15	TXVNB_0	E5	VDD12	G11	VSS
B16	VSS	E6	VSS	G12	VDD12
C1	XTAL2	E7	VSS	G13	CMODE0
C2	VDD33	E8	VSS	G14	CMODE1
C3	VSS	E9	VSS	G15	CLKOUT
C4	VDD33	E10	VSS	G16	RCVRD_CLK2
C5	VSS	E11	VSS	H1	LED0_1
C6	VDD33	E12	VDD12	H2	LED1_1

Pins by number *(continued)*

H3	LED2_1
H4	LED3_1
H5	VDD12
H6	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VDD12
H13	VDD33
H14	GPIO13
H15	THERMDC
H16	THERMDA
J1	RESERVED
J2	RESERVED
J3	RESERVED
J4	RESERVED
J5	VDD12
J6	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VDD12
J13	VSS
J14	GPIO12
J15	GPIO14
J16	GPIO15
K1	RESERVED
K2	RESERVED
K3	RESERVED
K4	RESERVED
K5	VDD12
K6	VSS
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VDD12
K13	GPIO8/I2C_SDA
K14	GPIO9/FastLinkFail
K15	GPIO10
K16	GPIO11
L1	RESERVED
L2	RESERVED
L3	NSRESET
L4	VSS
L5	VDD12
L6	VSS
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VDD12
L13	GPIO4/I2C_SCL_0
L14	GPIO5/I2C_SCL_1
L15	GPIO6
L16	GPIO7
M1	RESERVED
M2	MDINT0
M3	NRESET
M4	VDDIO
M5	VDD12
M6	VSS
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VDD12
M13	VDD33
M14	GPIO1/SIGDET1
M15	GPIO2
M16	GPIO3
N1	RESERVED
N2	MDIO
N3	MDINT1
N4	RESERVED
N5	VDD12
N6	VSS
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VDD12
N13	VSS
N14	GPIO0/SIGDET0
N15	TDP_0
N16	TDN_0
P1	RESERVED
P2	MDC
P3	VDDIO
P4	VSS
P5	VDD33
P6	VDD12A
P7	VDD12A
P8	VDD12A
P9	VDD12A
P10	VDD12A
P11	VDD12A
P12	VDD33
P13	VDD33
P14	VSS
P15	RDP_0
P16	RDN_0
R1	VSS
R2	RESERVED
R3	RESERVED
R4	RESERVED
R5	RESERVED
R6	RESERVED
R7	RESERVED
R8	RESERVED
R9	RESERVED
R10	FIBR_DOP_1
R11	FIBR_DIP_1
R12	RDP_1
R13	TDP_1

Pins by number *(continued)*

R14	FIBR_DOP_0
R15	FIBR_DIP_0
R16	VSS
T1	NC
T2	RESERVED
T3	RESERVED
T4	RESERVED
T5	RESERVED
T6	RESERVED
T7	RESERVED
T8	RESERVED
T9	RESERVED
T10	FIBR_DON_1
T11	FIBR_DIN_1
T12	RDN_1
T13	TDN_1
T14	FIBR_DON_0
T15	FIBR_DIN_0
T16	NC

6.6 Pins by Name

This section provides an alphabetical list of the VSC8662 device pins.

CLKOUT	G15
CMODE0	G13
CMODE1	G14
CMODE2	F14
CMODE3	F15
CMODE4	E14
CMODE5	D14
CMODE6	E15
CMODE7	E16
FIBR_DIN_0	T15
FIBR_DIN_1	T11
FIBR_DIP_0	R15
FIBR_DIP_1	R11
FIBR_DON_0	T14
FIBR_DON_1	T10
FIBR_DOP_0	R14
FIBR_DOP_1	R10
GPIO0/SIGDET0	N14
GPIO1/SIGDET1	M14
GPIO2	M15
GPIO3	M16
GPIO4/I2C_SCL_0	L13
GPIO5/I2C_SCL_1	L14
GPIO6	L15
GPIO7	L16
GPIO8/I2C_SDA	K13
GPIO9/FastLinkFail	K14
GPIO10	K15
GPIO11	K16
GPIO12	J14
GPIO13	H14
GPIO14	J15
GPIO15	J16
LED0_0	G1
LED0_1	H1
LED1_0	G2
LED1_1	H2
LED2_0	G3
LED2_1	H3
LED3_0	G4
LED3_1	H4
MDC	P2
MDINT0	M2
MDINT1	N3
MDIO	N2
NC	A1
NC	A16
NC	T1
NC	T16
NRESET	M3
NSRESET	L3
NTRST	E3
OSCEN	D2
PLLMODE	E1
RCVRD_CLK1	F16
RCVRD_CLK2	G16
RDN_0	P16
RDN_1	T12
RDP_0	P15
RDP_1	R12
REF_FILT	D3
REF_REXT	D4
RESERVED	A2
RESERVED	A3
RESERVED	A4
RESERVED	A5
RESERVED	A6
RESERVED	A7
RESERVED	A8
RESERVED	A9
RESERVED	B2
RESERVED	B3
RESERVED	B4
RESERVED	B5
RESERVED	B6
RESERVED	B7
RESERVED	B8
RESERVED	B9
RESERVED	C10
RESERVED	D13
RESERVED	E13
RESERVED	F13
RESERVED	J1
RESERVED	J2
RESERVED	J3
RESERVED	J4
RESERVED	K1
RESERVED	K2
RESERVED	K3
RESERVED	K4
RESERVED	L1
RESERVED	L2
RESERVED	M1
RESERVED	N1
RESERVED	N4
RESERVED	P1
RESERVED	R2
RESERVED	R3
RESERVED	R4
RESERVED	R5
RESERVED	R6
RESERVED	R7
RESERVED	R8
RESERVED	R9
RESERVED	T2
RESERVED	T3
RESERVED	T4
RESERVED	T5
RESERVED	T6
RESERVED	T7
RESERVED	T8
RESERVED	T9
TCK	F3
TDI	F2

Pins by name *(continued)*

TDN_0	N16	VDD12	N12	VSS	E10
TDN_1	T13	VDD33	C2	VSS	E11
TDO	F1	VDD33	C4	VSS	F4
TDP_0	N15	VDD33	C6	VSS	F6
TDP_1	R13	VDD33	C11	VSS	F7
THERMDA	H16	VDD33	C14	VSS	F8
THERMDC	H15	VDD33	E4	VSS	F9
TMS	E2	VDD33	H13	VSS	F10
TXVNA_0	B14	VDD33	M13	VSS	F11
TXVNA_1	B10	VDD33	P5	VSS	G6
TXVNB_0	B15	VDD33	P12	VSS	G7
TXVNB_1	B11	VDD33	P13	VSS	G8
TXVNC_0	C15	VDD12A	C7	VSS	G9
TXVNC_1	B12	VDD12A	C8	VSS	G10
TXVND_0	D15	VDD12A	C9	VSS	G11
TXVND_1	B13	VDD12A	C13	VSS	H6
TXVPA_0	A14	VDD12A	P6	VSS	H7
TXVPA_1	A10	VDD12A	P7	VSS	H8
TXVPB_0	A15	VDD12A	P8	VSS	H9
TXVPB_1	A11	VDD12A	P9	VSS	H10
TXVPC_0	C16	VDD12A	P10	VSS	H11
TXVPC_1	A12	VDD12A	P11	VSS	J6
TXVPD_0	D16	VDDIO	P3	VSS	J7
TXVPD_1	A13	VDDIO	M4	VSS	J8
VDD12	E5	VSS	B1	VSS	J9
VDD12	E12	VSS	B16	VSS	J10
VDD12	F5	VSS	C3	VSS	J11
VDD12	F12	VSS	C5	VSS	J13
VDD12	G5	VSS	C12	VSS	K6
VDD12	G12	VSS	D5	VSS	K7
VDD12	H5	VSS	D6	VSS	K8
VDD12	H12	VSS	D7	VSS	K9
VDD12	J5	VSS	D8	VSS	K10
VDD12	J12	VSS	D9	VSS	K11
VDD12	K5	VSS	D10	VSS	L4
VDD12	K12	VSS	D11	VSS	L6
VDD12	L5	VSS	D12	VSS	L7
VDD12	L12	VSS	E6	VSS	L8
VDD12	M5	VSS	E7	VSS	L9
VDD12	M12	VSS	E8	VSS	L10
VDD12	N5	VSS	E9	VSS	L11

Pins by name *(continued)*

VSS	M6
VSS	M7
VSS	M8
VSS	M9
VSS	M10
VSS	M11
VSS	N6
VSS	N7
VSS	N8
VSS	N9
VSS	N10
VSS	N11
VSS	N13
VSS	P4
VSS	P14
VSS	R1
VSS	R16
XTAL1/REFCLK	D1
XTAL2	C1

7 Package Information

The VSC8662 device is offered with two operating temperature ranges. The operating temperature range for VSC8662 is 0 °C ambient to 90 °C case, and the range for VSC8662-03 is –40 °C ambient to 100 °C case.

VSC8662XIC and VSC8662XIC-03 are packaged in a lead-free (Pb-free), 256-pin, plastic ball grid array (BGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 2 mm maximum height.

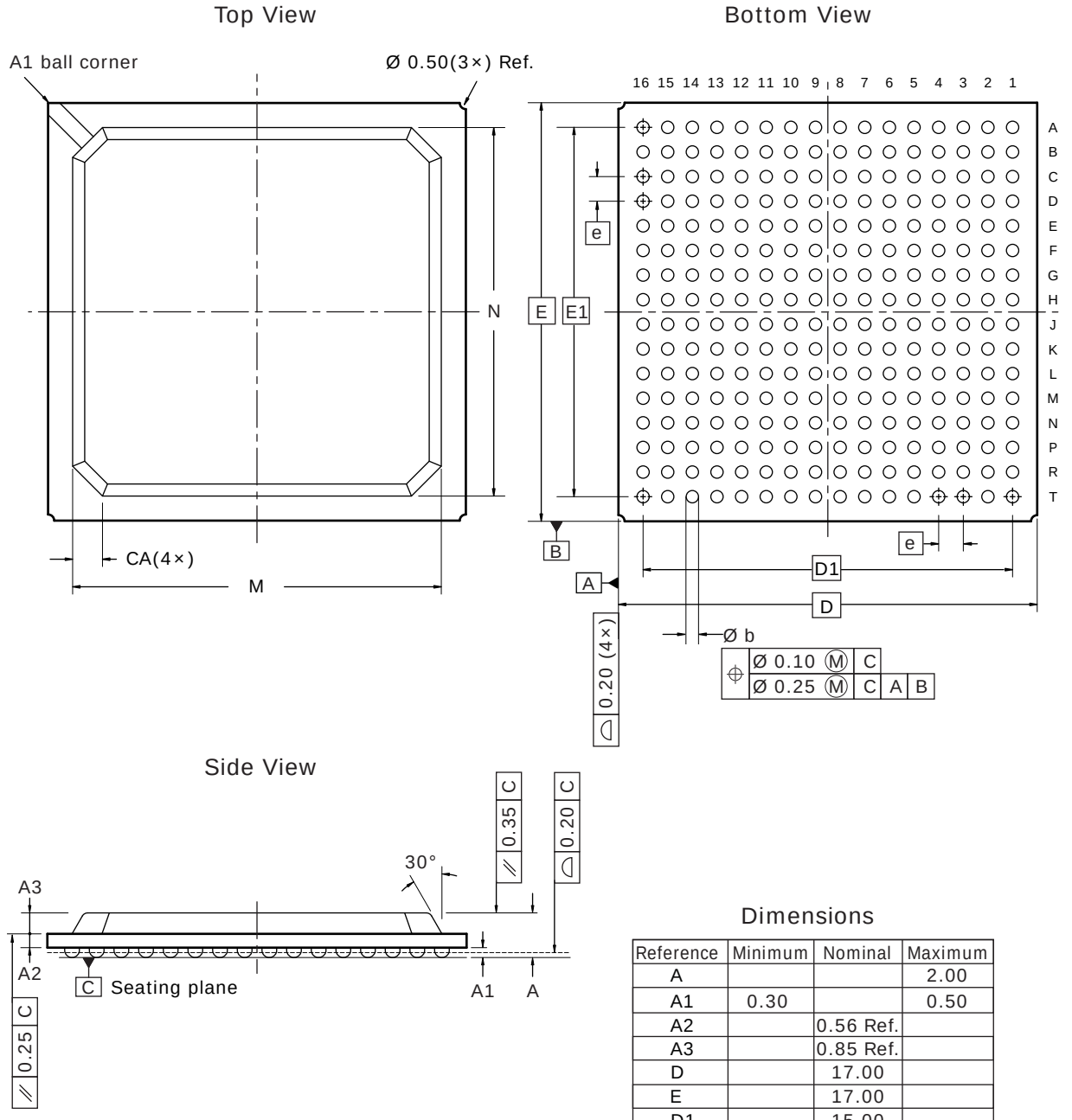
Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8662 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8662 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 27 • **Package Drawing**



Dimensions

Reference	Minimum	Nominal	Maximum
A			2.00
A1	0.30		0.50
A2		0.56 Ref.	
A3		0.85 Ref.	
D		17.00	
E		17.00	
D1		15.00	
E1		15.00	
e		1.00	
b	0.40	0.50	0.60
M		15.00	
N		15.00	
CA		1.21 Ref.	

Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Radial true position is represented by typical values.

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 103 • **Thermal Resistances**

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC8662XIC	7.5	11.2	21.9	20.4	19.4
VSC8662XIC-03	7.5	11.2	21.9	20.4	19.4

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Considerations

This section provides design guidelines for the VSC8662 device.

8.1 Required Device Configuration

After initial NRESET deassertion or any time NSRESET is deasserted, the following script must be run to correctly configure the part:

```
PhyWrite(BasePortNo + 2, 31, 0x0000);

PhyWrite(BasePortNo + 2, 0, 0x0800);

PhyWrite(BasePortNo + 3, 31, 0x0000);

PhyWrite(BasePortNo + 3, 0, 0x0800);
```

If a broadcast write is made to MII register 0 that either sets bit 15 or clears bit 11, the preceding script must be re-run afterwards.

8.2 Broadcast Writes

Because the scripts to implement the workarounds in this section need to be written to all ports of the device, the broadcast write feature is useful to reduce the time to initialize the device. Broadcast writes do not apply across multiple VSC8662 devices on a single SMI bus (for example, you must perform the broadcast write to each device).

Note that broadcast writes are enabled by setting register bit 22.0 in any one of the two ports in a given VSC8662 device. They may be disabled by clearing the bit in any one of the two ports in the same device.

Command format:

```
PhyWrite( PortNo, Register (dec), 16_bit_unsigned_data(hex) );
16_bit_unsigned_data = PhyRead( PortNo, Register (dec) );
```

To enable broadcast writes, precede the sequence of initialization scripts with the following script:

```
PhyWrite(PortNo, 31, 0x0000 ); // Goto Mii Register Page
MiiReg22 = PhyRead(PortNo, 22 ); // Read MiiReg22
MiiReg22 = (MiiReg22 | 0x0001); //Enable broadcast write
PhyWrite(PortNo, 22, MiiReg22 ); //Write MiiReg22
```

To disable broadcast writes, use the following script after the sequence of initialization scripts:

```
MiiReg22 = (MiiReg22 & 0xfffe); //Disable broadcast write
PhyWrite(PortNo, 22, MiiReg22 ); //Write MiiReg22
```

8.3 Enabling LED Blinking After Reset

Issue: To enable LED blinking after reset de-assertion, a software sequence must be run. Setting the register alone (register 19E, bit 11) does not enable the feature. In contrast, other Vitesse Ethernet PHY devices enable this feature either through the register setting or through a CMODE pin.

Implications: LEDs will not blink after reset de-assertion unless the feature is initialized as shown in the following script.

Workaround: Use the following script to change the value of the LED blink configuration register (address 19E, bit 11) on all ports and then perform a soft reset on all ports.

Command format:

```
PhyWrite( PortNo, Register (dec), 16_bit_unsigned_data(hex) );
16_bit_unsigned_data = PhyRead( PortNo, Register (dec) );
```

On hardware initialization, run the following:

```
PhyWrite( PortNo, 31, 0x0001 ); // Goto ExtMii Register Page
ExtReg19 = PhyRead(PortNo, 19); //Read ExtReg19
ExtReg19 = (ExtReg19 | 0x0800); //Enable LED blink for 1 second
PhyWrite( PortNo, 19, ExtReg19 ); //Write ExtReg19
```

After enabling LED blink after reset, you can assert and de-assert the NSRESET pin on the device to complete the soft reset. Using the NSRESET pin allows the LED blink to be synchronized across multiple VSC8662 devices. Alternatively, the following soft reset script may be issued to each VSC8662 port:

```
PhyWrite( 0, 31, 0x0000 ); // Goto Mii Register Page
PhyWrite( 0, 0, 0x9040 ); // Perform soft reset
```

8.4 100/1000BASE-T Amplitude Compensation

Issue: The 100BASE-TX and 1000BASE-T amplitudes must be increased to meet specifications.

Implications: If uncompensated, the 100BASE-TX and 1000BASE-T transmission is at reduced amplitude.

Workaround: Use the following script to adjust the 100BASE-TX and 1000BASE-T transmitter amplitude.

Command format:

```
PhyWrite( PortNo, Register (dec), 16_bit_unsigned_data(hex) );
16_bit_unsigned_data = PhyRead( PortNo, Register (dec) );
```

On hardware initialization, run the following:

```
PhyWrite( PortNo, 31, 0x2a30);
Reg24 = PhyRead(PortNo, 24 );
Reg24 = ((Reg24 & 0xfffb ) | 0x0003 );
PhyWrite( PortNo, 24, Reg24 );
PhyWrite( PortNo, 31, 0x0000);
Reg24 = PhyRead(PortNo, 24 );
Reg24 = ((Reg24 & 0xfff5 ) | 0x0004 );
PhyWrite( PortNo, 24, Reg24 );
```

8.5 Increase 10BASE-T Performance

Issue: In order to ensure robust performance of 10BASE-T links, an initialization script should be performed.

Workaround: Use the following script on hardware initialization.

```
PhyWrite( PortNo, 31, 0x52b5 );
PhyWrite( PortNo, 18, 0x0 );
PhyWrite( PortNo, 17, 0x3f );
PhyWrite( PortNo, 16, 0x8794 );

PhyWrite( PortNo, 18, 0xf7 );
PhyWrite( PortNo, 17, 0xadb4 );
PhyWrite( PortNo, 16, 0x879e );
```

```
PhyWrite( PortNo, 18, 0x0 );
PhyWrite( PortNo, 17, 0x32 );
PhyWrite( PortNo, 16, 0x87a0 );

PhyWrite( PortNo, 18, 0x41 );
PhyWrite( PortNo, 17, 0x410 );
PhyWrite( PortNo, 16, 0x87a2 );

PhyWrite( PortNo, 18, 0x41 );
PhyWrite( PortNo, 17, 0x410 );
PhyWrite( PortNo, 16, 0x87a4 );

PhyWrite( PortNo, 18, 0x41 );
PhyWrite( PortNo, 17, 0x284 );
PhyWrite( PortNo, 16, 0x87a6 );

PhyWrite( PortNo, 18, 0x92 );
PhyWrite( PortNo, 17, 0xbcb8 );
PhyWrite( PortNo, 16, 0x87a8 );

PhyWrite( PortNo, 18, 0x3 );
PhyWrite( PortNo, 17, 0xcfbf );
PhyWrite( PortNo, 16, 0x87aa );

PhyWrite( PortNo, 18, 0x49 );
PhyWrite( PortNo, 17, 0x2451 );
PhyWrite( PortNo, 16, 0x87ac );

PhyWrite( PortNo, 18, 0x1 );
PhyWrite( PortNo, 17, 0x1410 );
PhyWrite( PortNo, 16, 0x87c0 );

PhyWrite( PortNo, 18, 0x10 );
PhyWrite( PortNo, 17, 0xb498 );
PhyWrite( PortNo, 16, 0x87e8 );

PhyWrite( PortNo, 18, 0x71 );
PhyWrite( PortNo, 17, 0xe7dd );
PhyWrite( PortNo, 16, 0x87ea );

PhyWrite( PortNo, 18, 0x69 );
PhyWrite( PortNo, 17, 0x6512 );
PhyWrite( PortNo, 16, 0x87ec );

PhyWrite( PortNo, 18, 0x49 );
PhyWrite( PortNo, 17, 0x2451 );
PhyWrite( PortNo, 16, 0x87ee );

PhyWrite( PortNo, 18, 0x45 );
PhyWrite( PortNo, 17, 0x410 );
PhyWrite( PortNo, 16, 0x87f0 );

PhyWrite( PortNo, 18, 0x41 );
PhyWrite( PortNo, 17, 0x410 );
PhyWrite( PortNo, 16, 0x87f2 );
```

```
PhyWrite( PortNo, 18, 0x0 );
PhyWrite( PortNo, 17, 0x10 );
PhyWrite( PortNo, 16, 0x87f4 );

PhyWrite( PortNo, 31, 0x2a30);
Reg9 = PhyRead(PortNo, 9 );
Reg9 = ((Reg9 & 0xffff ) | 0x0040 );
PhyWrite( PortNo, 9, Reg9 );
//PhyWrite( PortNo, 31, 0x0000);

Reg22 = PhyRead(PortNo, 22 );
Reg22 = ((Reg22 & 0xffff ) | 0x0010 );
PhyWrite( PortNo, 22, Reg22 );
PhyWrite( PortNo, 31, 0x0000);
```

8.6 Performance Optimization for 100BASE-TX and 1000BASE-T Slave

Issue: To improve start-up reliability on the longest cables, an initialization sequence must be run. This initialization configures the receiver for optimal reach in both 1000BASE-T slave and 100BASE-TX operating modes.

Implications: If not optimized, 100BASE-TX and 1000BASE-T links over a 100 m or longer cable may fail to come up.

Workaround: Use the following script to optimize these links. This can be run once during hardware initialization regardless of the operating speed.

```
PhyWrite( PortNo, 31, 0x2a30);
Reg0 = PhyRead(PortNo, 0 );
Reg0 = ((Reg0 & 0xffef ) | 0x0060 );
PhyWrite( PortNo, 0, Reg0 );

PhyWrite( PortNo, 31, 0x52b5 );
PhyWrite( PortNo, 18, 0x12 );
PhyWrite( PortNo, 17, 0x480a );
PhyWrite( PortNo, 16, 0x8f82 );

PhyWrite( PortNo, 18, 0x0 );
PhyWrite( PortNo, 17, 0x422 );
PhyWrite( PortNo, 16, 0x8f86 );

PhyWrite( PortNo, 18, 0x3c );
PhyWrite( PortNo, 17, 0x3800 );
PhyWrite( PortNo, 16, 0x8f8a );

PhyWrite( PortNo, 18, 0x8 );
PhyWrite( PortNo, 17, 0xe33f );
PhyWrite( PortNo, 16, 0x83ae );
PhyWrite( PortNo, 31, 0x0000);
```

8.7 Enable SGMII Version 1.8

Issue: By default, the SGMII version supported is 1.7.

Implications: SGMII version 1.8 is not enabled by default.

Workaround: To enable SGMII version 1.8, set register 20E, bit 15 = 1.

8.8 Disabling Recovered Clock Output

Issue: When the recovered clock output is disabled by setting bit 15 to 0 in either register 23G or register 24G, the recovered clock output pins (RCVRD_CLK1 or RCVRD_CLK2) are not disabled.

Implications: The recovered clock output is not disabled by setting only bit 15 in register 23G or register 24G.

Workaround: To disable the recovered clock output, clear bit 15, and change the state of the selected PHY port in bit12, the clock frequency in bit 8, or the clock selection in bits 1:0.