W65C134S
8-bit Microcontroller

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DOCUMENT REVISION HISTORY

Version	Date	Authors	Description
2.0	10/15/2019	Bill Mensch	Rewrite of the W65C134S Datasheet

1 INTRODUCTION

The WDC W65C134S microcontroller is a complete fully static 8-bit computer fabricated on a single chip using a low power CMOS process. The W65C134S has been developed with life support features recommended by medical electronics firms. The Serial Interface Bus (SIB) was designed for an in-the-human-body token passing local area network (LAN) for eight (8) networked controllers.

This product description assumes that the reader is familiar with the W65C02S CPU hardware and programming capabilities. Refer to the W65C02S Datasheet, Programming the 65816: Including the 6502, 65C02 and 65802 and W65C134SXB Single Board Computer (SBC) for more information.

1.1 KEY FEATURES OF THE W65C134S

- CMOS low power process
- Operating TA= -40EC to +85EC
- Single 2.8V to 5.5V power supply
- Static to 8MHz clock operation
- W65C02S compatible CPU
  - 8-bit parallel processing
  - Variable length stack
  - True indexing capability
  - Fifteen addressing modes
  - Decimal or binary arithmetic
  - Pipeline architecture
  - Fully static CPU
  - W65C816S 16-bit CPU compatible
- Single chip microcomputer
  - Many power saving features
  - 56 CMOS compatible I/O lines
  - 4096 x 8 ROM on chip
  - 192 x 8 RAM on chip
- Low power modes
  - WAIt for interrupt
  - SToP the clock
  - Fast oscillator start and stop feature
- Twenty-two priority encoded interrupts
  - BRK software interrupt
  - RESET "RESTART" interrupt
  - NMIB Non-Maskable Interrupt input
  - SIB Interrupt
  - IRQ1B level interrupt input
  - IRQ2B level interrupt input
  - 2 timer edge interrupts
  - 7 positive edge interrupt inputs
  - 5 negative edge interrupt inputs
  - Asynchronous Receiver Interrupt
  - Asynchronous Transmitter Interrupt
- UART 7/8-bit w/wo odd or even parity
- 16M byte segmented address space
- 64K byte linear address space
- 4 x 16 bit timer/counters
- Bus control register for external memory
  - Internal or external ROM
  - 8 Decoded Chip Select outputs
- Surface mount 68 and 80 lead packages
- Real time clock features
- Third party tools available

2 W65C134S FUNCTION DESCRIPTION

The embedded microprocessor is the W65C02 Static 8-bit Microprocessor Core that does not include the bit-manipulation instructions made popular by Rockwell Semiconductor.

2.1 Monitor ROM

The W65C134S 4096 x 8 bit Read Only Memory (ROM) Monitor contains the user's programmer terminal interface with a library of built-in functions. These program instructions and constants are mask-programmed into the ROM during fabrication of the W65C134S device. The W65C134S ROM is memory mapped from $F000 to $FFFF. The W65C134S Monitor ROM Reference Manual, Monitor Rom code listing, and WDCTools for Assembly and C language software development are available for developers.

2.2 SRAM ($0040-FF and $0140-FF)

The 192 x 8 bit Static Random Access Memory (SRAM) contains the user program stack and is used for scratch pad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. In order to take advantage of zero page addressing capabilities, the W65C134S RAM is assigned to both page zero memory addresses $0040 to $00FF and to page one stack addresses $0140 to $01FF.

2.3 Bus Control Register (BCR) ($001B)

The Bus Control Register (BCR) controls the various modes of I/O and external memory interface. During power-up the value of BE defines the initial values of BCR0, BCR3 and BCR7, three bits in the BCR that set up the W65C134S for normal or test mode operation. When BE goes high after RESB goes high the BCR sets up the W65C134S for test mode. Port 0 and 1 are the address outputs, Port 2 is the data I/O bus and RUN is the multiplexed RUN function. See RUN pin function description. When BE goes high before RESB goes high, all bits in the BCR are "0". After RESB goes high BE no longer effects the BCR register, and BCR may be written under software control to reconfigure the W65C134S as desired. Table 2.3-1 indicates how BCR7 and BE define the W65C134S configuration.

Figure 2.3-1 BE Timing Relative to RESB Input.

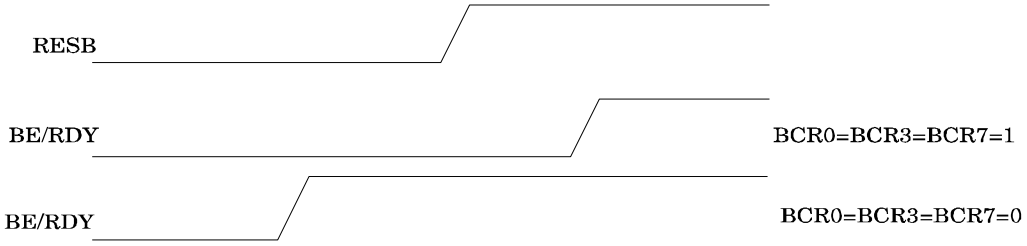


Table 2.3-1 BCR7 and BE Control

BCR7	BE	W65C134S configuration
0	0	Internal ROM External Processor (DMA test mode)
0	1	Internal ROM Internal Processor
1	0	External ROM External Processor (DMA test mode)
1	1	External ROM Internal Processor

2.3.1 Bus Control Register (BCR) Description

Address = $001B		BCR: BCR Register					Reset Value = 0x00	
7:0->	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
HWRES	0 = BE High	0	0	0	0	0	0	0
BERES	1 = BE Low	-	-	-	1	-	-	1

Bit	Name	Access	Description
7	BCR7	R/W	1 = External ROM at $F000-FFFF
			0 = Internal ROM at $F000-FFFF
6	BCR6	R/W	1 = P40=NMIB, P41=IRQ1B, P42=IRQ2B inputs
			0 = Pins 40-42 are standard I/O
5	BCR5	R/W	1 = EDGE interrupt inputs on P54-57
			0 = No EDGE interrupt inputs on P54-57
4	BCR4	R/W	1 = EDGE interrupt inputs on P50-53
			0 = No EDGE interrupt inputs on P50-53
3	BCR3	R/W	1 = Test Mode with on-chip addressed memory or I/O for reads or writes are output on the data bus.
			0 = Normal Operation RUN=RUN
2	BCR2	R/W	1 = SIB Enabled with Interrupt (P64=SCLK, P65=SDAT, P66=CHIN, P67=CHOUT)
			0 = SIB Disabled
1	BCR1	R/W	1 = Edge Interrupt Inputs on P44-47
			0 = No Edge Interrupt Inputs on P44-47
0	BCR0	R/W	1 = Ports 0,1,2 are address and data bus pins
			0 = Ports 0,1,2 are I/O pins

2.4 Port Chip Select 3 (PCS3) Register ($0007)

The Port Chip Select (PCS3) Register. The PCS3 provides enables or disables the chip select output on Port 3. When PCS30-PCS37 are equal to a "1", then CS0B to CS7B will be active. When CS1B is active, the defined memory space for CS3B and/or CS6B is reduced. It is reduced by the memory space 0100-011F for CS1B. When CS2B is active, the defined memory space for CS3B and/or CS6B is reduced. It is reduced by the memory space 0120-013F for CS2B.

CS7B is automatically enabled when BCR7=1.

The W65C134S will use the internal RAM as stack when PCS33 and PCS36 are disabled. If PCS33 or PCS36 are enabled then the off chip stack is used.

2.4.1 Chip Select Register on Port 3 (PCS3) Description

Address = $0007		PCS3: Timer Interrupt Enable Register					Reset Value = 0x00	
7:0->	PCS37	PCS36	PCS35	PCS34	PCS33	PCS32	PCS31	PCS30

Bit	Name	Access	Description
7	PCS37	R/W	1 = Chip Select 7 Enabled
			0 = Chip Select 7 Disabled
6	PCS36	R/W	1 = Chip Select 6 Enabled
			0 = Chip Select 6 Disabled
5	PCS35	R/W	1 = Chip Select 5 Enabled
			0 = Chip Select 5 Disabled
4	PCS34	R/W	1 = Chip Select 4 Enabled
			0 = Chip Select 4 Disabled
3	PCS33	R/W	1 = Chip Select 3 Enabled
			0 = Chip Select 3 Disabled
2	PCS32	R/W	1 = Chip Select 2 Enabled
			0 = Chip Select 2 Disabled
1	PCS31	R/W	1 = Chip Select 1 Enabled
			0 = Chip Select 1 Disabled
0	PCS30	R/W	1 = Chip Select 0 Enabled
			0 = Chip Select 0 Disabled

2.5 The Timers

Upon Timer clock input negative edge the timer low counter is decremented by 1.

When T1 or T2 prescaler mode is enabled, (making timer low counter a divide-by-N+1 prescaler) then timer low counter is reloaded from timer low latch. Monitor Timer M does not have a prescaler mode.

A write to the timer low counter writes the timer low latch.

A read of the timer high or low counter reads the timer high or low counter.

Upon Timer clock input negative edge when the timer low counter reaches zero, the timer high counter is decremented by 1.

Upon Timer clock input positive edge, when the timer high counter reaches zero, this sequence occurs:

Timer 1 and 2 set their associated interrupt flag. If the interrupt is enabled the MPU is then interrupted and control is transferred to the vector associated with the interrupt. When Timer M times out, the W65C134S is restarted: On-chip logic pulls RESB pin low for 2 CLK cycles and releases RESB to go high, "restarting" the W65C134S.

The timer hi counter is loaded from the timer hi latch, and timer low counter is loaded from timer low latch.

A write to the Timer 1, 2 or A high counter writes to the timer hi latch and this sequence occurs:

The timer hi latch is loaded from data bus. The timer low counter is loaded from the timer low latch, and the timer hi counter is loaded from the timer hi latch.

Timer M is disabled after RESB and is activated by the first Timer Control Register One (TCR10) transition from "0" to "1" (the first load of Timer M).

The Timer M counter is reloaded with the value in the Timer M latches when the TCR10 bit 0 makes a transition from a "0" to "1". TCR10 transition from a "1" to a "0" has no effect on the timer.

2.5.1 Timer Control Register One (TCR1) Description

Address = $000A		TCR1: Timer Control Register One					Reset Value = 0x00	
7:0->	TCR17	TCR16	TCR15	TCR14	TCR13	TCR12	TCR11	TCR10
Bit	**Name**	**Access**	**Description**					
7	TCR17	R/ W=1 Clears	1 = Timer A edge Interrupt has occurred. This interrupt vector is located at the Asynchronous Transmitter vector location. This bit is cleared to a "0" by writing a "1" to it. Writing a "0" to this bit has no affect.					
			0 = Timer A Edge Interrupt has not occurred. This bit cannot be set when UART is in operation.					
6	TCR16	R/W	1 = Timer A Interrupt Enabled.					
			0 = Timer A Interrupt Disabled.					
5	TCR15	R/W	1 = Timer A TOUT enabled. When ACSR0=1, Timer A and TXD are used for the UART.					
			0 = Timer A output disabled					
4	TCR14	R/W	1 = Timer A counts TIN negative pulses. When ACSR5=1, Timer A and RXD are used for the UART and this bit should be cleared to "0".					
			0 = Timer A counts PHI2 clock pulses					
3	TCR13	R/W	1 = Timer A clock enabled 1 for UART operation					
			0 = Timer A clock disabled (counter stopped)					
2	TCR12	R/W	1 = Start FCLK					
			0 = Stop FCLK					
1	TCR11	R/W	1 = PHI2 clock source is FCLK (Fast Clock)					
			0 = PHI2 clock source is CLK (Clock)					
0	TCR10	R/W	1 = 1 to 0 has no effect on M Watch Dog Timer					
			0 = 0 to 1 transition loads the M Watch Dog Timer					

2.5.2 Timer Control Register Two (TCR2) Description

Address = $000B		TCR1: Timer Control Register One					Reset Value = 0x00	
7:0->	TCR27	TCR26	TCR25	TCR24	TCR23	TCR22	TCR21	TCR20
Bit	**Name**	**Access**	**Description**					
7	TCR27	R always 0	1 = Never					
			0 = Does nothing					
6	TCR26	R/W	1 = Timer A Interrupt Enabled.					
			0 = Timer A Interrupt Disabled.					
5	TCR25	R/W	1 = 8 bit prescaled with 8 bit counter mode					
			0 = 16 bit counter mode					
4	TCR24	R/W	1 = T2 counts CLK clock pulses					
			0 = T2 counts PHI2 clock pulses					
3	TCR23	R/W	1 = T2 clock enabled (counting clock as selected by TCR24)					
			0 = T2 clock disabled (counter stopped)					
2	TCR22	R/W	1 = 8 bit prescaler with 8 bit counter mode					
			0 = 16 bit counter mode					
1	TCR21	R/W	1 = T1 counts CLK clock pulses					
			0 = T1 counts PHI2 clock pulses					
0	TCR20	R/W	1 = T1 clock enabled (counting clock as selected by TCR21)					
			0 = T1 clock disabled (counter stopped)					

2.6 Interrupt Flag Registers (IFR1, IFR2) ($002C, $0008)

Each bit of these interrupt flag registers is set to a "1" in response to a interrupt source. Sources specified as level-triggered assert the corresponding IFR bit if an edge occurs and is held to a "1" as long as the IRQxB input is held low. Sources specified as edge-triggered assert the corresponding IFR bit upon and only upon transition to the specified polarity. Note that changes for edge-triggered bits are asynchronous with PHI2.

2.6.1 Read of IFR1 and IFR2.

A read from an IFR register transfers its value to the internal data bus.
Write to IFR1 and IFR2
A write of a "1" to any bits of these registers disserts those bits but has no further effect when execution of that write instruction is completed; that is, the bit is reset by a pulse but not held reset. A write of a "0" to any bits of these registers has no effect.

2.6.2 Interrupt Priority

If more than one bit of the Interrupt Flag Registers are set to a "1" and enabled, the vector corresponding to the highest bit number asserted is used. For example, if both the IFR10 and IFR23 were asserted and enabled, then the vector corresponding to IFR23 would be used. For another example, if both the IFR13 and IFR20 were asserted and enabled, then the vector corresponding to IFR20 would be used.

2.6.1 Interrupt Flag Register One (IFR1) Description

Address = $002C		IFR1: Interrupt Flag Register One					Reset Value = 0x00	
7:0->	IFR17	IFR16	IFR15	IFR14	IFR13	IFR12	IFR11	IFR10
Bit	**Name**	**Access**	**Description**					
7	IFR17	R/W	1 = NE53 Negative Edge Interrupt Occurred					
			0 = NE53 Negative Edge Interrupt Did Not Occur					
6	IFR16	R/W	1 = NE52 Negative Edge Interrupt Occurred					
			0 = NE52 Negative Edge Interrupt Did Not Occur					
5	IFR15	R/W	1 = PE51 Positive Edge Interrupt Occurred					
			0 = PE51 Positive Edge Interrupt Did Not Occur					
4	IFR14	R/W	1 = PE50 Positive Edge Interrupt Occurred					
			0 = PE50 Positive Edge Interrupt Did Not Occur					
3	IFR13	R/W	1 = NE47 Negative Edge Interrupt Occurred					
			0 = NE47 Negative Edge Interrupt Did Not Occur					
2	IFR12	R/W	1 = NE46 Negative Edge Interrupt Occurred					
			0 = NE46 Negative Edge Interrupt Did Not Occur					
1	IFR11	R/W	1 = PE45 Positive Edge Interrupt Occurred					
			0 = PE45 Positive Edge Interrupt Did Not Occur					
0	IFR10	R/W	1 = PE44 Positive Edge Interrupt Occurred					
			0 = PE44 Positive Edge Interrupt Did Not Occur					

2.6.2 Interrupt Flag Register One (IFR2) Description

Address = $0008		IFR2: Interrupt Flag Register Two					Reset Value = 0x00	
7:0->	IFR27	IFR26	IFR25	IFR24	IFR23	IFR22	IFR21	IFR20
Bit	**Name**	**Access**	**Description**					
7	IFR27	R/W	1 = IRQ2B Low Level Interrupt Occurred					
			0 = IRQ2B Low Level Interrupt Did Not Occur					
6	IFR26	R/W	1 = IRQ1B Low Level Interrupt Occurred					
			0 = IRQ1B Low Level Interrupt Did Not Occur					
5	IFR25	R/W	1 = Timer 2 Edge Interrupt Occurred					
			0 = Timer 2 Edge Interrupt Did Not Occur					
4	IFR24	R/W	1 = Timer 1 Edge Interrupt Occurred					
			0 = Timer 1 Edge Interrupt Did Not Occur					
3	IFR23	R/W	1 = NE57 Negative Edge Interrupt Occurred					
			0 = NE57 Negative Edge Interrupt Did Not Occur					
2	IFR22	R/W	1 = PE56 Positive Edge Interrupt Occurred					
			0 = PE56 Positive Edge Interrupt Did Not Occur					
1	IFR21	R/W	1 = PE55 Positive Edge Interrupt Occurred					
			0 = PE55 Positive Edge Interrupt Did Not Occur					
0	IFR20	R/W	1 = PE54 Positive Edge Interrupt Occurred					
			0 = PE54 Positive Edge Interrupt Did Not Occur					

2.7 Interrupt Enable Registers (IER1, IER2) ($002D, $0009)

IER1 and IER2 are the interrupt enable registers. Reading an IER register reads its contents and puts the value on the internal data bus. Writing an IER writes a value from the data bus into the register. Setting a bit in an IER to "1" permits the interrupt corresponding to the same bit in the IFR to cause a processor interrupt. Also, if the RUN pin was low prior to the interrupt, the pin will go high if BCR3 = 0.

2.7.1 Interrupt Enable Register One (IER1) Description

Address = $002D		IFR1: Interrupt Enable Register One					Reset Value = 0x00	
7:0->	IER17	IER16	IER15	IER14	IER13	IER12	IER11	IER10
Bit	**Name**	**Access**	**Description**					
7	IER17	R/W	1 = NE53 Negative Edge Interrupt Enabled					
			0 = NE53 Negative Edge Interrupt Disabled					
6	IER16	R/W	1 = NE52 Negative Edge Interrupt Enabled					
			0 = NE52 Negative Edge Interrupt Disabled					
5	IER15	R/W	1 = PE51 Positive Edge Interrupt Enabled					
			0 = PE51 Positive Edge Interrupt Disabled					
4	IER14	R/W	1 = PE50 Positive Edge Interrupt Enabled					
			0 = PE50 Positive Edge Interrupt Disabled					
3	IER13	R/W	1 = NE47 Negative Edge Interrupt Enabled					
			0 = NE47 Negative Edge Interrupt Disabled					
2	IER12	R/W	1 = NE46 Negative Edge Interrupt Enabled					
			0 = NE46 Negative Edge Interrupt Disabled					
1	IER11	R/W	1 = PE45 Positive Edge Interrupt Enabled					
			0 = PE45 Positive Edge Interrupt Disabled					
0	IER10	R/W	1 = PE44 Positive Edge Interrupt Enabled					
			0 = PE44 Positive Edge Interrupt Disabled					

2.7.2 Interrupt Flag Register One (IER2) Description

Address = $0009		IFR2: Interrupt Enable Register Two					Reset Value = 0x00	
7:0->	IER27	IER26	IER25	IER24	IER23	IER22	IER21	IER20
Bit	**Name**	**Access**	**Description**					
7	IER27	R/W	1 = IRQ2B Low Level Interrupt Enabled					
			0 = IRQ2B Low Level Interrupt Disabled					
6	IER26	R/W	1 = IRQ1B Low Level Interrupt Enabled					
			0 = IRQ1B Low Level Interrupt Disabled					
5	IER25	R/W	1 = Timer 2 Edge Interrupt Enabled					
			0 = Timer 2 Edge Interrupt Disabled					
4	IER24	R/W	1 = Timer 1 Edge Interrupt Enabled					
			0 = Timer 1 Edge Interrupt Disabled					
3	IER23	R/W	1 = NE57 Negative Edge Interrupt Enabled					
			0 = NE57 Negative Edge Interrupt Disabled					
2	IER22	R/W	1 = PE56 Positive Edge Interrupt Enabled					
			0 = PE56 Positive Edge Interrupt Disabled					
1	IER21	R/W	1 = PE55 Positive Edge Interrupt Enabled					
			0 = PE55 Positive Edge Interrupt Disabled					
0	IER20	R/W	1 = PE54 Positive Edge Interrupt Enabled					
			0 = PE54 Positive Edge Interrupt Disabled					

2.8 Universal Asynchronous Receiver/Transmitters (UARTs)

The W65C134S has one full duplex Universal Asynchronous Receiver/Transmitter (UART) with programmable bit rates. The serial I/O functions are controlled by the Asynchronous Communication Control and Status Registers (ACSR). The serial bit rate is determined by Timer A for all modes for the UART's. The maximum data rate using the internal clock is 0.5MHz bits per second (FCLK = 8MHz). The Asynchronous Transmitter and Asynchronous Receiver can be independently enabled or disabled.

All transmitter and receiver bit rates will occur at one sixteenth of Timer A as selected.

Whenever Timer A is required as a timing source, it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Table 2.8.6-1 for a table of hexadecimal values that represent the desired data rate.

Standard UART Features

- 7 or 8 bit data with or without Odd or Even parity.
- The Transmitter has 1 stop bit with parity or 2 stop bits without parity.
- The Receiver requires only 1 stop bit for all modes.
- Both the Receiver and Transmitter have priority encoded interrupts for service routines.
- The Receiver has error detection for parity error, framing error, or over-run error conditions that may require re-transmission of the message.
- The Receiver Interrupt occurs due to a receiver data register full condition.
- The Transmitter Interrupt can be selected to occur on either the data register empty (end-of-byte transmission) or both the data register empty and the shift register empty (end-of-message transmission) condition.

2.8.1 Transmitter Operation

The transmitter operation is controlled by the Asynchronous Control and Status Register (ACSR). The transmitter automatically adds a start bit, parity bit and one or two stop bits as defined by the ACSR. A word of transmitted data is 7 or 8 bits of data.

The Transmitter Data Register (ARTD) is located at addresses $ and is loaded on a write. The Receiver is read at this same address.

2.8.2 UART Data Register Description

Address = $0023		ARTDx: UART Data Register					Reset Value = 0x00	
7:0->	ARTDx7	ARTDx6	ARTDx5	ARTDx4	ARTDx3	ARTDx2	ARTDx1	ARTDx0
Bit	**Name**	**Access**	**Description**					
7 - 0	**ARTDx** [7-0]	R/W	R = Read Receiver Data Register					
			W = Write Transmitter Data Register					

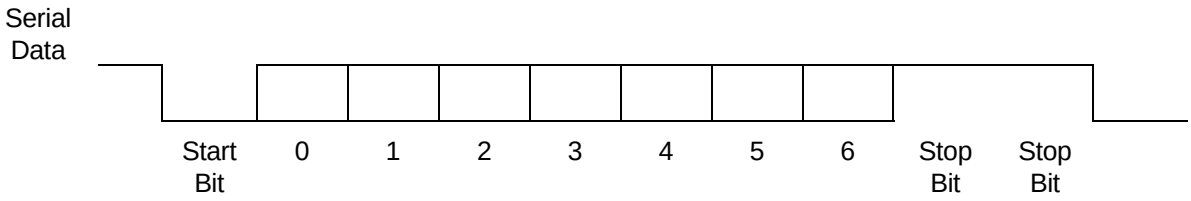
2.8.3 Transmitter Mode with Parity

The Transmitter Interrupt is controlled by the Asynchronous Control Status Register bit ACSRx1.

IRQATx = ACSRx0 ((ACSRx1B) (DATA REGISTER EMPTY) + (ACSRx1) (DATA REGISTER AND SHIFT REGISTER EMPTY))

2.8.4 Receiver Operation

The receiver and its selected control and status functions are enabled when ACSRx5 is set to a "1". The data format must have a start bit, 7 or 8 data bits, and one stop bit or one parity bit and one stop bit. The receiver bit period is divided into 16 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit, and a strobe signal is generated at the approximate center of each incoming bit. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. A framing error, parity error or an over-run will set ASCRx7 the receiver error detection bit. An over-run condition occurs when the receiver data register has not been read and new data byte is transferred from the receiver shift register.



2.8.5 Data Timing for 7-bit Data without Parity and two stop bits.

The receiver requires only one stop bit but the transmitter supplies two stop bits for older system timing.

A receiver interrupt (IRQARx) is generated whenever the receiver shift register is transferred to the receiver data register.

2.8.6 UART RXD and TXD Data Rate Generation.

Timer 3 and 4 provide clock timing for the RXD and TXD data rate. Timer 3 and 4 operate as configured by Timer Control Register (TCRx) and Timer Enable Register (TERx) should be set up prior to enabling the UARTx.

The table below identifies the values to be loaded into Timer 3 and 4 to select standard data rates. Any data rate can be selected by using the formula:

N = (FCLK / (16 x bps)) - 1

N = decimal value to be loaded into timer using its hexadecimal equivalent
FCLK = the clock frequency
bps = bits per second data rate

Note that one may notice slight differences between the standard rate and the actual data rate. However, transmitter and receiver error of 1.5% or less is acceptable.

Table 2.9.6-1 Timer 3 and 4 Values for Baud Rate Selection

Standard Baud Rate	1.8432MHz	2.4576MHz	3.6864MHz	4.9152MHz	6.1440MHz
110	$0416	$0573	$082E	$0AE8	$0DA2
150	$02FF	$03FF	$05FF	$07FF	$09FF
300	$017F	$01FF	$02FF	$03FF	$04FF
600	$00BF	$00FF	$017F	$01FF	$027F
1200	$005F	$007F	$00BF	$00FF	$013F
1800	$003F	$0054	$007F	$00AA	$00DF
2400	$002F	$003F	$005F	$007F	$009F
4800	$0017	$001F	$002F	$003F	$004F
9600	$000B	$000F	$0017	$001F	$0027
19200	$0005	$0007	$000B	$000F	$0013
38400	$0002	$0003	$0005	$0007	$0009
57600	$0001	$0002	$0003	$0004	$0006

Note: Shading indicates transmitter or receiver error greater than 1.5%.

2.8.7 Asynchronous Control and Status Registers (ACSR) Description

The Asynchronous Control and Status Register (ACSR) enables the Receiver and Transmitter and holds information on communication status error conditions.

Address = $0022		ACSR: Asynchronous Control and Status Register					Reset Value = 0x00	
7:0->	ACSR7	ACSR6	ACSR5	ACSR4	ACSR3	ACSR2	ACSR1	ACSR0
Bit	**Name**	**Access**	**Description**					
7	ACSR7	R/W	1 = Receiver Error Flag. The Receiver logic detects three possible error conditions and sets ACSR7: parity, framing or over-run. A parity error occurs when the parity bit received does not match the parity generated on the receive data. A framing error occurs when the stop bit time finds a "0" instead of a "1". An over-run occurs when the last data in the Receiver Data Register has not been read and new data is transferred from the Receive Shift Register.						
			0 = Cleared by writing a "1" to ACSR7. Writing a "0" to ACSR7 has not effect on ACSR7.						
6	ACSR6	R/W	1 = Software Semaphore. ACSRx6 may be used for communications among routines which access the UART. This bit has no effect on the UART operation. The bit can be thought of as a manually set busy signal.						
			0 = User defined.						
5	ACSR5	R/W	1 = Enable Receiver, Receiver Interrupt, and RXD output on Port 6.						
			0 = Disable Receiver.						
4	ACSR4	R/W	1 = Even parity is enabled. Even parity is when the number of ones in the data register plus parity bit equal an even number of "1's".						
			0 = Odd parity is enabled. Odd parity is generated where the number of ones is the data register plus parity bit equal an odd number of "1's".						
3	ACSR3	R/W	1 = Enable Parity.						
			0 = Disable Parity						
2	ACSR2	R/W	1 = Transmitter and Receiver send and receive 8-bit data. The Transmitter sends 11 bits of information (one start, 8 data, one parity and one stop or two stop bits). The Receiver receives 10 or 11 bits of information (one start, 8 data, one stop or one parity and one stop bit).						
			0 = Transmitter and Receiver send and receive 7-bit data. The Transmitter sends a total of 10 bits of information (one start, 7 data, one parity and one stop or 2 stop bits). The Receiver receives 9 or 10 bits of information (one start, 7 data, and one stop or one stop and one parity bits). When writing to the Transmitter in seven bit mode, bit 7 is discarded. When reading from the receive data register during seven bit mode, bit 7 is always zero.						
1	ACSR1	R/W	1 = Transmitter Interrupt occurs due to both the Transmitter Data and Shift register empty condition (end-of-message transmission. ACSR0 = 0 clears this bit if set.						
			0 = Transmitter Interrupt occurs due to a Transmitter Data Register Empty condition (end-of-byte transmission).						
0	ACSR0	R/W	1 = Enable Transmitter, Transmitter Interrupt, and TXD on Port 6						
			0 = Disable transmitter, Transmitter Interrupt, and TXD on Port 6						

2.9 The Serial Interface Bus (SIB)

The Serial Interface Bus (SIB) is configured as a token passing Local Area Network, and is intended for inter-chip communications in parallel processing applications. The Serial Interface Bus has four pins associated with its use: CHIN CHOUT, SDAT, and SCLK (see Section 2.19 for more information). The SIB has seven (7) registers associated with its use: STATE, SR0, SR1, SR2, SR3, SCSR, and BAR.

2.9.1 The STATE Register

The STATE register is a read-only register that provides the host processor with the timing state of the SIB (see Figure 1-13 for more information on activities during each timing state). The STATE register is the decoded output of a "state machine" that counts up from 0 to 37 and then back to 0 on positive transitions of SCLK. Only one decoded output is asserted at a time. STATE has the same value at the same time in all devices and is used to synchronize message transfer. It is reset to State 0 upon system RESET.

STATE is normally read only during manufacturing test. A read of the state register can produce invalid results if the SCLK is not synchronous with the processor clock. When the SCLK is enabled on the chip with its MPU, it is always synchronized with the SIB.

2.9.2 STATE Register (STATE) Description

Address = $0014		STATE: State Register					Reset Value = 0x00	
7:0->	STATE7	STATE6	STATE5	STATE4	STATE3	STATE2	STATE1	STATE0
Bit	**Name**	**Access**	**Description**					
7	STATE7	R/W	1 = Never					
			0 = Always 0					
6	STATE6	R/W	1 = State 37					
			0 = Not state 37					
5	STATE5	R/W	1 = State 36					
			0 = Not state 36					
4	STATE4	R/W	1 = State 35					
			0 = Not state 35					
3	STATE3	R/W	1 = State 3 through 34					
			0 = Not state 3 through 34					
2	STATE2	R/W	1 = State 2					
			0 = Not state 2					
1	STATE1	R/W	1 = State 1					
			0 = Not state 1					
0	STATE0	R/W	1 = State 0					
			0 = Not state 0					

2.9.3 SR0, SR1, SR2, and SR3 Shift Register

The SR0, SR1, SR2, and SR3 are the four (4) 8-bit shift registers (32-bit shift register) that are used to transfer messages from one SIB to another SIB on a token passing ring network. Two to eight SIB's may be connected together (see Figure 1-14 Serial Interface Bus (SIB) Wiring Diagram for more information).

SR3 bits SR37, SR36 and SR35 are the Bus Address Register field of the 32-bit message. All other bits are command, data, or address fields. Reading SR3 clears the read pending bit SCSR4 and writing SR0 clears the write pending bit SCSR0.

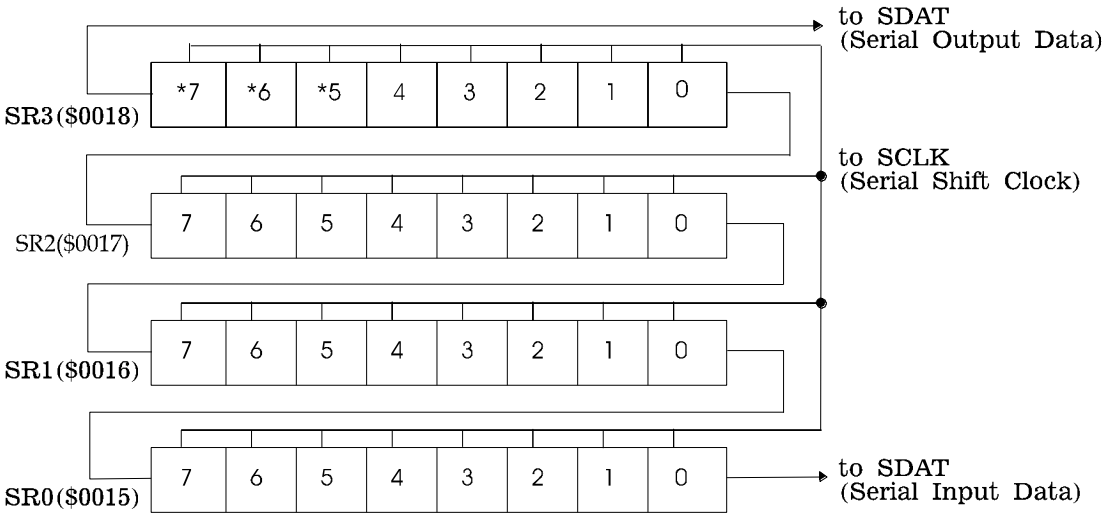


Figure 2.9.3-1 SR0, SR1, SR2, and SR3 Shift Register

2.9.4 SIB Shift Register Description

Address = $0015-18		SR0, SR1, SR2, SR3: SIB Data Register					Reset Value = xx	
7:0->	SRx7	SRx6	SRx5	SRx4	SRx3	SRx2	SRx1	SRx0
Bit	**Name**	**Access**	**Description**					
7 - 0	**SRx**[7-0]	R/W	R = Read Receiver Data Register					
			W = Write Transmitter Data Register					

2.9.5 SIB Control and Status Register (SCSR)

The SIB Control and Status Register (SCSR) is used for controlling the SIB and for reading the status of the SIB. The SCSR is writable only in the sense that a high level can be written to bits SCSR0, SCSR2, SCSR6 and SCSR7. Together with the STATE Register, it gives the state of the SIB controller. Bit SCSR6 is used to enable PHI2 as the clock source for SCLK, bits SCSR4 and SCSR5 are used for receiving, bits SCSR0, SCSR1, and SCSR2 are used for sending, and STATE is used for both. The SCSR is reset on a system RESET.

Address = $0022		SCSR: SIB Control and Status Register					Reset Value = 0x00	
7:0->	SCSR7	SCSR6	SCSR5	SCSR4	SCSR3	SCSR2	SCSR1	SCSR0

Bit	Name	Access	Description
7	SCSR7	R/ W=1 Clears	1 = SIB interrupted. Cleared by a write of a "1" to SCSR7. A write of a "0" has no effect. The SIB causes a SIBIRQ (SIB interrupt) when the SIB enable bit of the Bus Control Register is set (BCR2=1) and SCSR1=1 (SIB master is set), or SCSR3=1 (SIB message not acknowledged), or SCSR4=1 (reading pending). SIBIRQ=BCR2 (SCSR1+SCSR3+SCSR4)
			0 = SIB did not interrupt.
6	SCSR6	R/W	1 = SIB Clock Enabled. "Serial clock enable" control bit.
			0 = Clock Disabled.
5	SCSR5	R/W	1 = SIB cannot receive a message in progress because when the message started, its processor had not read its previous message. "Deaf" status bit.
			0 = SIB ready to receive a message.
4	SCSR4	R/W	1 = Set to a "1" due to a match between the incoming message BAR field with the BAR, this means that the SIB has received a message but its processor has not yet finished reading it. "Read pending" status bit.
			0 = SIB waiting to receive a message
3	SCSR3	R/W	1 = Set to a "1" by the SIB logic due to SDAT equals a "1" during timing state 36, this means that the last message this SIB sent was not acknowledged by the receiver whose address matches the Bus Address Register (BAR) field of the message (SR35, SR36 and SR37). “Message not acknowledged” status bit.
			0 = Message was acknowledged.
2	SCSR2	R/W	1 = Set to a "1", this means that the SIB was master before the last time mastery changed. One device is chosen as previous master (one MPU on the network writes a "1" to SCSR2) before the first message is sent. SCSR2 is set to a "1" for one SIB on the network as part of system initialization upon power up or reset. This bit is ignored during normal system operation. “Previous master” status bit.
			0 = Normal operating state.
1	SCSR1	R/W	1 = Set to a "1" this means that the SIB's microprocessor was requesting master (SCSR0 was set to a "1") just before the last time mastery changed. If CHIN (CHain IN) is high as well then this device is master when the "token" is passed, “master status” bit.
			0 = Not requesting to be master.
0	SCSR0	R/W	1 = Set to a "1" by the on-chip microprocessor, it means that the processor wants to send a message, “write pending" status bit.
			0 = Cleared when SR0 is written.

2.9.6 Sequence of events for the SIB message transmission.

State 0 events (STATE=$01) The SIB controllers wait for some device to request mastery. All devices on the serial bus wait for one or more devices to request mastery. At any time any processor with data to send sets SCSR0 (write pending) and the SIB is in state 0 (STATE=$01) then the following occurs:

1. SCLK stops running.
2. Each device with SCSR0=1 pulls SDAT low to request SCLK.
3. SCLK restarts and advances the state machine to state 1 (STATE=$02).

State 1 events (STATE=$02)

The SIB controllers establish mastery for this message. State 1 determines which devices is master for this message and insures that SDAT is high on transition to state 2 (STATE=$04) in state 1 (STATE=$02) the following occurs:

1. The device that was master just before transition to state 1 sets SCSR2 (previous master), and all other devices reset SCSR2.
2. The device with SCSR2 set to a "1" makes its CHOUT high. Other devices only make CHOUT high if both their CHIN is high and SCSR0=0. Thus the first device in the chain after the previous master that has write pending (SCSR0=1) is the master for this message.
3. The device that is master for this message outputs a high level on SDAT.
4. SCLK advances to state 2 (STATE=$04).

State 2 events (STATE=$04)

The master's SIB controller waits for data from its processor. The SIB waits in state 2 (STATE=$04) for the master to load its data and the following occurs:

1. SCLK stops running.
2. The SIB controller that is master sets SCSR7 to interrupt and signal its processor that it has acquired mastery.
3. In response to the interrupt the processor should:
   a) check "read pending" (SCSR4) to see if it has received a message before acquiring mastery, and if so read it, thus clearing SCSR4;
   b) check "message not acknowledged" SCSR3 to see if the last message it sent was not acknowledged;
   c) place the data it wants to send in SR0, SR1, SR2, and SR3, and;
   d) clear "write pending" SCSR0 to signal the SIB controller that data is there to send. This happens on the trailing edge of the write to SR0 so SR0 must be the last byte written into the shift register.
4. The master pulls SDAT low to request SCLK.
5. After at least one-half-cycle, SCLK advances the state counter to state 3 (STATE=$08).

States 3 through 34 events (STATE=$08)

The message is sent. During state 3 through 34 (STATE=$08) the SIB transfers the message from the master's shift register to all devices that have read their previous messages.

1. Any device that had "read pending" (SCSR4=1) just before transition to state 3 sets "deaf" SCSR5, so that it cannot receive the incoming message on top of the one its processor has not read.
2. While in state 3-34 (STATE=$08) the device that is master sends its shift-register data output onto SDAT.
3. Any device that does not have "deaf" SCSR5 set, including the master, advances its shift register, on SCLK positive transitions, thus acquiring the data that was in the master's shift-register.
4. SCLK advances the state counter to state 35 (STATE=$10).

State 35 events (STATE=$10)

The SIB is prepared for acknowledgement. State 35 (STATE=$10) is for the master to insure that SDAT is high on entry to state 36 (STATE=$20). The device that is master outputs a high level on SDAT. SCLK advances the state counter to state 36 (STATE=$20).

State 36 events (STATE=$20)

The receiver should acknowledge its receipt of the message in state 36 (STATE=$20). When asserted, the destination device (the device that has SR37, SR36, SR35 equal to BAR2, BAR1, BAR0 and "deaf" SCSR5=0) pulls SDAT low to acknowledge reception to the master. SCLK advances the state counter to state 37 (STATE=$40).

State 37 events (STATE=$40)

The MPU's are interrupted with the result of transmission in the SR's. State 37 (STATE=$40) is for the master to interrupt and signal its processor if the message it sent was not acknowledged, for the receiver to interrupt and signal its processor that a message is available to read, and for the master to insure that SDAT is high on transition to state 0 (STATE=$01). In state 37 (STATE=$40) the following occurs:

1. If the master saw SDAT high just before the transition to state 37 (STATE=$40) (meaning there was no acknowledgement) then it sets SCSR3 "message not acknowledged" to interrupt and signal its processor that the message was not received. If the master saw SDAT low just before the transition to state 37 (STATE=$40) (meaning there was acknowledgement) then SCSR3 is cleared and does not interrupt its processor.
2. The device with SCSR5=0 that has the SR37,6,5=BAR2,1,0 (message with its address), sets SCSR4 "read pending" to interrupt and signal its processor that a message is pending.
3. The master outputs a high level on SDAT for the duration of state 37 (STATE=$40).
4. SCLK advances the state counter to state 0 (STATE=$01).

Message processing may now be performed by the receiver. The message is read by the receiver's processor in response to the SIB interrupt (SIBIRQ) generated by SCSR4 "read pending", by reading the message in its shift register, and when finished clears SCSR4 "read pending" (on the trailing edge of the read of SR3).

The message may now be processed. The next message may now be sent on the SIB.

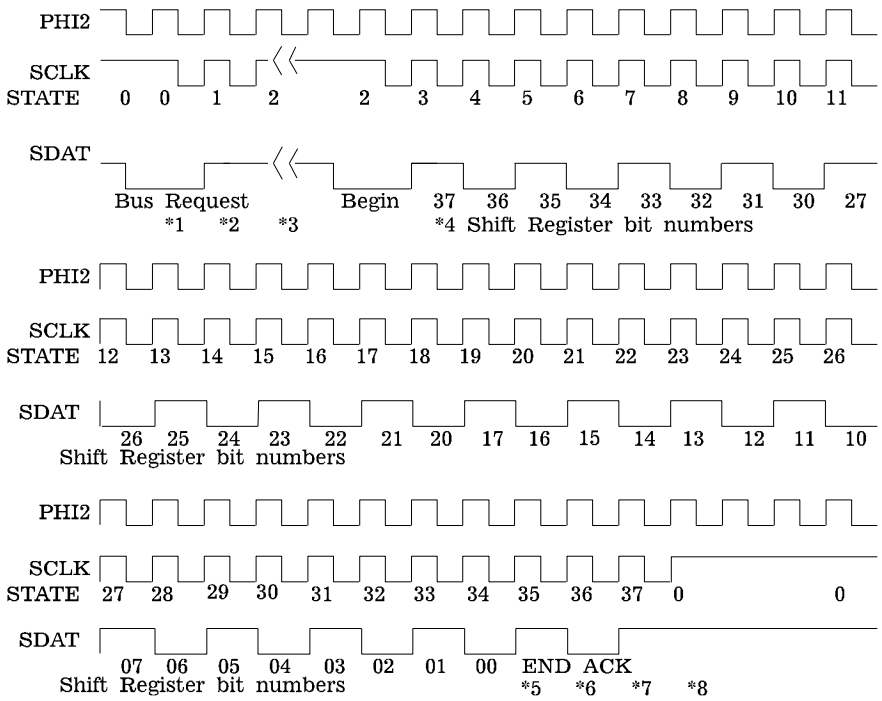


Figure 2.9.6-1 Serial Interface Bus (SIB) Message Transmission Timing Diagram

Bus Address Register (BAR)

The Bus Address Register (BAR) contains the address that is used by the receive function logic of the SIB to compare against the "address field" (SR37, SR36 and SR35) of the Shift Register incoming data. When the BAR address matches the "address field" of the Shift Register the host is interrupted indicating that a "message has been received".

*1 The SDAT goes low due to SCSR0 (write pending) set in all devices that are requesting the bus.

*2 The previous master sets SCSR2 (previous master) and sets CHOUT high, all others clear SCSR2. The next device with CHIN high and SCSR0 set becomes bus master, and clears CHOUT to low.

*3 The bus master interrupts its MPU and the MPU loads the shift register. Writing to SR0 clears SCSR0 (write pending) and sends the message. The SIB waits until the shift register SR0 is written. Any device that has SCSR4 set (read pending), sets SCSR5 (deaf) indicating the MPU never read the last message sent to it. Reading SR3 clears SCSR4 (read pending).

*4 The 32-bit message is sent by the bus master during states 3-34. The BEGIN low time begins on the transfer of data to the masters shift register during state 2 and stays low until the first transmit data bit time in state 3. The output data is transferred on the rising edge of SCLK with the input data latched on the falling edge of SCLK.

*5 The bus master sets SDAT to '1' signaling the end of transmission.

*6 The receiver device pulls SDAT low signaling the bus master that the message was received. If the receiving device does not pull SDAT low then the bus master sets SCSR3 (message not acknowledged) indicating the message was not received, and will interrupt its MPU in the next state (State 37).

*7 The receiver sets SCSR4 (read pending) and interrupts its MPU. The bus master (sending device) outputs a high level on SDAT and interrupts its MPU if SCSR3 (message not acknowledged) was set in state 36, signaling the message was not received.

*8 Wait in state 0 for message processing and next message transmission bus request.

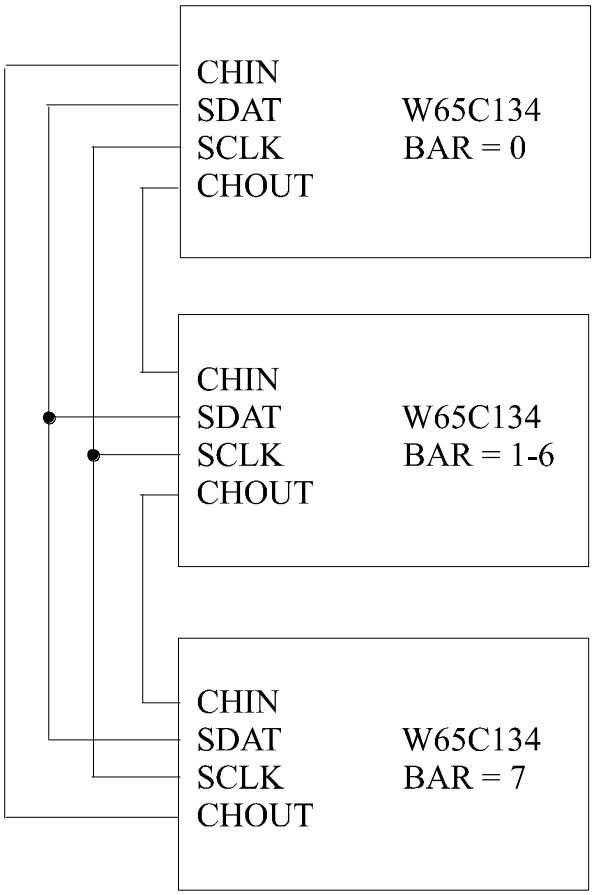


Figure 2.9.6-2 Serial Interface Bus (SIB) Wiring Diagram

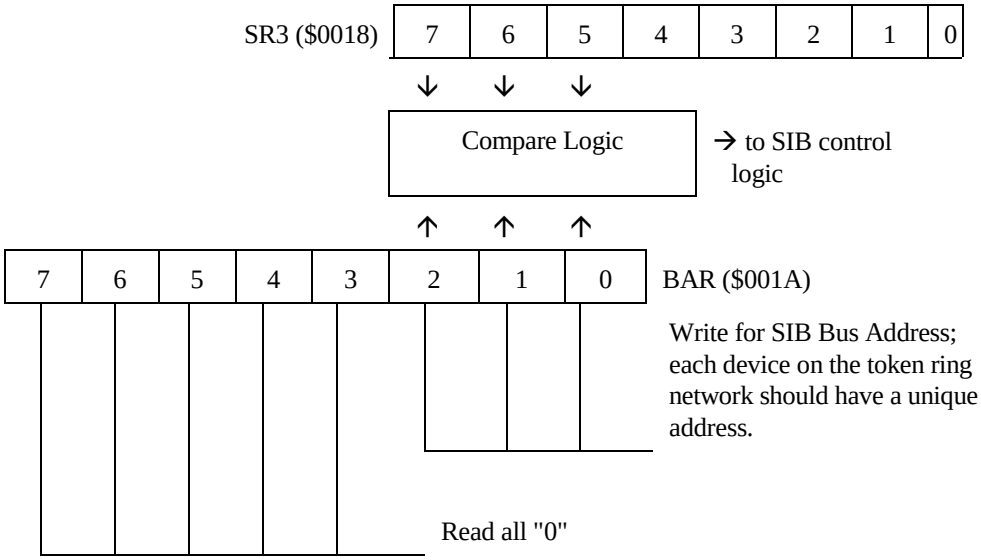


Figure 2.9.6-3 Bus Address Register (BAR)

3 Memory Map

Table 3-1 System Memory Map

Address	Label	Function
FFFF FFD0	See Table 1-5	Vector Table (See Vector Table 1-5) Chip Select (CS7B) when Internal ROM disabled by BCR7=1
FFCF F000	 ROM	On-Chip Mask ROM Chip Select (CS7B) when Internal ROM disabled by BCR7=1
EFFF 8000	 CS7B	Chip Select (CS7B) 32K block (28672 available)
7FFF 0100	 CS6B	Chip Select (CS6B) 32K block (32512 available) (Note 1)
5FFF 4000	 CS5B	Chip Select (CS5B) 8K block
3FFF 2000	 CS4B	Chip Select (CS4B) 8K block
1FFF 0100	 CS3B	Chip Select (CS3B) 8K block (7836 available) (Note 1)
01FF 0140	 STACK	On-Chip Stack RAM (same as 0040-00FF) when PCS33=0 and PCS36=0 (On-Chip Stack)
013F 0120	 CS2B	Chip Select (CS2B) 32 Bytes
011F 0100	 CS1B	Chip Select (CS1B) 32 Bytes
00FF 0040	 RAM	On-Chip RAM
003F 0030	 CS0B	Chip Select (CS0B) 16 Bytes
002F 0000	See Table 1-4	On-Chip I/O (See I/O Memory Map Table 1-4)

Note 1: When PCS31=1 and/or PCS32=1 then CS1B and/or CS2B are active. CS3B's and CS6B's memory spaces are reduced by CS1B and/or CS2B memory space in order to prevent external bus conflicts.

Table 3-2 I/O Memory Map

Address	Label	Function	Reset Value
002F	----	Reserved	uninitialized
002E	----	Reserved	uninitialized
002D	IER1	Interrupt Enable Register One	$00
002C	IFR1	Interrupt Flag Register One	$00
002B	TMCH	Timer M Counter High (read only)	uninitialized
002A	TMCL	Timer M Counter Low (read only)	uninitialized
0029	TMLH	Timer M Latch High	uninitialized
0028	TMLL	Timer M Latch Low	uninitialized
0027	TACH	Timer A Counter High	uninitialized
0026	TACL	Timer A Counter Low	uninitialized
0025	TALH	Timer A Latch High	uninitialized
0024	TALL	Timer A Latch Low	uninitialized
0023	ARTD	UART RXD/TXD Data Register	uninitialized
0022	ACSR	UART RXD/TXD Control/Status Register	$00
0021	PDD6	Port 6 Data Direction Register	$00
0020	PD6	Port 6 Data Register	$00
001F	PDD5	Port 5 Data Direction Register	$00
001E	PDD4	Port 4 Data Direction Register	$00
001D	PD5	Port 5 Data Register	$00
001C	PD4	Port 4 Data Register	$00
001B	BCR	Bus Control Register	$00/$89
001A	BAR	SIB Address Register	$00
0019	SCSR	SIB Control and Status Register	$00
0018	SR3	SIB Shift Register 3	uninitialized
0017	SR2	SIB Shift Register 2	uninitialized
0016	SR1	SIB Shift Register 1	uninitialized
0015	SR0	SIB Shift Register 0	uninitialized
0014	STATE	SIB State Register (read only)	$01
0013	T2CH	Timer 2 Counter High	uninitialized
0012	T2CL	Timer 2 Counter Low	uninitialized
0011	T1CH	Timer 1 Counter High	uninitialized
0010	T1CL	Timer 1 Counter Low	uninitialized
000F	T2LH	Timer 2 Latch High	uninitialized
000E	T2LL	Timer 2 Latch Low	uninitialized
000D	T1LH	Timer 1 Latch High	uninitialized
000C	T1LL	Timer 1 Latch Low	uninitialized
000B	TCR2	Timer Control Register Two	$00
000A	TCR1	Timer Control Register One	$00
0009	IER2	Interrupt Enable Register Two	$00
0008	IFR2	Interrupt Flag Register Two	$00
0007	PCS3	Port 3 Chip Select Register	$00
0006	PDD2	Port 2 Data Direction Register	$00
0005	PDD1	Port 1 Data Direction Register	$00
0004	PDD0	Port 0 Data Direction Register	$00
0003	PD3	Port 3 Data Register	$FF
0002	PD2	Port 2 Data Register	$00
0001	PD1	Port 1 Data Register	$00
0000	PD0	Port 0 Data Register	$00

Table 3-3 Vector Table

Address	Label	Function
FFFF,E	IRQBRK	BRK Vector High, Low
FFFD,C	IRQRES	RES Vector High, Low
FFFB,A	NMI	Non-Maskable Interrupt Vector High, Low
FFF9,8	IRQ2	IRQ2 Vector High, Low
FFF7,6	IRQ1	IRQ1 Vector High, Low
FFF5,4	IRQT2	Timer 2 Interrupt Vector High, Low
FFF3,2	IRQT1	Timer 1 Interrupt Vector High, Low
FFF1,0	NE57	Negative Edge Interrupt Vector High, Low
FFEF,E	PE56	Positive Edge Interrupt Vector High, Low
FFED,C	PE55	Positive Edge Interrupt Vector High, Low
FFEB,A	PE54	Positive Edge Interrupt Vector High, Low
FFE9,8	IRQSIB	SIB Interrupt Vector High, Low
FFE7,6	IRQAR	Asynchronous RXD Interrupt Vector High, Low
FFE5,4	IRQAT	Asynch, TXD or Timer A Interrupt Vector High, Low
FFE3,2	----	Reserved
FFE1,0	----	Reserved
FFDF,E	NE53	Negative Edge Interrupt Vector High, Low
FFDD,C	NE52	Negative Edge Interrupt Vector High, Low
FFDB,A	PE51	Positive Edge Interrupt Vector High, Low
FFD9,8	PE50	Positive Edge Interrupt Vector High, Low
FFD7,6	NE47	Negative Edge Interrupt Vector High, Low
FFD5,4	NE46	Negative Edge Interrupt Vector High, Low
FFD3,2	PE45	Positive Edge Interrupt Vector High, Low
FFD1,0	PE44	Positive Edge Interrupt Vector High, Low

4 Pin List

Table 4-1 68 Lead Pin Map (continued on next page)

Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
1	P57	BCR5	P57	NE57
2	P60	ACSR5	P60	RXD
		TCR14		TIN
3	P61	ACSR0	P61	TXD
		TCR15		TOUT
4	P62	----	P62	P62
5	P63	----	P63	P63
6	P64	BCR2	P64	SCLK
7	P65	BCR2	P65	SDAT
8	P66	BCR2	P66	CHIN
9	P67	BCR2	P67	CHOUT
10	RESB	----	RESB	RESB
11	WEB	----	WEB	WEB
12	RUN	BCR3	RUN	RUN
13	FCLKOB	----	FCLKOB	FCLKOB
14	FCLK	----	FCLK	FCLK
15	BE	----	BE	BE
16	CLK	----	CLK	CLK
17	CLKOB	----	CLKOB	CLKOB
18	PHI2	----	PHI2	PHI2
19	A0	BCR0 + 3 + 7	P00	A0
20	A1	BCR0 + 3 + 7	P01	A1
21	A2	BCR0 + 3 + 7	P02	A2
22	A3	BCR0 + 3 + 7	P03	A3
23	A4	BCR0 + 3 + 7	P04	A4
24	A5	BCR0 + 3 + 7	P05	A5
25	A6	BCR0 + 3 + 7	P06	A6
26	A7	BCR0 + 3 + 7	P07	A7
27	VSS	----	VSS	VSS
28	A8	BCR0 + 3 + 7	P10	A8
29	A9	BCR0 + 3 + 7	P11	A9
30	A10	BCR0 + 3 + 7	P12	A10
31	A11	BCR0 + 3 + 7	P13	A11
32	A12	BCR0 + 3 + 7	P14	A12
33	A13	BCR0 + 3 + 7	P15	A13
34	A14	BCR0 + 3 + 7	P16	A14

Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
35	A15	BCR0 + 3 + 7	P17	A15
36	VDD	----	VDD	VDD
37	P30	PCS30	P30	CS0B
38	P31	PCS31	P31	CS1B
39	P32	PCS32	P32	CS2B
40	P33	PCS33	P33	CS3B
41	P34	PCS34	P34	CS4B
42	P35	PCS35	P35	CS5B
43	P36	PCS36	P36	CS6B
44	P37	PCS37 + BCR7	P37	CS7B
45	D0	BCR0 + 3 + 7	P20	D0
46	D1	BCR0 + 3 + 7	P21	D1
47	D2	BCR0 + 3 + 7	P22	D2
48	D3	BCR0 + 3 + 7	P23	D3
49	D4	BCR0 + 3 + 7	P24	D4
50	D5	BCR0 + 3 + 7	P25	D5
51	D6	BCR0 + 3 + 7	P26	D6
52	D7	BCR0 + 3 + 7	P27	D7
53	VSS	----	VSS	VSS
54	P40	BCR6	P40	NMIB
55	P41	BCR6	P41	IRQ1B
56	P42	BCR6	P42	IRQ2B
57	P43	----	P43	P43
58	P44	BCR1	P44	PE44
59	P45	BCR1	P45	PE45
60	P46	BCR1	P46	NE46
61	P47	BCR1	P47	NE47
62	P50	BCR4	P50	PE50
63	P51	BCR4	P51	PE51
64	P52	BCR4	P52	NE52
65	P53	BCR4	P53	NE53
66	P54	BCR5	P54	PE54
67	P55	BCR5	P55	PE55
68	P56	BCR5	P56	PE56

5 PIN FUNCTION DESCRIPTION

W65C134S Interface Requirements

This section describes the interface requirements for the W65C134S single chip microcontroller. Figure 5-1 is the Interface Diagram for the W65C134S, while Figures 2-2 and 2-3 show the 68 lead plastic chip carrier and 80 lead quad flat pack pinout configurations, respectively.

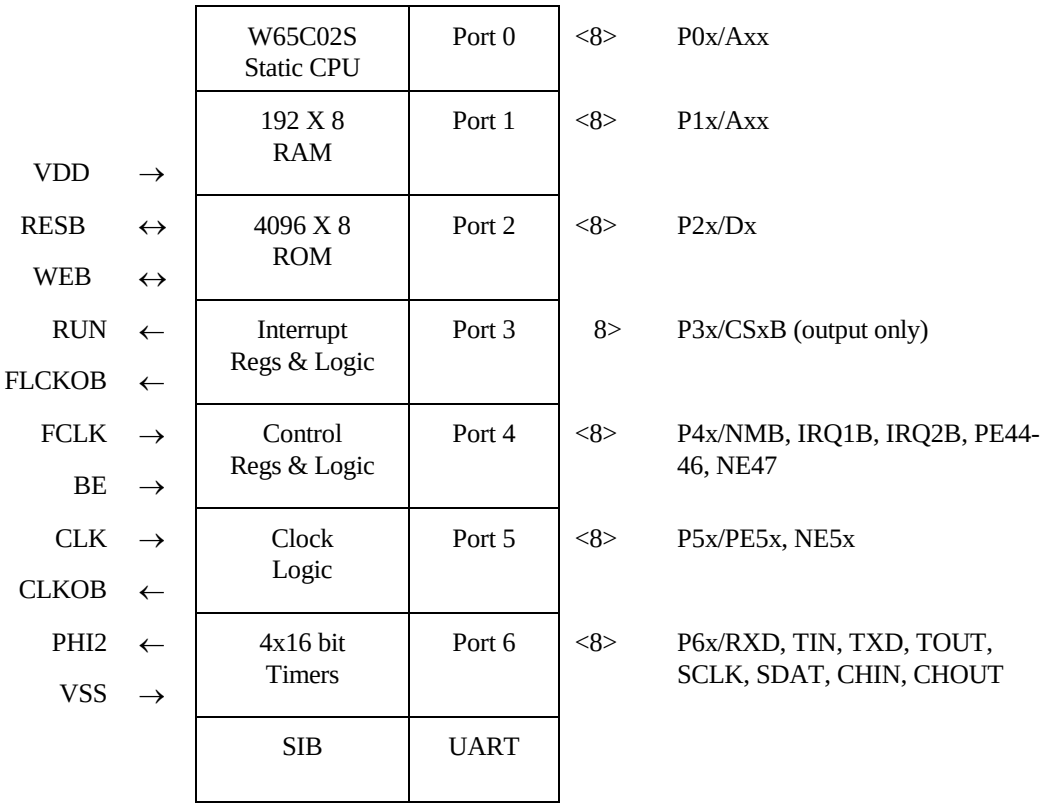


Figure 5-1 Interface Diagram

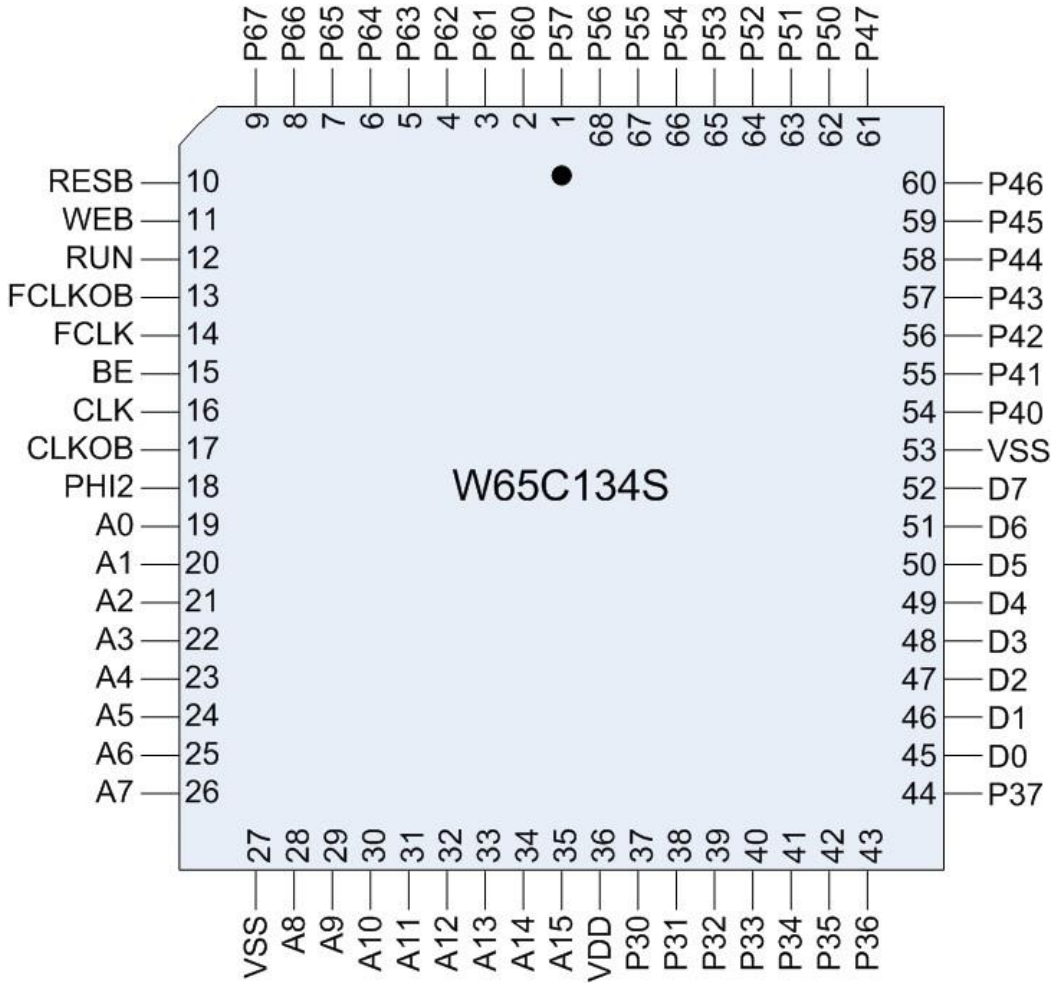


Figure 5-2 68 Lead PLCC Pinout

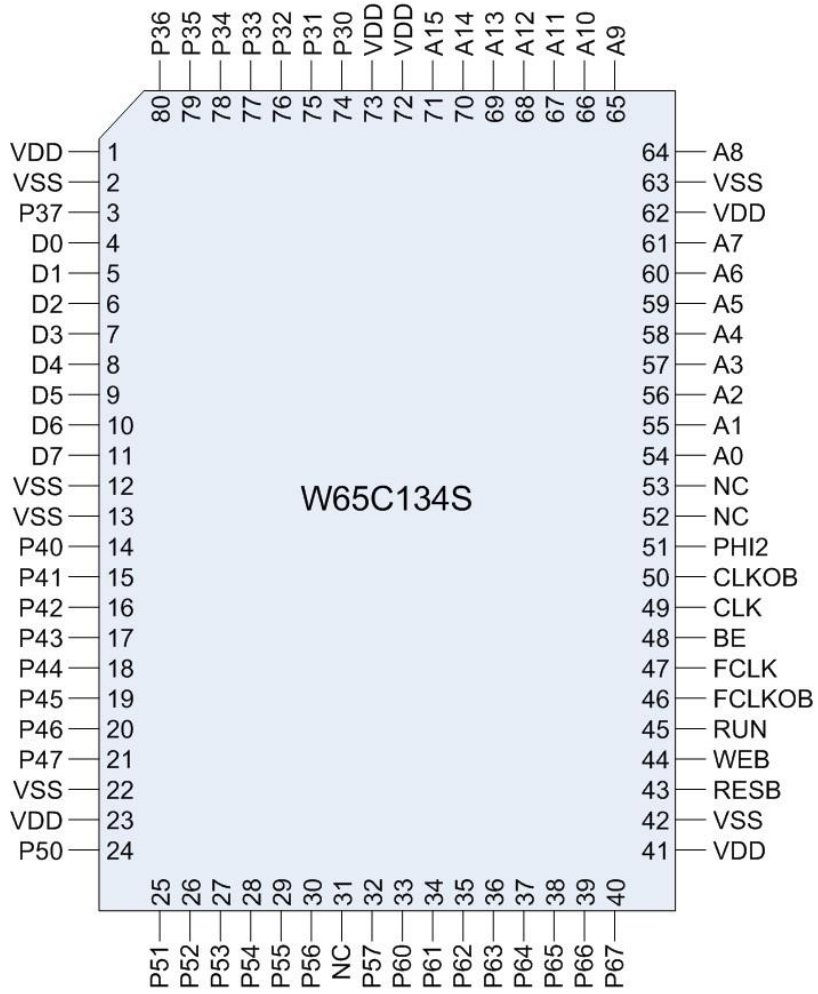


Figure 5-3 80 Lead QFP Pinout

5.1 WEB Write Enable (WEB) (active low)

The WEB signal is high when the microprocessor is reading data from external memory or I/O and high when it is reading or writing to internal memory or I/O. When WEB is low the microprocessor is writing to external memory or external I/O. The WEB signal is bidirectional; when BE is low WEB is an input for DMA operations to on-chip RAM or I/O. When BE is high during PHI2 low the internal microprocessor controls WEB.

5.2 RUN and SYNC outputs with WAI and STP defined (RUN)

The RUN function of the RUN output is pulled low as the result of a WAI or STP instruction. RUN is used to signal an external oscillator to start PHI2. The processor is stopped when RUN is low.

When BCR3=1 (test mode), the SYNC function (SYNC=1 indicates an opcode fetch) is multiplexed on RUN during PHI2 low time and RUN is multiplexed during PHI2 high time. When BCR3=0 (normal operating mode), the RUN function is output during the entire clock cycle. The test module demultiplexs RUN to provide full test capability for the RUN function. The BE input has no effect on RUN.

When RUN goes low the PHI2 signal may be stopped when high or low; however, it is recommended PHI2 stop in the high state. When RUN goes high due to an enabled interrupt or reset, the internal PHI2 clock is requested to start. The clock control function is referred to as the RUN function of RUN.

The WAI instruction pulls RUN low during PHI2 high time. RUN stays low until an enabled interrupt is requested or until RESB goes from low to high, starting the microprocessor.

The STP instruction pulls RUN low during PHI2 high time and stops the internal PHI2 clock. RUN remains low and the clock remains stopped until an enabled interrupt is requested or RESB goes from low to high.

5.3 FCLK

FCLK can be started or stopped by writing to Timer Control Register One (TCR12) bit 2. When TCR12=0 (reset forces TCR12=0), FCLK is stopped. When TCR12=1, FCLK is started. When starting FCLK oscillator, the system software should wait (100 milliseconds or an appropriate amount of time) for the oscillator to be stable before using FCLK.

5.4 Phase 2 Clock Output (PHI2)

PHI2 output is the main system clock used by the microprocessor for instruction timing, general on-chip memory, and I/O timing. PHI2 also is used by the timers when enabled for counting PHI2 clock pulse. The PHI2 clock source is either CLK or FCLK depending on the value of Timer Control Register One bit 1 (TCR11). When TCR11=0, then CLK is the PHI2 clock source. When TCR11=1, then FCLK is the PHI2 clock source.

5.5 Clock Inputs (CLK, FCLK), Clock Outputs (CLKOB, FCLKOB)

CLK and FCLK inputs are used by the timers for PHI2 system clock generation, counting events or implementing Real Time clock type functions. CLK should always be equal to or less than one-fourth the FCLK clock rate when FCLK is running (see the timer description for more information). CLKOB, FCLKOB outputs are the inverted CLK and FCLK inputs that are used for oscillator circuits that employ crystals or a resistor-capacitor time base. Timer Control Register One bit 1 (TCR11) selects if CLK (TCR11=0) or FCLK (TCR11=1) is used as the PHI2 clock source.

5.6 Bus Enable and RDY Input (BE)

BE controls the address bus, data bus and WEB signals. When RESB goes high signaling the power-up condition, the processor starts; and if BE was low when RESB went from low to high, then the Bus Control Register (BCR) bits 0, 3, and 7 (BCR0, BCR3, and BCR7) are set to 1 (emulation mode).

After RESB goes high BE controls the direction of the address bus (A0-A7, A8-A15), data bus (D0-D7) and WEB.

When BE goes low during PHI2 low time, the address bus and WEB are inputs, providing for DMA (direct memory and I/O access) for emulation purposes. Data from D0-D7 is written to any register addressed by A0-A15 when WEB is low. Data is read from D0-D7 when WEB is high. The W65C02S is stopped when BE is low.

When BE is high, the A0-A15, D0-D7 and WEB are controlled by the on-chip microprocessor.

When BE is pulled low during PHI2 high time, BE does not affect the direction of the address, data BUS and WEB signals. When BE is pulled low in PHI2 high time, the W65C02S is stopped so that the processor may be single stepped in emulation.

BE = BE (RDY + PHI2B) (This logic is on the ICE to provide the emulation interface normally used for W65C02S systems.)

Notes:

1) Address and WEB are inputs with data bus input except when reading on-chip I/O registers or memory. Use this mode for DMA.
2) W65C02S stopped with RDY function of BE pin. When BCR3=1, the W65C02S read or write of internal I/O register or memory is output on the external data bus so that the internal data bus may be traced in emulation.

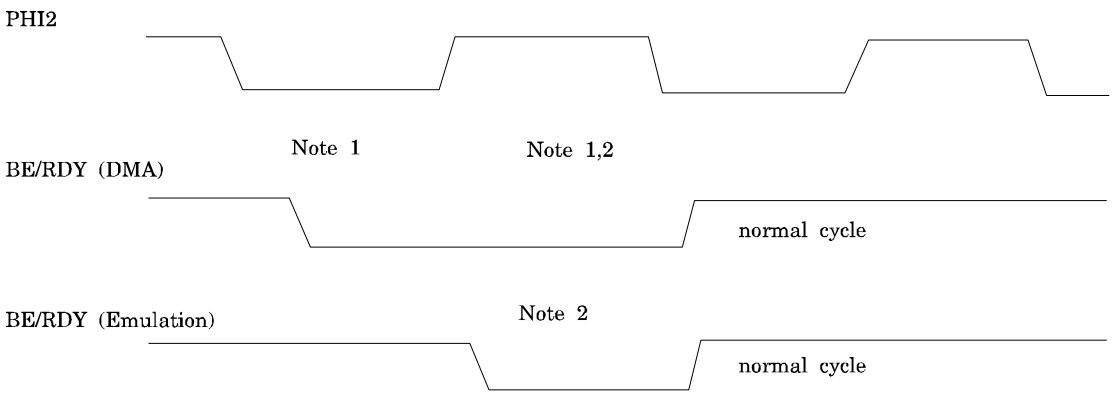


Figure 5-1 BE Timing Relative to PHI2

5.7 Reset Input/Output RESB (RESB)

When RESB is low for 2 or more processor PHI2 cycles all activity on the W65C134S stops and the chip goes into the static low power state.

After a Reset, all I/O pins become inputs. Because of NOR gates on the inputs, RESB disables all input buffers. The inputs will not float due to the bus holding devices. Inputs that are unaffected by RESB are BE and WEB.

When RESB goes from low to high, RUN goes high, the Bus Control Register is initialized to $89 if BE is low or to $00 if BE is high. The MPU then begins the power-up reset interrupt sequence in which the program counter is loaded with the reset vector that points to the first instruction to be executed. (See WDC's W65C02 microprocessor data sheet for more information and instruction timing.)

The reset sequence takes 9 cycles to complete before loading the first instruction opcode.

RESB is a bidirectional pin which is pulled low internally for "restarting" due to a "monitor time out", Timer M times out causing a system Reset. (See section 1.5, The Timers for more information.)

5.8 Positive Power Supply (VDD)

VDD is the positive power supply and has a range given in Table 6-4.

5.9 Internal Logic Ground (VSS)

VSS is the system logic ground. All voltages are referenced to this supply pin.

5.10 I/O Port Pins (Pxx)

All ports, except Port 3, which is an output only Port, are bidirectional I/O ports. Each of these bidirectional Ports has a port data register (PDx) and port data direction register (PDDx). A zero ("0") in PDDxx defines the associated I/O pin as an input with the output transistors in the "off" high impedance state. A one ("1") in PDDxx defines the I/O pin as an output. A read of PDx always reads the pin. After reset, all Port pins become input pins with both the data and data direction registers reset to 0. The inputs will not float due to the bus holding devices.

Port 3 has an associated Chip Select register (PCS3) that is used to enable Chip Selects (CSxB); this register is defined in Table 1-3 System Memory Map. A "1" in bit x of PCS3 enables Chip Select CSxB to be output over P3x while a "0" in PCS3x specifies the value in the output data register is to be output on P3x. Port 3 data register is set to all "1's" after Reset, and PCS3 is cleared to all "0's" after RESET, except if BCR7=1 then CS7B is enabled.

5.11 Address Bus (Axx)

Ports 0 and 1 are also the address bus A0-A15 when configured by the Bus Control Register (BCR). (See section 1.4 for BCR mode selection.) When BCR0 and BCR7 are set to "1" and BCR3=0 (normal operating mode) for external memory addressing, Axx are all "1's" when addressing on-chip memory. When BCR3=1 (ICE mode), the address bus is always active so that the ICE can trace internal read and write operations.

5.12 Data Bus (Dx)

Port 2 is the data bus D0-D7 when configured by the Bus Control Register (BCR). (See section 1.4 for BCR mode selection.) When BCR0 and BCR7 are set to a "1" and BCR3=0 (normal operating mode) for external memory addressing, Dx are all "1's" when addressing on-chip memory. When BCR3=1 (ICE mode), the data bus is always active so that the ICE can trace internal read and write operations. During external memory cycles the data bus is in the Hi-Z state during PHI2 low time.

5.13 Positive Edge Interrupt inputs (PExx)

Port pins P44, P45, P50, P51, P54, P55, and P56 have the Positive Edge sensitive interrupt inputs (PE44, PE45, PE50, PE51, PE54, PE55, and PE56) multiplexed with the I/O. When the pin is enabled as an edge interrupt (as defined by the Bus Control Register (BCR)), an interrupt is generated, and the associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a positive transition from "0" to "1". The transition from "1" to "0" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is "1", interrupts are disabled.

5.14 Negative Edge Interrupt inputs (NExx)

Port pins P46, P47, P52, P53, and P57 have the Negative Edge sensitive interrupt inputs (NE46, NE47, NE52, NE53, and NE57) multiplexed with the I/O. When the pin is enabled as an edge interrupt (as defined by the Bus Control Register (BCR)), an interrupt is generated, and the associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a negative transition from "1" to "0". The transition from "0" to "1" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When I equals a "1", interrupts are disabled.

5.15 Chip Select outputs (active low) (CSxB)

The CSxB Chip Select outputs are enabled (individually) as outputs on Port 3 with the PCS3x (Port 3 Chip Select register). Chip select 7, CS7B, is also automatically enabled by BCR7=1. Each of the eight chip selects is dedicated to one block of external memory; the mapping of each chip select to external addresses is given in Table 1-3 System Memory Map. Chip selects CS3B, CS4B, CS5B, CS6B, and CS7B are considered "clocked" chip selects. This means that they only become active during PHI2 high time. Chip selects CS0B, CS1B, and CS2B are "not clocked," and are active anytime the address bus is in the appropriate memory block.

5.16 Level Sensitive Interrupt Request inputs (IRQxB)

Port pins P41 and P42 I/O functions are multiplexed with IRQ1B and IRQ2B Level Sensitive Interrupt inputs that are selected by Bus Control Register bit 6 (BCR6). When IRQxB is held low the associated Interrupt Flag is set to a "1" in the Interrupt Flag Register Two (IFR2). When the associated Interrupt Enable Register Two (IER2) bit is set to a "1" the MPU will be interrupted provided the I flag of the MPU is cleared to a "0" allowing interrupts. Unlike the edge interrupts, which do not hold the interrupt bit set, an interrupt will be generated as long as IRQxB is low.

5.17 Non-Maskable Edge Interrupt Input (NMIB)

Port pin P40 I/O function is multiplexed with NMIB edge triggered interrupt and is controlled by Bus Control Register bit 6 (BCR6). When NMIB is selected by setting BCR6 equal to "1", the MPU will be interrupted on all negative edges of NMIB. Since the I flag cannot prevent NMI- from interrupting, NMIB is thought of as non-maskable, once enabled in the Bus Control Register.

5.18 Asynchronous Receive Input/Transmitter Output (RXD, TXD)

The W65C134S has a full duplex Universal Asynchronous Receiver and Transmitter (UART) that may be enabled by the Asynchronous Control and Status Register (ACSR). When the Receiver is enabled by ACSR5=1 then port pin P60 becomes the Asynchronous Receiver Input (RXD). When the Transmitter is enabled by ACSR0=1, then port pin P61 becomes the Asynchronous Transmitter Output (TXD).

5.19 Timer A Input and Output (TIN, TOUT)

Timer A is controlled by TCR1x (see TCR1x for more information). When the UART is not in use, Timer A can be used for counting input negative pulses on TIN. Timer A can also be used to put out a square wave or rectangular wave form on TOUT. When counting negative pulses on TIN, the TIN frequency should always be less than one-half the frequency of PHI2. TOUT changes state on every time-out of Timer A; therefore, varying waveform and frequency depends on the timer latch values and may be modified under software control.

5.20 The Serial Interface Bus (SIB) pins. (See Serial Interface Bus (SIB) Message Transmission Timing diagram.)

CHIN Serial Interface Bus (SIB) CHain INput for token passing. CHIN (CHain INput) is connected to CHOUT (CHain OUTput) of the previous device on the chain. When high it indicates that this device can be master because all devices between the previous master and this device are not master.

CHOUT SIB CHain OUTput for token passing. CHOUT goes to CHIN of the next device on the chain.

SCLK Serial Clock for the SIB. SCLK is connected to all devices. It is connected to the output of the serial clock generator in the device in which the clock generator is enabled. It synchronously advances the state machines for sending and receiving in all devices and also shifts data serially from the sending device to a receiving device.

SDAT Serial Data for the SIB. SDAT is connected to all devices. When it is not being driven during a data transfer, it should be connected to an external current source to suppress noise transients. When a message is not being sent, a device that wants to send a message pulls it low to start the serial clock generator. When a message is being sent, the device that is sending uses it to convey data to all other devices. At the end of the message the receiving device uses it to acknowledge reception to the master.

6 TIMING, AC AND DC CHARACTERISTICS

6.1 Absolute Maximum Ratings (Note 1)

Table 6-1 Absolute Maximum Ratings

Rating	Symbol	Value
Supply Voltage	VDD	-0.3 to +7.0V
Input Voltage	VIN	-0.3 to VDD +0.3V
Storage Temperature	TS	-55 °C to +150 °C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

6.2 DC Characteristics

VDD = 2.8V to 5.5V (except where noted), VSS = 0V, TA = -40°C to +85°C (except where noted)

Table 6.2-1 DC Characteristics

	Symbol	Min	Max	Unit
Input High Threshold Voltage CLK, FCLK, RESB, all other inputs	Vih	.9XVDD 0.7XVDD	VDD+0.3 VDD+0.3	V V
Input Low Threshold Voltage CLK, FCLK, RESB, all other inputs	Vil	VSS-0.3 VSS-0.3	.1XVDD .3XVDD	V V
Input Leakage Current (Vin=VSS to VDD, VDD=5.5V) all inputs	Iin	-1	+1	uA
Output High Voltage Ioh=-100uA, VDD=2.8V all outputs	Voh	0.9XVDD	-	V
Output Low Voltage Iol=100uA, VDD=2.8 all outputs	Vol	-	.1XVDD	V
Supply Current (No Load 2.8V and all on-chip 5.5V circuits operating)	Icc	- -	2 4	mA/MHz mA/MHz
Supply Current (No Load) TA= 25°C Reset Condition RESB, BE=VSS; CLK=32768Hz, VDD=5.5V FCLK=HI, PHI2=HI STP Condition CLK=HI, VDD=2.8V FCLK=HI, PHI2=HI Wait for Interrupt Condition CLK=32768Hz FCLK=HI, VDD=2.8V	Ires Istp Iwai	- - -	5 1 5	uA uA uA
Capacitance (sample Tested) (Vin=0, Ta=25°C, f=1MHz) all pins except VSS, VDD	Cin	-	10	pF

6.3 AC Characteristics

Table 6.3-1 AC Characteristics

Timing Parameter	Definition
tISA	Address input setup from PHI2
tIHA	Address input hold from PHI2
tODA	Address output delay from PHI2
tOHA	Address output hold from PHI2
tISD	Data input setup from PHI2
tIHD	Data input hold from PHI2
tODD	Data output delay from PHI2
tOHD	Data output hold from PHI2
tISB	BE input setup from PHI2
tIHB	BE input hold from PHI2
tODSY	SYNC output delay from PHI2
tISRR	RDY/RESB input setup from PHI2
tIHRR	RDY/RESB input hold from PHI2
tODRN	RUN output delay from PHI2
tOHRN	RUN output hold from PHI2
tISP	Port input setup from PHI2
tIHP	Port input hold from PHI2
tODP	Port output delay from PHI2
tOHP	Port output hold from PHI2
tISI	Interrupt input setup from PHI2
tIHI	Interrupt input hold from PHI2
tISS	Serial Data input setup from SCLK
tIHS	Serial Data input hold from SCLK
tODS	Serial Data output delay from SCLK
tOHS	Serial Data output hold from SCLK
tISC	Chain input setup from SCLK
tIHC	Chain input hold from SCLK
tODC	Chain output delay from SLCK
tOHC	Chain output hold from SCLK
tISU	UART Data input setup from PHI2
tIHU	UART Data input hold from PHI2
tODU	UART Data output delay from PHI2
tOHU	UART Data output hold from PHI2
tODD (DMA)	Data output delay from PHI2 (ROM read)
tODPH	PHI2 output delay from CLK/FCLK
tODSC	SCLK output delay from PHI2
tODCSR	CS output delay from PHI2 rising
tODCSF	CS output delay from PHI2 falling
tR	FCLK/CLK risetime
tF	FCLK/CLK falltime
tBR	BE to RESB
tBV	BE to D0-7, A0-15, WEB Valid
CEXT	External Capactive load
tCYC	CLK cycle time
tPWL	CLK low time
tPWH	CLK high time
tCYC2	PHI2 cycle time
tPWL2	PHI2 low time
tPWH2	PHI2 high time
tCYCF	FCLK cycle time
tPWLF	FCLK low time
tPWHF	FCLK high time

6.4 AC Parameters Table 6.4-1 AC Parameters

Timing Parameter	VDD=1.8V 100 KHz #2,3		VDD=2.8V 1 MHz #2,3		VDD=5V+/-10% 2 MHz #2,3		VDD=5V+/-10% 4 MHz #2,3		Units
	Min	Max	Min	Max	Min.	Max	Min	Max	
tISA	3960	-	460	-	210	-	85	-	nS
tIHA	20	-	20	-	20	-	20	-	nS
tODA	-	2800	-	280	-	180	-	90	nS
tOHA	20	-	20	-	20	-	20	-	nS
tISD	2700	-	270	-	100	-	60	-	nS
tIHD	20	-	20	-	20	-	20	-	nS
tODD	-	3300	-	330	-	150	-	75	nS
tOHD	10	-	10	-	10	-	10	-	nS
tISB	3900	-	390	-	180	-	75	-	ns
tIHB	20	-	20	-	20	-	20	-	nS
tODSY	-	2700	-	270	-	150	-	75	nS
tISRR	700	-	70	-	40	-	65	-	nS
tIHRR	20	-	20	-	20	-	20	-	nS
tODRN	-	3300	-	330	-	150	-	75	nS
tOHRN	20	-	20	-	20	-	20	-	nS
tISP	2700	-	270	-	100	-	60	-	nS
tIHP	20	-	20	-	20	-	20	-	nS
tODP	-	2800	-	280	-	180	-	90	nS
tOHP	20	-	20	-	20	-	20	-	nS
tISI	800	-	80	-	40	-	25	-	nS
tIHI	20	-	20	-	20	-	20	-	nS
tISS	800	-	80	-	40	-	25	-	nS
tIHS	20	-	20	-	20	-	20	-	nS
tODS	-	2900	-	290	-	170	-	90	nS
tOHS	20	-	20	-	20	-	20	-	nS
tISC	800	-	200	-	100	-	60	-	nS
tIHC	20	-	20	-	20	-	20	-	nS
tODC	-	7500	-	750	-	375	-	190	nS
tOHC	-	20	-	20	-	20	-	20	nS
tISU	800	-	80	-	40	-	25	-	nS
tIHU	20	-	20	-	20	-	20	-	nS
tODU	-	3000	-	300	-	150	-	75	nS
tOHU	10	-	10	-	10	-	10	-	nS
tODD (DMA)	-	3800	-	380	-	200	-	100	nS
tODPH	-	2000	-	200	-	100	-	50	nS
tODSC	-	2000	-	200	-	100	-	50	nS
tODCSR	0	1000	0	100	0	50	0	25	nS
tODCSF	0	1000	0	100	0	50	0	25	nS
tOCHCN	-	4500	-	450	-	225	-	125	nS
tR	-	100	-	50	-	25	-	15	nS
tF	-	100	-	50	-	25	-	15	nS
tBR	2000	-	200	-	100	-	35	-	nS
tBV	-	1900	-	190	-	90	-	50	nS
CEXT	50	-	50	-	50	-	50	-	pf
tCYC #1	16000	inf.	4000	inf.	2000	inf.	1000	inf.	nS
tPWL	8000	inf.	2000	inf.	1000	inf.	500	inf.	nS
tPWH	8000	inf.	2000	inf.	1000	inf.	500	inf.	nS
tCYC2	TCYCF	inf.	TCYCF	inf.	TCYCF	inf.	TCYCF	inf.	nS
tPWL2	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tPWH2	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tCYCF	4000	inf.	1000	inf.	500	inf.	250	inf.	nS
tPWLF	2000	inf.	500	inf.	250	inf.	125	inf.	nS
tPWHF	2000	inf.	500	inf.	250	inf.	125	inf.	nS

6.5.1 AC Timing Diagram Notes

1. tCYC must always be equal to or greater than four times tCYCF when FCLK is running.

2. Rise and Fall Times for all signals are measured on a sample basis from .3xVDD to .7xVDD. The Rise and Fall times are not programmable on the automated test system that is used for production testing. A typical Rise and Fall time is 5-10ns; therefore, the spec indicates the duty cycle of the clock as tested (tPWL=tCYC/2-tF). The Rise and Fall times indicate output Rise and Fall times. The most critical Rise and Fall times are for PHI2 because all timing is related to PHI2. The input Rise and Fall times can affect the input setup time (tIS), output delay time (tOD) and hold time (tH). This must be taken into account in an application. At 2MHz and 4MHz the worst case input Rise and Fall times may prevent a system from working.

3. Hold Time for all inputs and outputs is relative to the associated clock edge.

6.6 AC Timing Diagrams

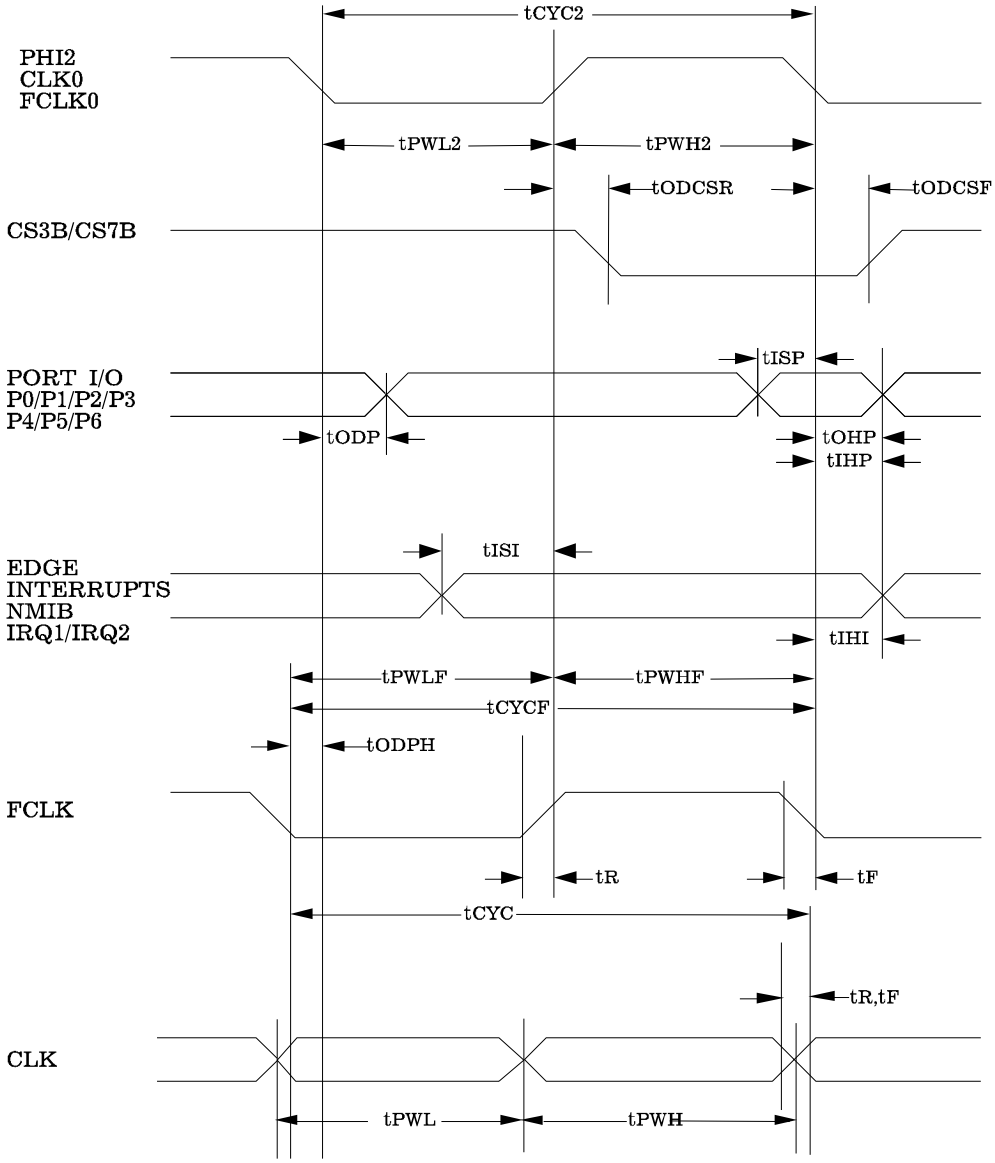


Figure 6.6-1 AC Timing Diagram #1

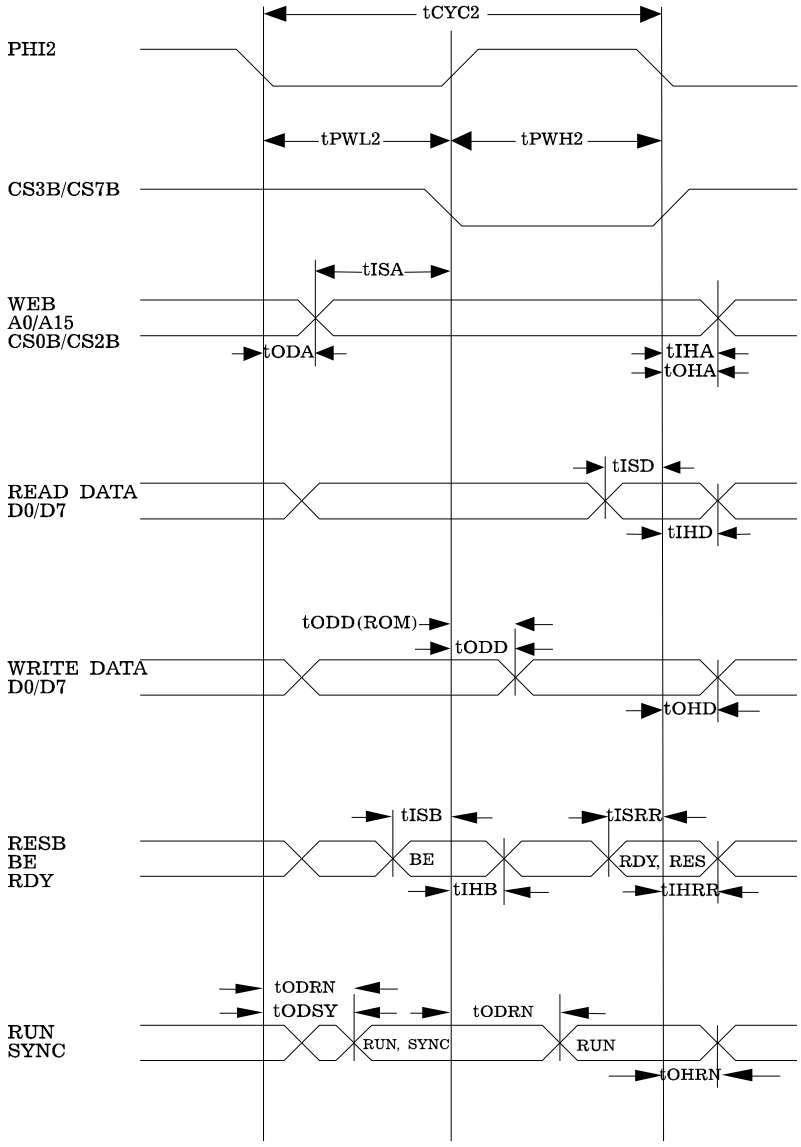


Figure 6.6-2 AC Timing Diagram #2

Notes:

1. Voltage levels shown are VL = VSS and VH = VDD.
2. Measurement points shown are .5xVDD and .5xVDD.
3. CLK can be asynchronous, tCYC equal or greater than 4xtCYCF.
4. The PHI2 and CSxB timing is controlled by TCR11. When TCR11=0 PHI12 and CSxB are related to CLK. When TCR11=1, PHI2 and CSxB are related to FCLK.

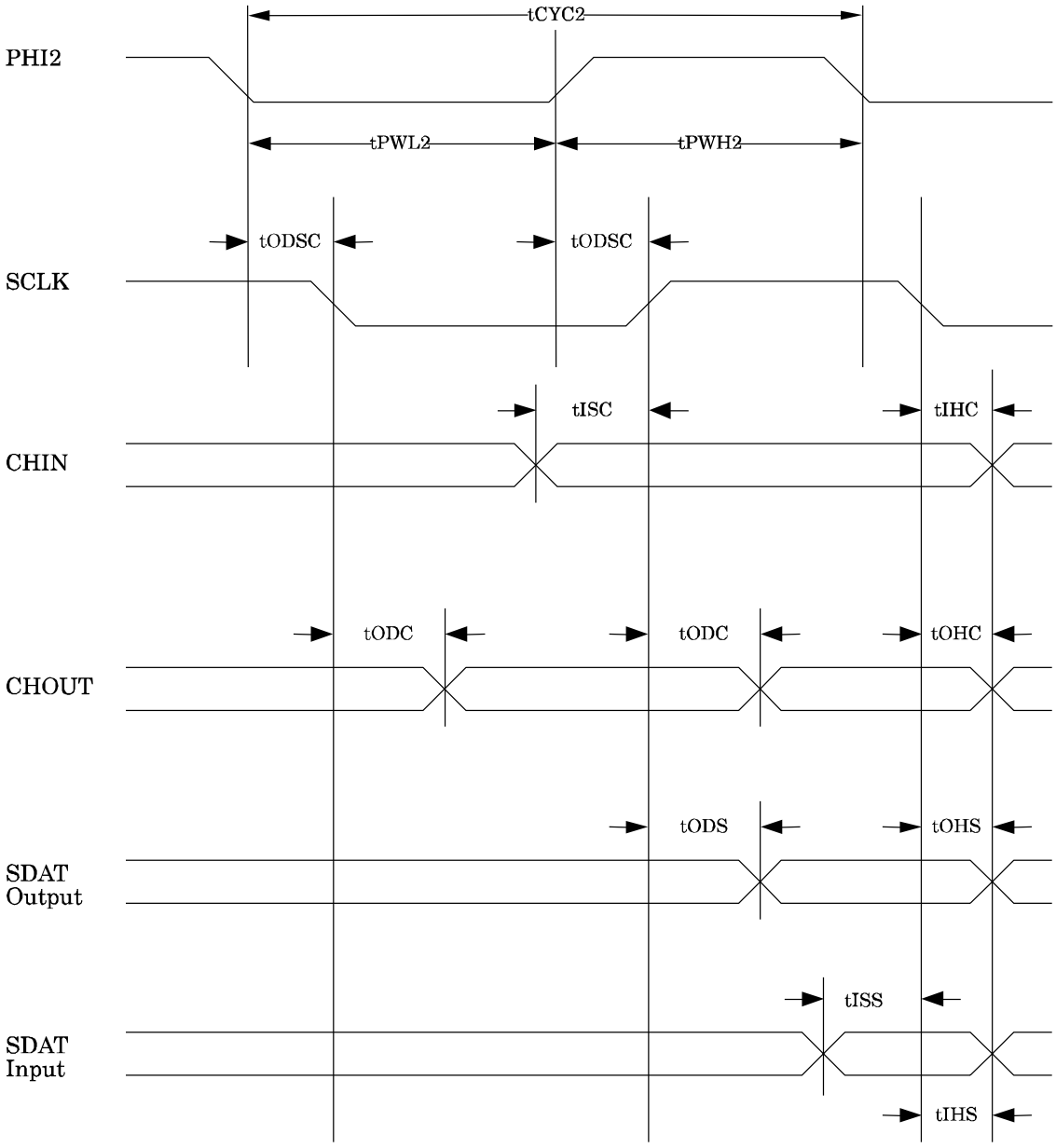


Figure 6.6-3 AC Timing Diagram #3

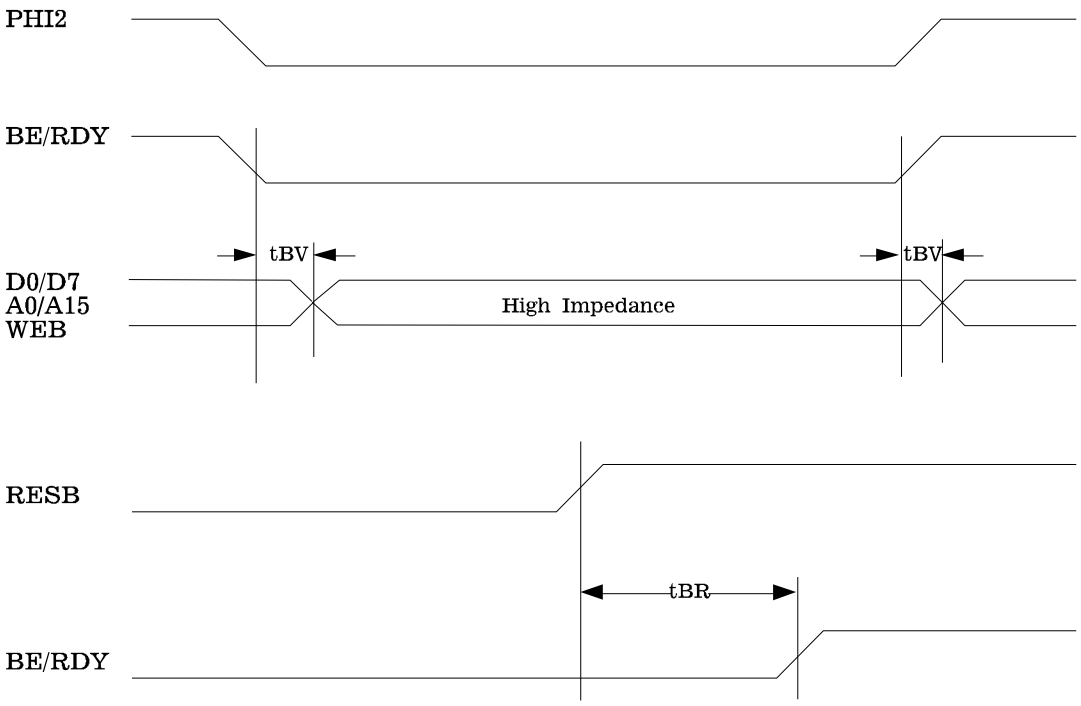


Figure 6.6-4 AC Timing Diagram #4

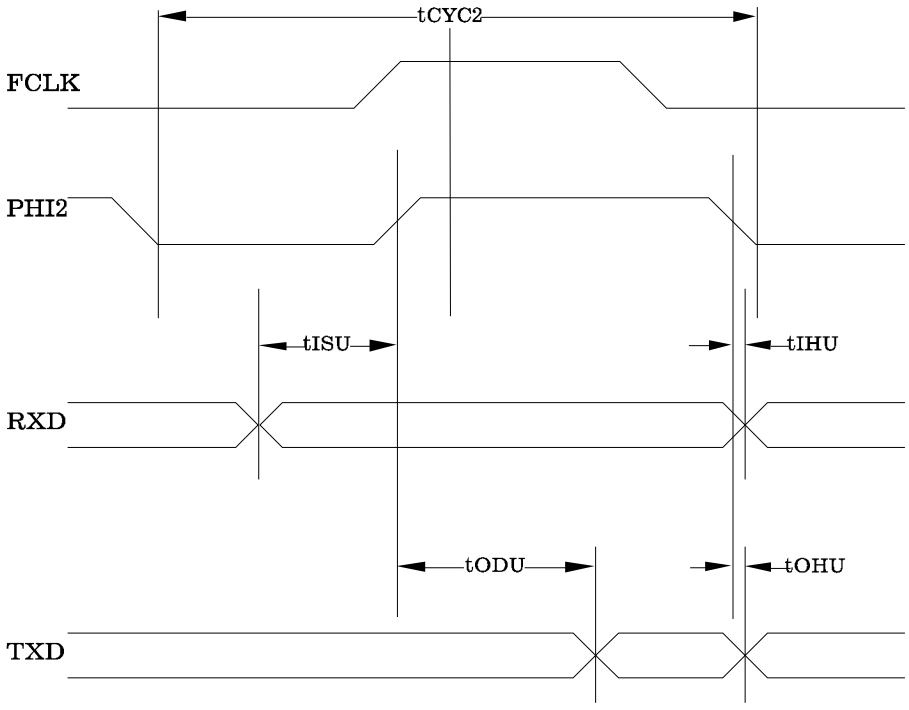
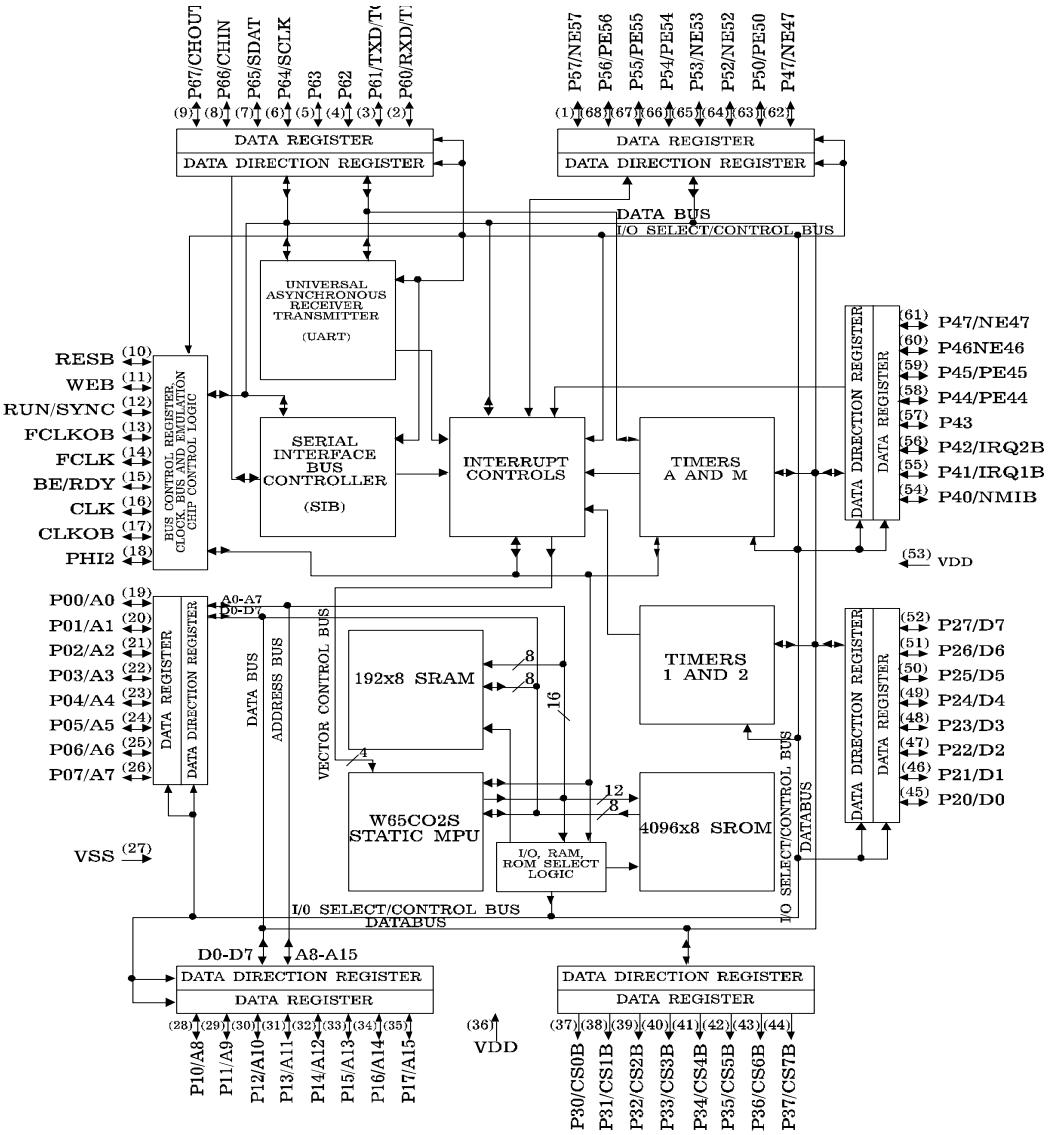


Figure 6.6-5 AC Timing Diagram #5

7 Block Diagrams

Figure 7-1 W65C134S Block Diagrams



Note: Pin numbers apply to PLCC package only.

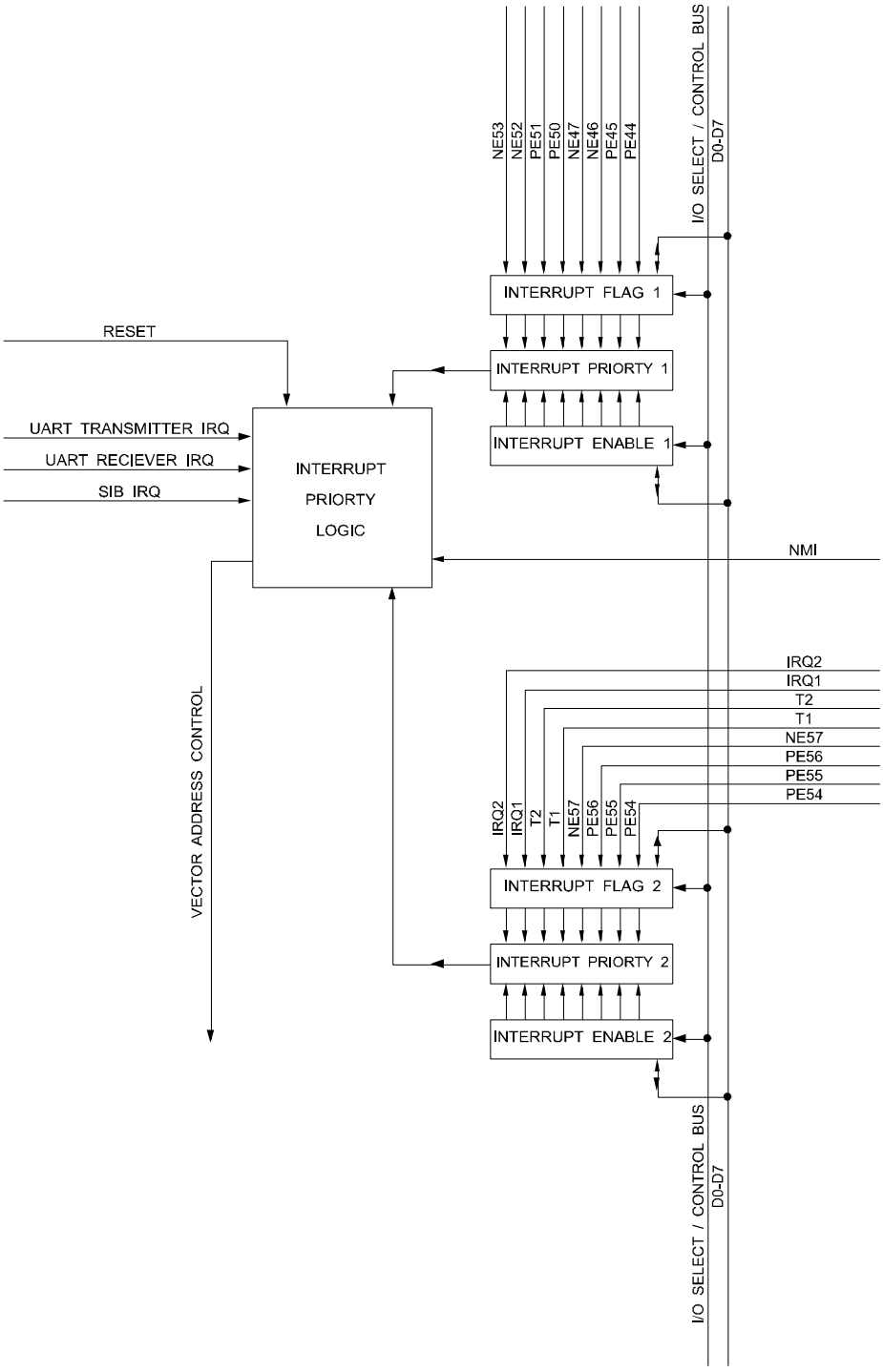


Figure 7-2 Interrupt Controller Block Diagram

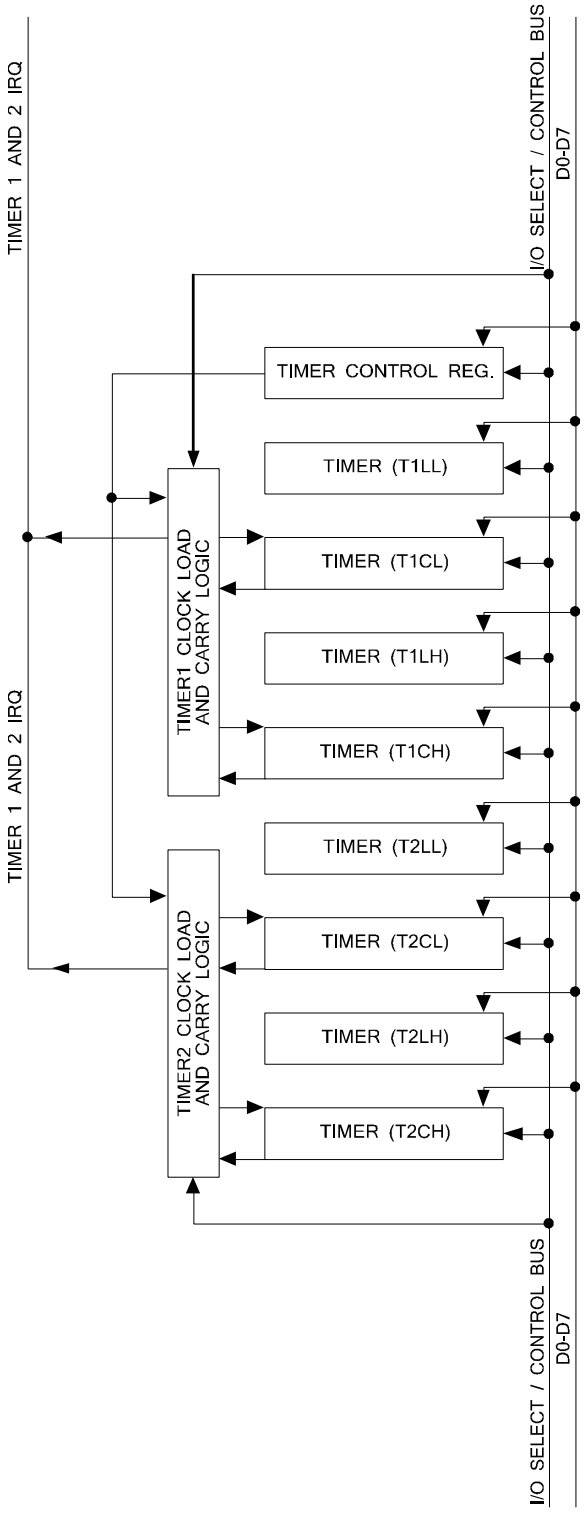


Figure 7-3 T1 and T2 Block Diagram

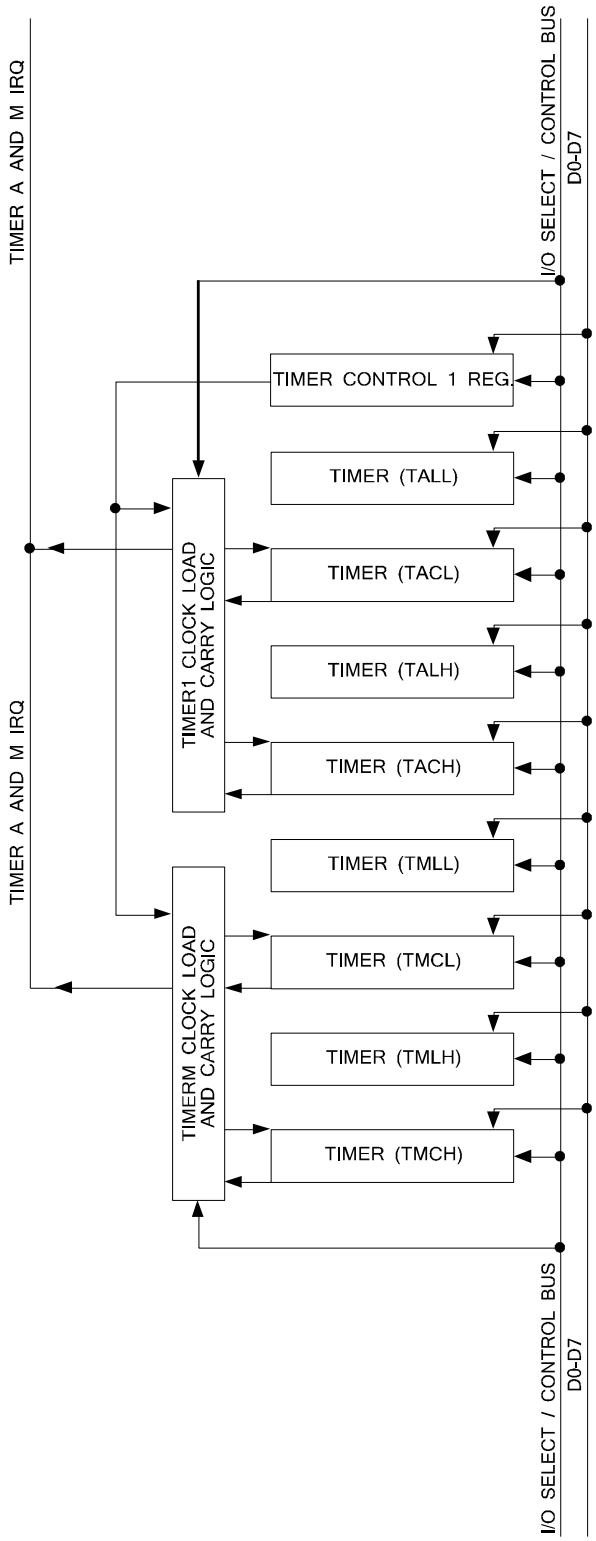


Figure 7-4 Timer A and M (TA and TM) Block Diagram

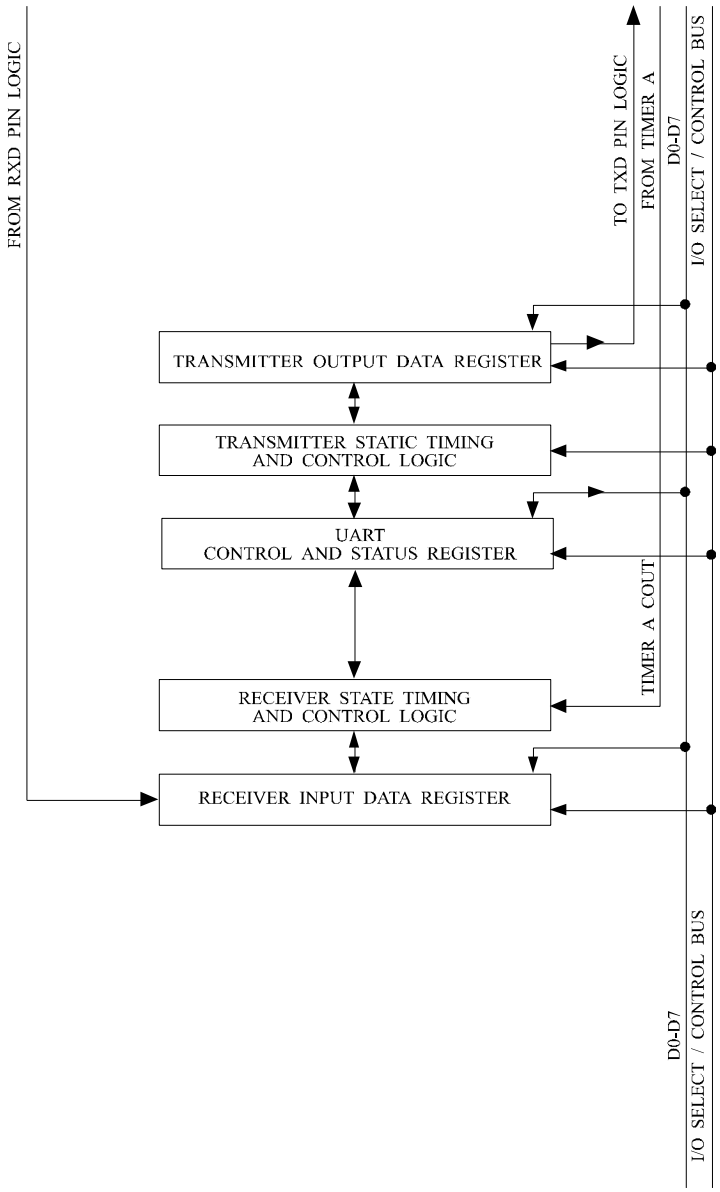


Figure 7-5 Universal Asynchronous Receiver Transmitter (UART) Block Diagram

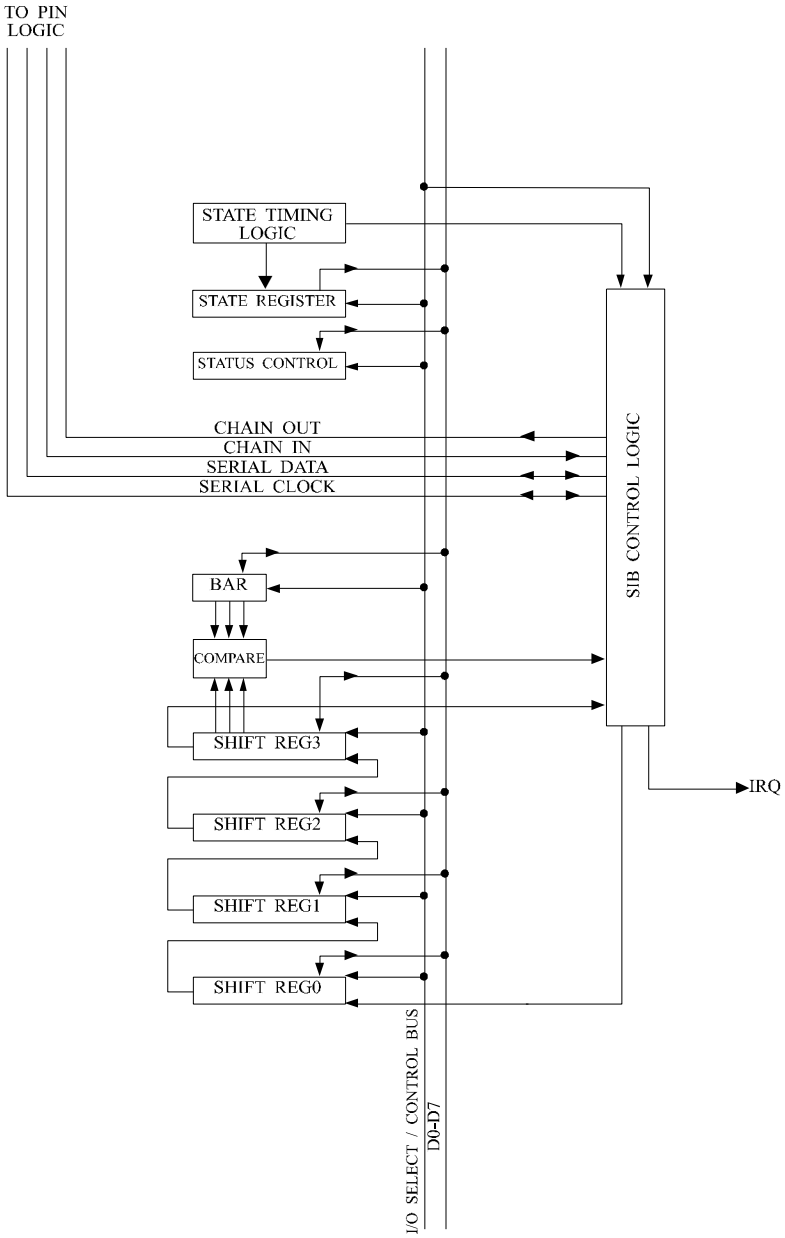


Figure 7-6 Serial Interface Bus (SIB) Block Diagram

8 Application Information

8.1 External ROM Startup with W65C134S Mask ROMs

Future versions of the W65C134S mask ROM may vary, but each version should contain standard machine code that allows startup to an external memory. Standard versions of the W65C134S will always contain such a startup option. Anyone writing a custom mask ROM for the 134 is encouraged to follow this standard.

The startup standard allows a program in an external memory to be executed after RESET if the startup code WDC (in ASCII, $57, $44, $43) is present at addresses $8000-$8002 or $0200-$0202. If the startup code is found at either set of addresses, the mask ROM does a JMP instruction to $8004 or $0204 respectively. W65C134S chip selects CS6 and CS7 can be used to address the memories.

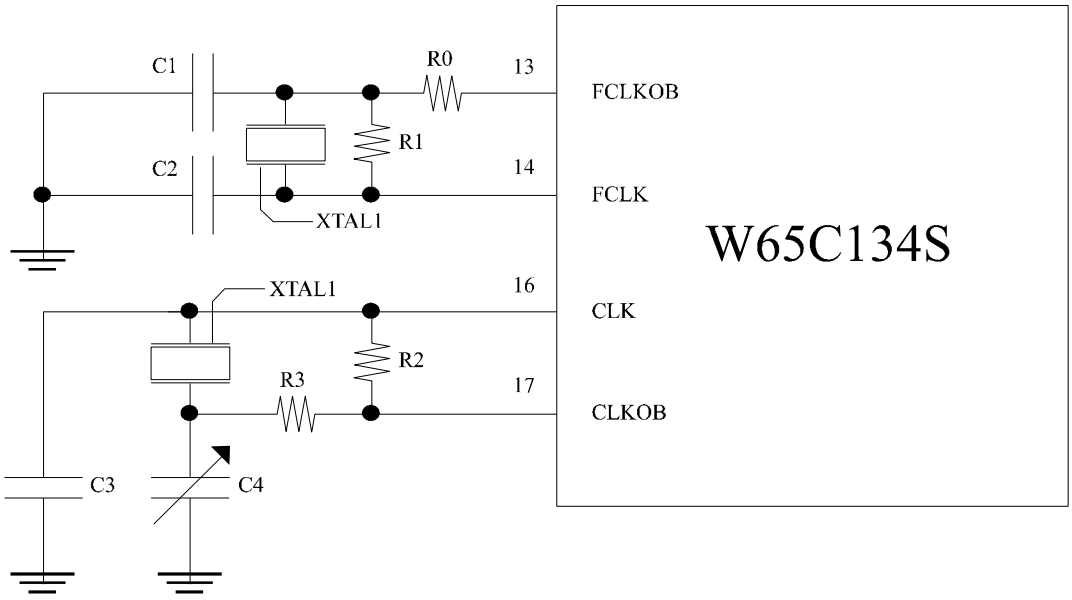
The startup standard was set (and will be followed) with the original WDC-101 mask ROM in the early W65C134S prototypes. A sample startup program (modified from WDC-101) appears below. The W65C02S RESET vector ($FFFC) should be set to STARTUP.

```
STARTUP     LDA     #$01    ;ENABLE EXTERNAL MEMORY BUS
            TSB     BCR     ;(BCR=$001B)
            LDA     #$C0    ;ENABLE CHIP SELECTS CS6-, CS7-
            STA     PCS3    ;ON P36, P37 (PCS3=$0007)
;
TRY80       LDA     $8000   ;CHECK $8000 FOR 'WDC'
            CMP     #'W'
            BNE     TRY02
            LDA     $8001
            CMP     #'D'
            BNE     TRY02
            LDA     $8002
            CMP     #'C'
            BNE     TRY02
            JMP     $8004   ;EXECUTE EXTERNAL ROM PROGRAM
;
TRY02       LDA     $0200   ;CHECK $0200 FOR 'WDC'
            CMP     #'W'
            BNE     NOEXT
            LDA     $0201
            CMP     #'D'
            BNE     NOEXT
            LDA     $0202
            CMP     #'C'
            BNE     NOEXT
            JMP     $0204   ;EXECUTE EXTERNAL ROM PROGRAM
;
NOEXT       JMP     MASK_ROM_PROGRAM    ;EXECUTE PROGRAM IN MASK ROM
```

8.2 Recommended clock (CLK) and fclock (FCLK) oscillators

The following circuit is a possible clocking system for the W65C134S providing both 32,768 KHz and 2.0 MHz frequencies. The 32,768 KHz clock is well suited for setting up a time of day clock with one of the W65C134S's internal timers.

Figure 8.2-1 Oscillator Circuit



In constructing this oscillator circuit, components should be kept as physically close to the W65C134S as possible and any excess in component leads should be trimmed off.

C1 = 47pF	R0 = 100Ω
C2 = 27pF	R1 = 800KΩ
C3 = 22pF	R2 = 2.6MΩ
C4 = 5-30pF variable	R3 = 150KΩ
XTAL1 = 4 MHz	XTA L2= 32.768 KHz

Note:

1. Depending on trace layout or construction techniques used, values may need to be altered slightly.
2. Pin numbers only apply to PLCC package only.

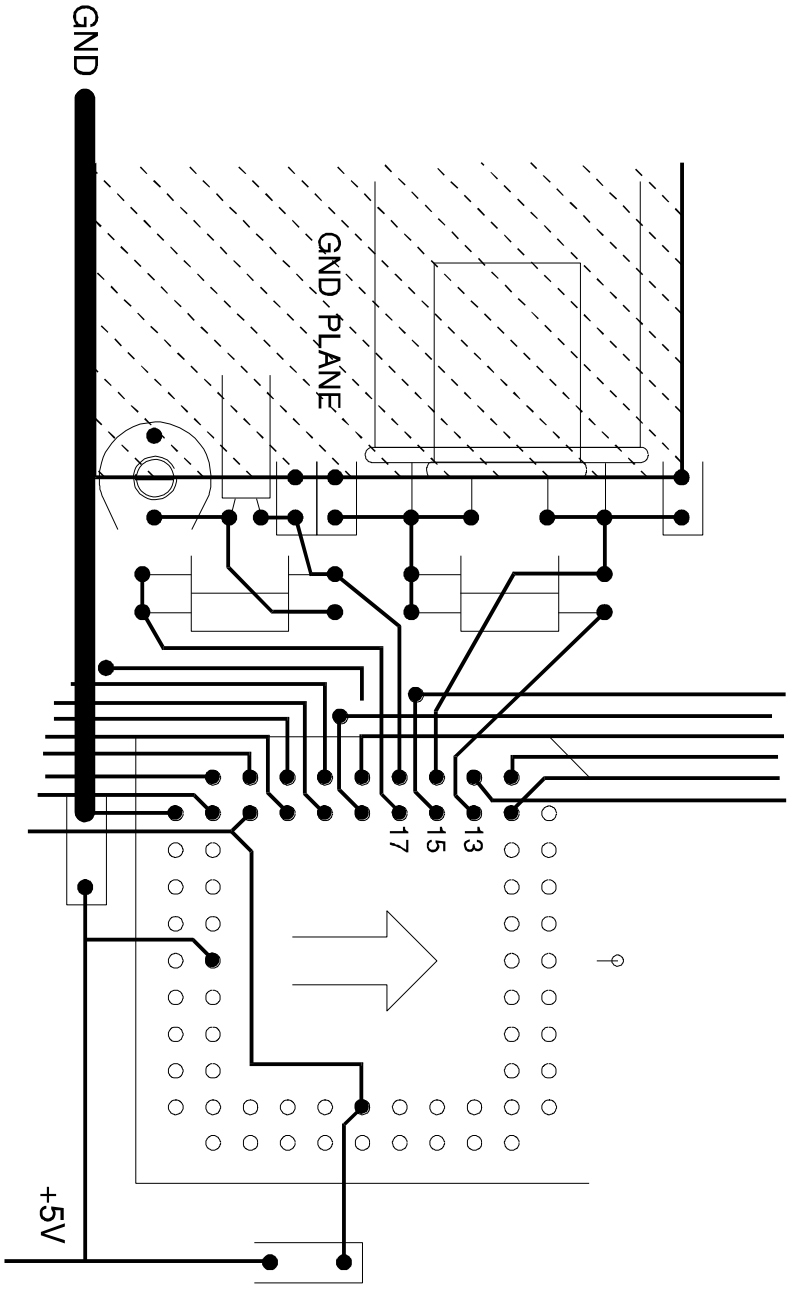


Figure 8.2-2 Circuit Board Layout for Oscillator Circuit

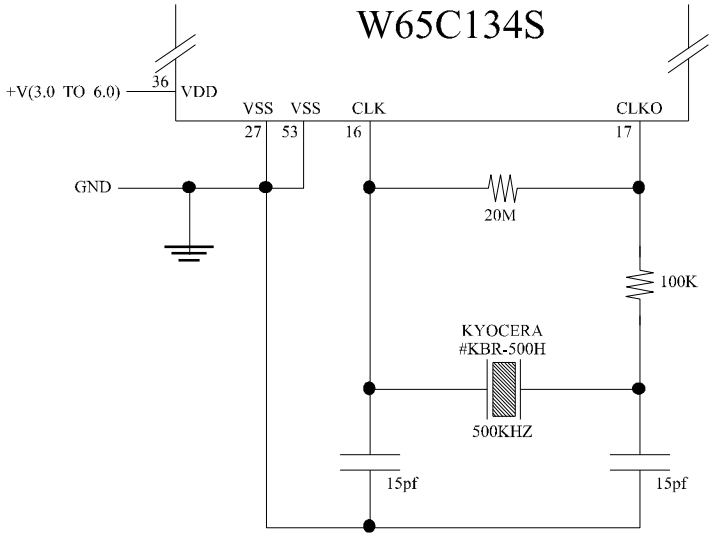


Figure 8.2-3 W65C134S Resonator Circuit

8.3 Wait state information and uses for the BE pin

The BE pin has two functions; allowing DMA into the W65C134S (BE function) and stopping the microprocessor (RDY function). Changing BE during PHI2 low time changes the BE function; changing BE during PHI2 high time changes RDY. If you want to stop the processor, you should pull BE low in the PHI2 high time for as many cycles as needed. Pulling the BE low in PHI2 high time does not tristate the memory bus. Note also that the PHI2 pin does not stay high while RDY is pulled low; PHI2 going out will continue normally regardless of BE.

Pulling BE low during PHI2 low time turns off the output buffers on the address pins; however, the pins do not float because of weak bus holding devices. Note that the addresses are really inputs to the W65C134S when BE is low. If an external driver puts an address on the bus while BE is low, internal memory (RAM, ROM, or memory-mapped registers) will be accessed depending on the state of WEB. If you have no desire to turn off the busses when you slow down for the peripheral chips, you should hold BE high while you hold RDY low. That is,

BE = (PHI2BAR or RDY)

Where PHI2BAR is PHI2 inverted and delayed at least 10ns. RDY is your signal to request the microprocessor to stop. If you are not using the FCLK oscillator, another (less desirable) way to stop the microprocessor is to extend the low or high time of FCLK as long as you need to. This will work only if you know the microprocessor is using FCLK, not CLK.