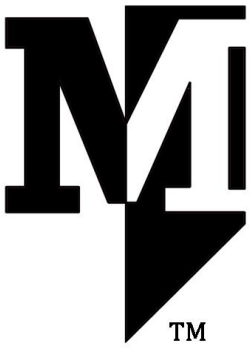
MENSCH™



Microcomputer

DOCUMENT REVISION HISTORY

Version	Date	Author	Description
1.0	17-Mar-03	David Gray and Bill Mensch	Initial Document Entry
1.1	17-Mar-05/06	David Gray and Bill Mensch	Page 1 Microcomputer Datasheet changed to Microcomputer, Schematic page location changed, Internal Memory Map added, Header updated, Expansion Connectors table centered and Revision History resized.
1.2	17-Mar-13	Bill Mensch	Updated Internal Memory Map on page 9.
1.3	17-April-08	Bill Mensch and David Gray	Added Internal RAM Memory Map
1.4	17-July-31	Bill Mensch and David Gray	Updated Internal RAM Memory Map
1.5	19-Oct-16	David Gray	Correct J5 Pinout

Contents

Introduction

The MENSCH™ microcomputer (Part No. W65C265QBX) is a small single board computer (SBC), 1.25" x 2.25", using the System on a Chip (SoC) W65C265S MCU. The W65C265S was invented and designed by Bill Mensch WDC's founder after he invented and designed the 65816 microprocessor.

As a recognized pioneer of the microprocessor industry. Mr. Mensch's twenty two patented inventions were/are used on the original Motorola 6800 Microprocessor Family, MOS Technology 6502 Microprocessor Family, and WDC's 65C02 and 65816 Microprocessor Families. As an electrical engineer, 1971 BSEE from The University of Arizona (UA), having taught graduate level classes at Arizona State University (ASU) on SOC design for five years, advisor to four university colleges of engineering for over two decades, the MENSCH™ was designed in hopes that it will attract learners to consider a career based on an Electrical and Computer Engineering (ECE) education, hardware and software engineering.
The MENSCH™ can be used to learn about all kinds of electronic components and all kinds of state-of-the-art programmable logic. Operating at 3.3 volts provides for easy connectivity with various state-of-the-art electronic components and modules such as sensors and actuators. Operating at 5.0 volts provides easy connectivity to 5.0 volts electronic components and modules.

Learning to code in Machine language, Assembly Language, and C language as well as learning to describe hardware with software using Verilog HDL for use in different types of FPGA boards from Altera/Intel, Lattice, Microsemi, and Xilinx already at colleges of engineering provides an excellent basis for a future as an engineer. Describing hardware with software supports further retargeting to low cost and high performance ASICs for high volume commercial use.

Exploring the fundamentals of Electrical and Computer Engineering (ECE) with the MENSCH™ provides a strong foundation for understanding of all kinds of electronics and computer technologies such as the x86 microprocessors from Intel, used on PCs and Macs, and ARM microprocessors, used in all kinds of Android Tablets and iOS and Android Smartphones.

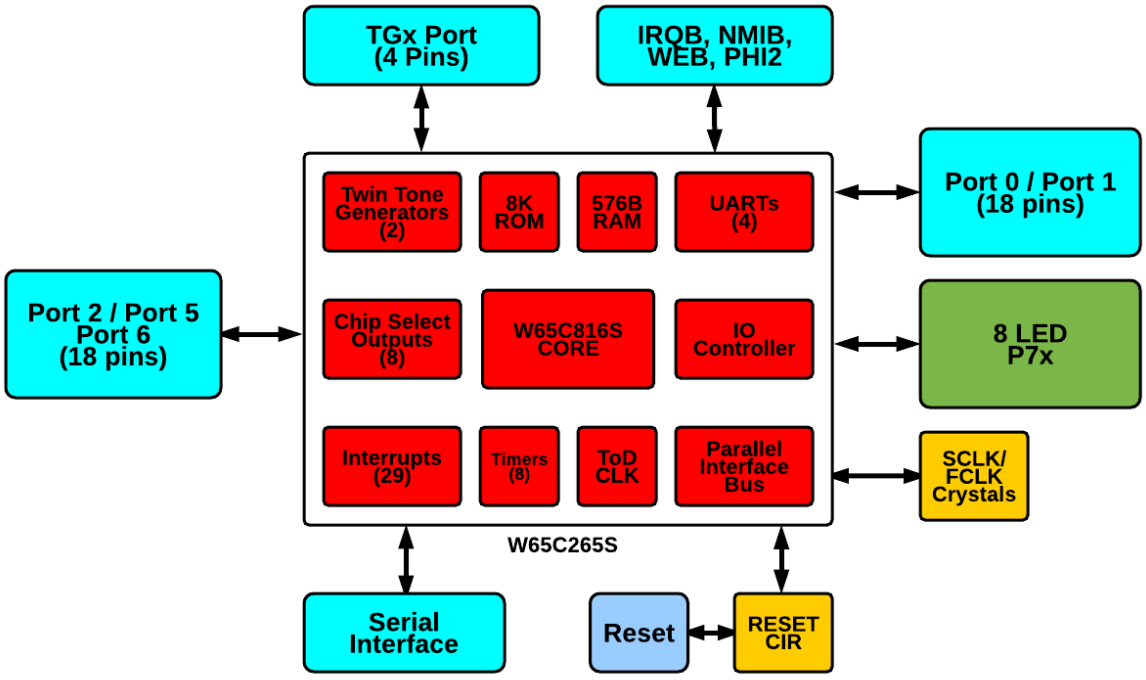
The MENSCH™ has a simple connector arrangement that can be used as stand alone, plugged into a bread board or plugged into your own custom "daughterboard" for your favorite Maker project. The MENSCH™ has a built in operating system called a "Monitor". The Mensch Monitor™ interfaces through a USB cable providing power and development through all kinds of "Terminal Emulators" found in most computers, PCs, Macs, tablets, and Smartphones.

Features

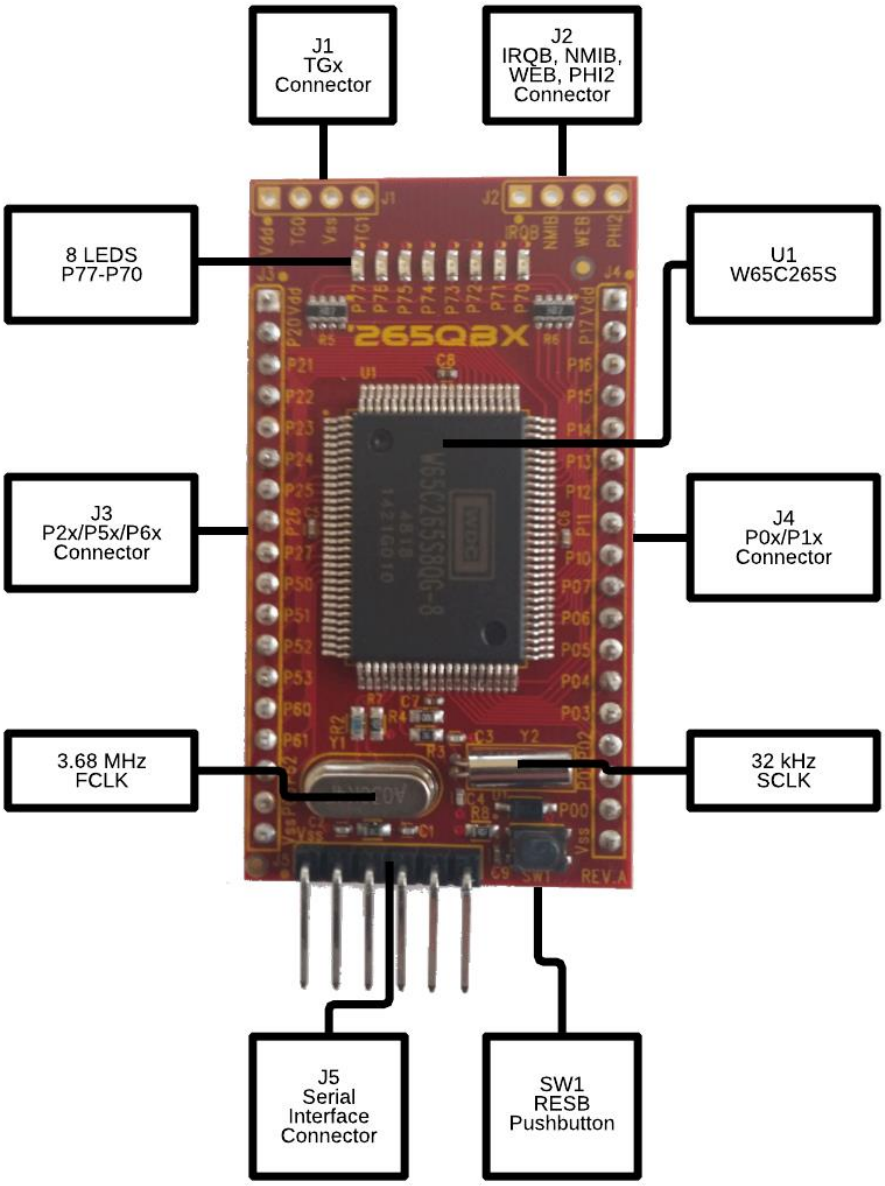
1.1 Feature List

- W65C265S MCU operating at 3.6864 MHz
- Works at 3.3V or 5V (Cable not provided), giving access to a wider range of sensors, memories, FPGAs, etc.
- 2 – 18 pin connectors plug into standard breadboards for quick prototyping. Signals accessed are Ports P0x (A0-A7), P1x(A8-A15), P3x (D0-D7), Serial Ports S0 and S1
- 8 LEDs connected to P7x
- 1 x 4 pin Connector with PHI2, WEB, NMIB and IRQB signals for expansion.
- 1 x 4 pin Twin Tone Generator Connector (Driven by TG0/1)
- Serial Terminal Programming Interface Serial Port #3 (P66/P67/P56/P57) NOTE: Requires external FTDI FT232 or similar cable/board (not included)

1.2 Functional Block Diagram

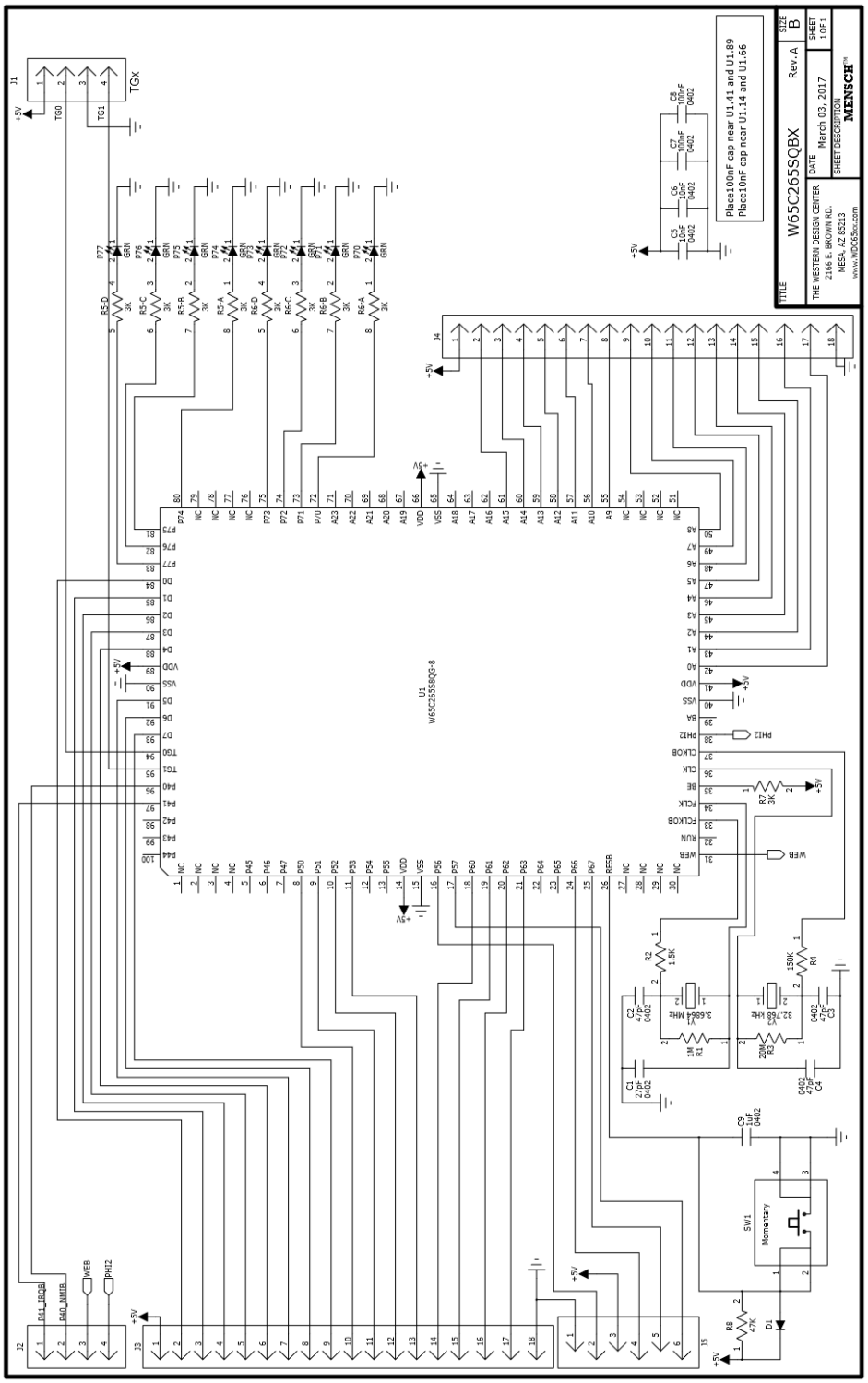


1.3 Board Diagram



1.25" x 2.25" PCB

1.4 Schematic



1.5 W65C265S 16MB System Memory Map

W65C265S 16MB System Memory Map				
Start	***End***	***Size***	***Chip Select***	***Description***
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY *See Note 2*
(00)E000 (00)8000	(00)FFFF (00)DEFF	8192 B 24320 B	CS4B	ROM MEMORY (*Note 1*) ROM MEMORY (*Note 1*)
(00)0200	(00)7FFF	32256	CS3B	Cache Memory *See Note 3*
(00)FF00 (00)E000 (00)DF80 (00)DF70 (00)DF50 (00)DF40 (00)DF20 (00)DF00 (00)0000	(00)FFFF (00)FEFF (00)DFBF (00)DF7F (00)DF6F (00)DF4F (00)DF27 (00)DF07 (00)01FF	256 B 7936 B 64 B 16 B 32 B 16 B 8 B 8 B 512 B	CS2B	On Chip Interrupt Vectors On-Chip ROM On-Chip RAM On-Chip Comm. Registers On-Chip Timer Registers On-Chip Control Registers On-Chip IO Registers On-Chip IO Registers On-Chip RAM
(00)DFC0	0xDFFF	64 B	CS1B	External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B	CS0B	External Chip Select 0 (P70) *See Note 4*

Note 1 - When on-chip 8K bytes of ROM are enabled:
- a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
- b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
- a.) CS5B decode is reduced by the addresses used by same.
- b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

1.6 W65C265S Internal On-Chip Memory Map

See the W65C265S Datasheet for more details. Also, the demo code has a complete listing of labels for each of the register address locations for ease of coding in Assembly Language.

Start	*End*	*Size*	*Description*
(00)FF00	(00)FFFF	256B	Interrupt Vectors
(00)E000	(00)FEFF	7936B	MENSCH™ Monitor ROM
(00)DF80	(00)DFBF	64B	IO Page DF SRAM
(00)DF70	(00)DF7F	16B	Control Registers
(00)DF50	(00)DF6F	32B	UART Registers
(00)DF40	(00)DF4F	16B	Timer Registers
(00)DF27	(00)DF27	1B	Chip Select Register
(00)DF24	(00)DF26	3B	Data Direction Registers
(00)DF20	(00)DF23	4B	IO Registers
(00)DF04	(00)DF07	4B	Data Direction Registers
(00)DF00	(00)DF03	4B	IO Registers
(00)0100	(00)01FF	256B	65C02 Page One aka Stack Page SRAM
(00)0000	(00)00FF	256B	Page Zero SRAM

1.7 Internal User SRAM Memory Map

MENSCH™ Internal User SRAM																
Byte	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Page 0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
(00)0000	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0010	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N
(00)0020	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0030	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N
(00)0040	Y	Y	Y	N	N	N	N	N	N	N	N	N	N	N	N	N
(00)0050	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N	N	N	N
(00)0060	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
(00)0070	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
(00)0080	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0090	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00A0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00B0	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00C0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00D0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00E0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)00F0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Page 1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
(00)0100	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
(00)0110	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
(00)0120	C	C	C	C	N	N	N	N	N	N	N	N	N	N	N	N
(00)0130	C	C	C	C	C	C	C	C	N	Y	Y	Y	Y	Y	Y	Y
(00)0140	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0150	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N	N
(00)0160	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0170	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)0180	Y	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N
(00)0190	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N	N
(00)01A0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)01B0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)01C0	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)01D0	Y	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	N	N
(00)01E0	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N	N	N
(00)01F0	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
Page DF	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
(00)DF80	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)DF90	Y	Y	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)DFA0	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
(00)DF80	Y	Y	Y	Y	Y	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y

Legend
These areas are open RAM locations
These areas should not be used.
These areas are for USER use, but are reset when the reset button is pushed.

1.8 Expansion Connectors

J1 – TGx Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	TG0
3	VSS	4	TG1

J2 – Bus Control Connector			
Pin	Signal Name	Pin	Signal Name
1	P41-IRQB	2	P40-NMIB
3	WEB	4	PHI2

J3 –Left Expansion Connector		J4 –Right Expansion Connector	
Pin	Signal Name	Pin	Signal Name
1	VDD	1	VDD
2	P20-D0	2	P17-A15
3	P21-D1	3	P16-A14
4	P22-D2	4	P15-A13
5	P23-D3	5	P14-A12
6	P24-D4	6	P13-A11
7	P25-D5	7	P12-A10
8	P26-D6	8	P11-A9
9	P27-D7	9	P10-A8
10	P50-DTRB0	10	P07-A7
11	P51-DSRB0	11	P06-A6
12	P52-DTRB1	12	P05-A5
13	P53-DSRB1	13	P04-A4
14	P60-RXD0	14	P03-A3
15	P61-TXD0	15	P02-A2
16	P62-RXD1	16	P01-A1
17	P63-TXD1	17	P00-A0
18	VSS	18	VSS

J5 – UART Serial Connector			
Pin	Signal Name	Pin	Signal Name
1	VSS	2	P56-DTRB3
3	VDD	4	P66-RXD3
5	P67-TXD3	6	P57-DSRB3

1.9 8 LEDs

The MENSCH™ has 8 LEDs connected to the Port 7 chip select signals. The LED furthest to the left is connected to P77. The LED furthest to the right is connected to P70. Each LED is labeled for the appropriate signal on the board.

Connector Descriptions

Following are descriptions of main board connectors. For Port pins coming from the W65C265S chip, careful review of the W65C265S Datasheet is recommended.

2.1 TGx Connector (J1)

The Twin Tone Generator outputs (TGx) are synthesized 16 step cosine waveform outputs. Each Tone Generator is comprised of a 16 bit timer and a 16 step divider circuit that selects the proper Digital to Analog (DA) output level. The enable bits for the tone generators are located in bits 1 and 2 of the BCR registers. Refer to the W65C265S Datasheet (Section 1.11) for detailed operation information.

2.2 Control Connector (J2)

4 Control lines (P41-IRQB, P40-NMIB, WEB, PHI2) for external expansion.

2.3 Left IO Connector – P2x/P50-P53/P60-P63 (J3)

The J3 Left Connector has 16 IO lines that are connector to the P20-P27, P50-P53, and P60-P63 signals. This gives the user either 16 general purpose IO lines, the Data bus (P20-P27), or 2 serial UART ports (the signals are on both P5x and P6x). See Section 1.5 for connection information.

2.4 Right IO Connector – P0x/P1x (J4)

The J4 Right Connector has 16 IO lines that are connector to the P00-P07, and P10-P17 signals. This gives the user either 16 general purpose IO lines or the A0-A15 Address Bus of the W65C265S. See Section 1.5 for connection information.

2.5 Serial Port (J5)

The Serial Port connector is dual purpose. It is through this connector that you will generally power the board if you are hooking the board up to a PC, smartphone, etc. for serial communications.
In addition to the power, the J5 has the signals from UART3. The built-in monitor has software to communicate through this port to a terminal. See Section 1.5 for connection information.