W65C265SXB
65xxcelr8r Board
Datasheet

DOCUMENT REVISION HISTORY

Version	Date	Author	Description
1.0	1-May-13	David Gray	Initial Document Entry
1.1	13-June-14	David Gray	Reformatted Datasheet. Completed all diagrams and descriptions. First public release.
1.2	31-Oct-14	David Gray	Updated Block and Board Diagrams.

Contents

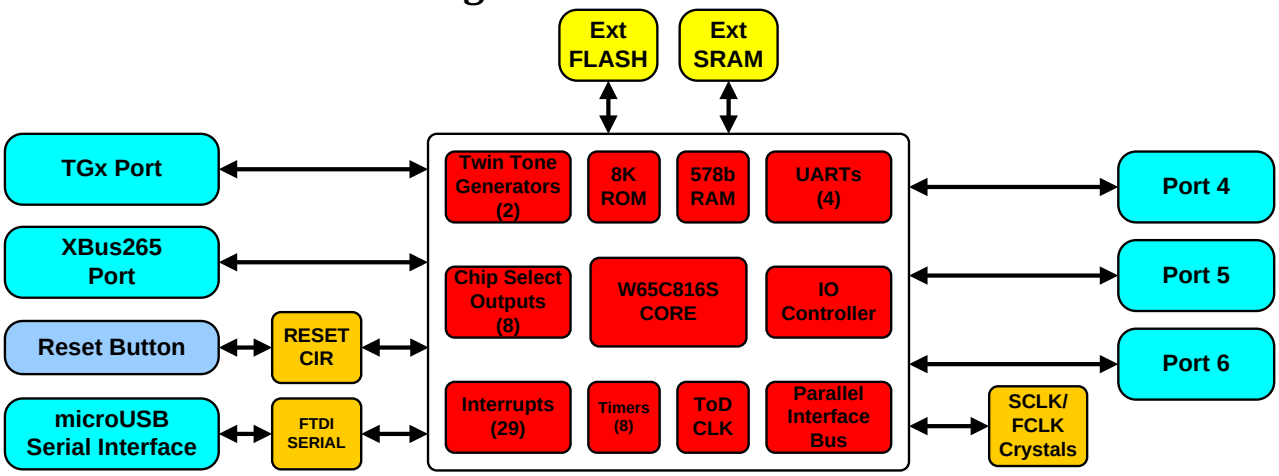
1 Introduction and Features

The W65C265SXB is based around the W65C265S which is a feature rich 8/16–bit microcontroller based on the W65C816. With proven functionality for applications in production that require in-system diagnostics, the SXB is a perfect solution, featuring internal system monitor ROM. If you need robust math for applications in sensing, such as pressure, temperature, revolutions per minute, flow monitoring and control, variable climate control or other systems for scientific, automotive, communications, home appliance/automation, then you'll benefit from our ANSI Standard C compiler.

1.1 Feature List

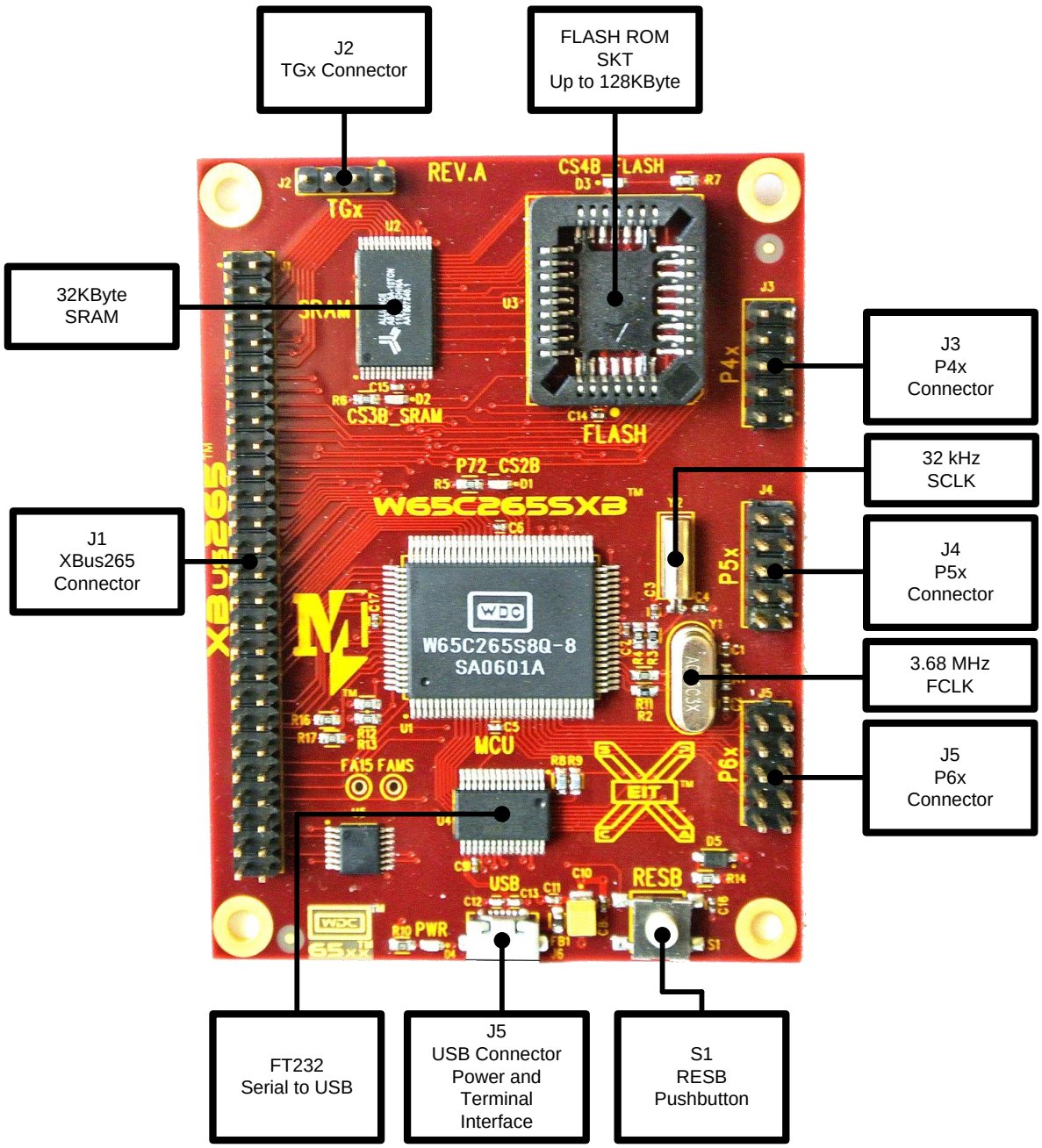
- W65C265S MCU operating at 3.6864 MHz
- 1 x 32Kbytes SRAM
- 1 x 128Kbytes FLASH ROM (32PLCC Socket) mapped as upper 32KB of Memory Map with overlays off of 2 IO pins from the W65C265S (P43 = FA15; P44 = FAMS).
- 1 x XBus265 Connector (50 Pin) with full Data, Address and Control lines for system expansion
- Twin Tone Generator Connector (Driven by TG0/1)
- 3 x 10 IO Connectors (Ports 4/5/6)
- TIDE Programming Interface – FTDI232 UART Interfaced to S3 (P66/P67/P56/P57) Serial Port of the W65C265S using the MASK Serial Monitor.
- 5V Powered by Micro USB Connector

1.2 Functional Block Diagram



W65C265S Microcontroller

1.3 Board Diagram



2.5" x 3.25" PCB

1.4 Quick Reference Guide – Memory Map

W65C265SXB Memory Map				
Start	*End*	*Size*	*Chip Select*	*Description*
(C0)	(FF)	4 MB	CS7B	USER MEMORY (FOR EXPANSION)
(40)	(BF)	8 MB	CS6B	USER MEMORY (FOR EXPANSION)
(00)	(3F)	4 MB	CS5B	MEMORY *See Note 2*
(00)E000	(00)FFFF	8192 B	CS4B	ROM MEMORY (*Note 1*)
(00)8000	(00)DEFF	24320 B		ROM MEMORY (*Note 1*)
(00)0200	(00)7FFF	32256	CS3B	Cache Memory *See Note 3*
(00)FF00	(00)FFFF	256 B	CS2B	On Chip Interrupt Vectors
(00)E000	(00)FEFF	7936 B		On-Chip ROM
(00)DF80	(00)DFBF	64 B		On-Chip RAM
(00)DF70	(00)DF7F	16 B		On-Chip Comm. Registers
(00)DF50	(00)DF6F	32 B		On-Chip Timer Registers
(00)DF40	(00)DF4F	16 B		On-Chip Control Registers
(00)DF20	(00)DF27	8 B		On-Chip IO Registers
(00)DF00	(00)DF07	8 B		On-Chip IO Registers
(00)0000	(00)01FF	512 B		On-Chip RAM
(00)DFC0	0xDFFF	64 B	CS1B	External Chip Select 1 (P71)
(00)DF00	0xDF1F	32 B	CS0B	External Chip Select 0 (P70) *See Note 4*

Note 1 - When on-chip 8K bytes of ROM are enabled:
- a.) Addresses (00)E000-FFFF will not appear in CS4B chip select decode.
- b.) On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2 - When on-chip ROM, CS3B and/or CS4B are enabled:
- a.) CS5B decode is reduced by the addresses used by same.
- b.) CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3 - When SSCR2 is "0" (internal RAM), then CS3B is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4 - CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0). When (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

1.5 Quick Reference Guide – Expansion Connectors

J1 – XBus816 Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	VSS
3	D0	4	D1
5	D2	6	D3
7	D4	8	D5
9	D6	10	D7
11	A0	12	A1
13	A2	14	A3
15	A4	16	A5
17	A6	18	A7
19	A8	20	A9
21	A10	22	A11
23	A12	24	A13
25	A14	26	A15
27	A16	28	A17
29	A18	30	A19
31	A20	32	A21
33	A22	34	A23
35	P70 / CS0B	36	P71 / CS1B
37	P75 / CS5B	38	P76 / CS6B
39	P77 / CS7B	40	P41 / IRQB
41	P40 / NMIB	42	RESB
43	CLKOB	44	FLCKOB
45	RUN	46	BE
47	RWB	48	PHI2
49	VSS	50	VDD

J2 – TGx Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	TG0
3	VSS	4	TG1

J3 – P4x Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	VSS
3	P40 / NMIB	4	P41 / IRQB
5	P42	6	P43 / FA15
7	P44 / FAMS	8	P45
9	P46	10	P47

J4 – P5x Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	VSS
3	P50 / DTRB0	4	P51 / DSRB0
5	P52 / DTRB1	6	P53 / DSRB1
7	P54 / DTRB2	8	P55 / DSRB2
9	P56 / DTRB3	10	P57 / DSRB3

J5 – P6x Connector			
Pin	Signal Name	Pin	Signal Name
1	VDD	2	VSS
3	P60 / RXD0	4	P61 / TXD0
5	P62 / RXD1	6	P63 / TXD1
7	P64 / RXD2	8	P65 / TXD2
9	P66 / RXD3	10	P67 / TXD3

2. Connector Descriptions

Following are descriptions of main board connectors. For Port pins coming from the W65C265S chip, careful review of the W65C265S Datasheet is recommended.

2.1 XBus Port (J1)

The "XBus265" is a 50-pin male connector with the following signals:

- 8 Data Bus lines (D0-D7)
- 24 Address Bus lines (A0-A15; 64 Kbyte space)
- 5 External Chip Select Lines for expansion (CS0B, CS1B, CS5B-CS7B)
- 9 Control lines (PHI2, RWB, BE, CLKOB, FCLKOB, RUN, RESB, NMIB, IRQB)
- 4 Power and Ground - 2x VSS (Pins 2 and 49) and 2x VDD (Pins 1 and 50)

2.2 PIA Port (J2)

The Twin Tone Generator outputs (TGx) are synthesized 16 step cosine waveform outputs. Each Tone Generator is comprised of a 16 bit timer and a 16 step divider circuit that selects the proper Digital to Analog (DA) output level. The enable bits for the tone generators are located in bits 1 and 2 of the BCR registers. Refer to the W65C265S Datasheet (Section 1.11) for detailed operation information.

2.3 P4x Port (J3)

The P4x Port Connector is an expansion connector that has VDD, VSS and each of the I/O pins from Port 4 on the W65C265S. This is a multipurpose port in that P40 can be an I/O line as well NMIB. P41 can be an I/O line as well as IRQB. P42-P47 are I/O lines in addition to control lines for the Parallel Interface Bus (PIB).

2.4 P5x Port (J4)

The P5x Port Connector is an expansion connector that has VDD, VSS and each of the I/O pins from Port 5 on the W65C265S. This is again a multipurpose port in that P50-57 can be an I/O lines as well as the Data lines for the Parallel Interface Bus (PIB). They can also be configured as the DSRB and DTRB handshake lines for the 4 UARTs of the W65C265S. P56 can also be a Positive Edge Interrupt Input (PE56) and P57 can be a Negative Edge Interrupt Input (NE57).