

APPROVAL SHEET

WA04P

π type chip attenuator

50 Ω , 0dB, 0.5dB to 20dB

Size 1.0 x 1.0 mm

FEATURE

1. Unbalanced π type attenuator circuit in one chip (1.0mm x 1.0mm)
2. Mounting occupation area reduction
3. Mounting assembly cost saving

APPLICATION

- Attenuation, level control, impedance matching of high frequency signals of communication equipment;
- Mobile phone (GSM, CDMA, PDC, etc,...)
- Telecom

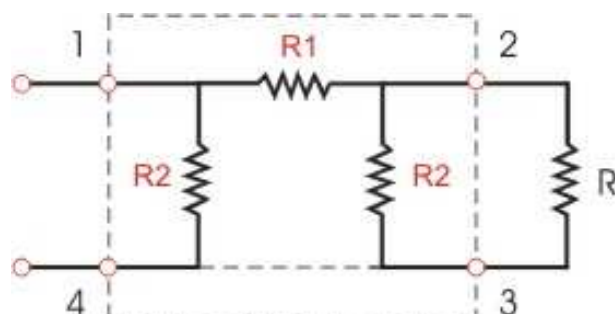
DESCRIPTION

The attenuator is constructed in a high grade ceramic body (aluminum oxide). Internal circuit is applied to the top surface of the substrate, and its design determines the required attenuation value. The attenuation layer is covered with a protective coating and a rectangular marker indicates input pin1 as shown in circuit configuration.



Fig 1. Outline of WA04P Chip attenuator

CIRCUIT CONFIGURATION



QUICK REFERENCE DATA

| Item | General Specification |
|---------------------------------------|-----------------------|
| Series No. | WA04P(Convex type) |
| Size | 1.0 x 1.0 mm |
| Attenuation Range | 0dB, 0.5 dB ~ 20dB |
| Attenuation Tolerance | |
| 0dB | - |
| 0.5 dB | ±0.1dB |
| 1dB ~ 5dB | ±0.3dB |
| 6dB ~ 10dB | ±0.4dB |
| 11dB ~ 13dB | ±0.8dB |
| 14dB | ±1.0dB |
| 15 ~ 16dB | ±1.5dB |
| 17 ~ 19dB | ±2.0dB |
| 20dB | ±2.5dB |
| Characteristic impedance | 50Ω |
| Rated power at T _{amb} =70°C | 0.1 W / package |
| Limiting voltage (DC) | 50V |
| Frequency range (DC) | Max. 3GHz |
| VSWR (Voltage Standing Wave Ratio) | Max. 1.2 |
| Number of Resistors | 3 resistors |
| Number of Terminals | 4 terminals |
| category temperature range | -40 ~ +125 |

DIMENSIONS(mm)

| | WA04P |
|-----------|-----------------|
| L | 1.00 ± 0.10 |
| W | 1.00 +0.10 / -0 |
| T | 0.35 ± 0.10 |
| P | 0.65 ± 0.10 |
| A | 0.33 ± 0.10 |
| Ta | 0.15 ± 0.10 |
| Tb | 0.25 ± 0.10 |

**MARKING**



| | | | | | | | | | | | | | | | | | | | | | | | |
|------|---|-------------|---|-------------|---|---|---|---|---|---|---|---|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| code | 0 | X | 1 | Y | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G | H | J | K | L |
| dB | 0 | 0 . 5 | 1 | 1 . 5 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 1 0 | 1 1 | 1 2 | 1 3 | 1 4 | 1 5 | 1 6 | 1 7 | 1 8 | 1 9 | 2 0 |

FUNCTIONAL DESCRIPTION

Product characterization

Standard attenuation values include 0, 0.5dB to 20dB with a tolerance as defined in quick reference data.

CATALOGUE NUMBERS AND PACKAGING

The attenuators have a catalogue number starting with .

| WA04 | P | 001 | X | B | T | L |
|--|---|--|-----------------------------|---|--|--|
| Size code WA04 : 0402 per element | Type code P : convex, π type attenuator | Attenuation code 000 = 0dB 001 = 1dB 005 = 5dB 010 = 10dB 020 = 20dB R05 = 0.5dB R15 = 1.5dB | Impedance X : 50Ω | Tolerance A : ±0.1dB B : ±0.3dB C : ±0.4dB D : ±0.8dB E : ±1.0dB F : ±1.5dB G : ±2.0dB H : ±2.5dB P : - | Packaging code T : 7" reel taped | Termination code L = Sn base (lead free) |

Packaging : 8mm width paper taping 10,000pcs per reel.

SOLDERING CONDITION

The robust construction of chip resistors allows them to be completely immersed in a solder bath of 260°C for 10 seconds. Therefore, it is possible to mount Surface Mount Resistors on one side of a PCB and other discrete components on the reverse (mixed PCBs).

Surface Mount Resistors are tested for solderability at 235°C during 2 seconds. The test condition for no leaching is 260°C for 30 seconds. Typical examples of soldering processes that provide reliable joints without any damage are given in Fig 3.

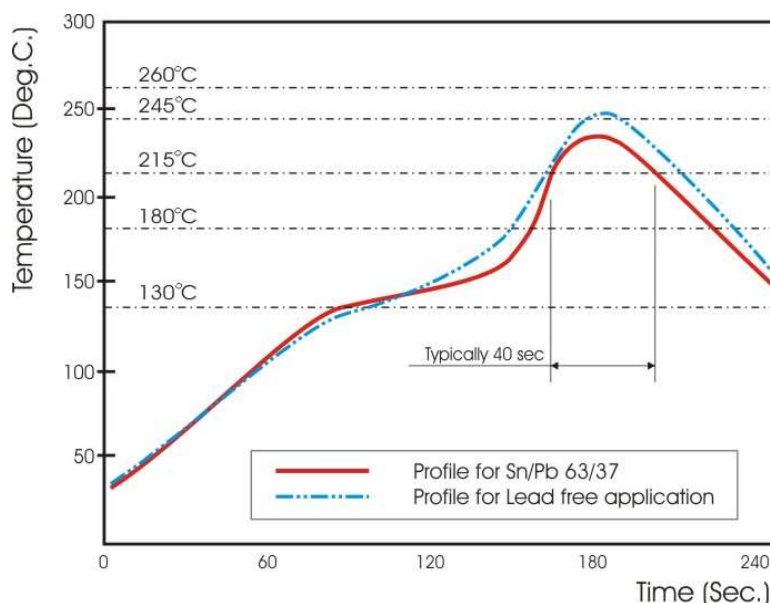


Fig 3. Infrared soldering profile

TEST AND REQUIREMENTS (JIS C 5201-1 : 1998)

| TEST | PROCEDURE | REQUIREMENT |
|---|--|--|
| Characteristic Impedance | Measuring circuit  | 50Ω |
| Insulation resistance Clause 4.6 | Apply the 50VDC for 1minute | At least 100MΩ |
| Solderability Clause 4.17 | Un-mounted chips completely immersed for 2±0.5 second in a SAC solder bath at 235°C±5°C | good tinning (>95% covered) no visible damage |
| Resistance to soldering heat(R.S.H) Clause 4.18 | Un-mounted chips completely immersed for 10±1 second in a SAC solder bath at 260°C±5°C | no visible damage Attenuation 0.5~ 2dB : within ±0.1dB Attenuation 3~ 5dB : within ±0.2dB Attenuation 6~ 20dB : within ±0.3dB |
| Temperature cycling Clause 4.19 | 30 minutes at -55°C±3°C, 2~3 minutes at 20°C+5°C-1°C, 30 minutes at +125°C±3°C, 2~3 minutes at 20°C+5°C-1°C, total 5 continuous cycles | no visible damage Attenuation 0.5~ 2dB : within ±0.1dB Attenuation 3~ 5dB : within ±0.2dB Attenuation 6~ 20dB : within ±0.3dB |
| Load life (endurance) Clause 4.25 | 1000 +48/-0 hours, loaded with RCWV or Vmax in chamber controller 85±2°C, 1.5 hours on and 0.5 hours off | no visible damage Attenuation 0.5~ 2dB : within ±0.1dB Attenuation 3~ 5dB : within ±0.2dB Attenuation 6~ 20dB : within ±0.3dB |
| Dielectric Withstand Voltage Clause 4.7 | Apply the maximum overload voltage (AC) for 1 minute | No breakdown or flashover |