

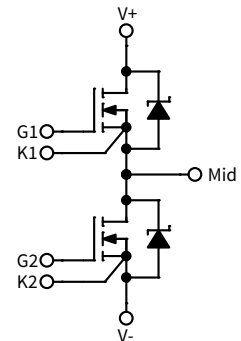
# WAS530M12BM3

1200 V, 530 A, Silicon Carbide, Half-Bridge Module

$V_{DS}$	<b>1200 V</b>
$I_{DS}$	<b>530 A</b>

## Technical Features

- Industry Standard 62mm Footprint
- High Humidity Operation THB-80 (HV-H3TRB)
- Ultra Low Loss , High-Frequency Operation
- Zero Reverse Recovery from Diodes
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator



## Applications

- Induction Heating
- Motor Drives
- Renewables
- Railway Auxiliary & Traction
- EV Fast Charging
- UPS and SMPS

## System Benefits

- 62mm Form Factor Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC

## Maximum Parameters (Verified by Design)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	$V_{DS}$			1200	V		
Gate-Source Voltage, Maximum Value	$V_{GSmax}$	-8		+19		Transient, <100 ns	Fig. 33
Gate-Source Voltage, Recommended	$V_{GSop}$	-4		+15		Static	
DC Continuous Drain Current	$I_D$		630		A	$V_{GS} = 15\text{ V}, T_c = 25\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	Fig. 21
			484			$V_{GS} = 15\text{ V}, T_c = 90\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	
DC Source-Drain Current (Diode)	$I_{SD}$		632			$V_{GS} = -4\text{ V}, T_c = 25\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	
			454			$V_{GS} = -4\text{ V}, T_c = 90\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	
Pulsed Drain Current	$I_{D(pulsed)}$			1060		$t_{pmax}$ limited by $T_{VJmax}$ $V_{GS} = 15\text{ V}, T_c = 25\text{ }^\circ\text{C}$	
Virtual Junction Temperature	$T_{VJop}$	-40		150	°C	Operation	
				175		Intermittent with Reduced Life	

## MOSFET Characteristics (Per Position) ( $T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	$V_{GS} = 0\text{ V}, T_{VJ} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 127\text{ mA}$	
			2.0			$V_{DS} = V_{GS}, I_D = 127\text{ mA}, T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$		12.8	1692	$\mu\text{A}$	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$		60	600	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		2.67	3.47	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 530\text{ A}$	Fig. 2 Fig. 3
			4.30			$V_{GS} = 15\text{ V}, I_D = 530\text{ A}, T_{VJ} = 150\text{ }^{\circ}\text{C}$	
Transconductance	$g_{fs}$		449		S	$V_{DS} = 20\text{ V}, I_D = 530\text{ A}$	Fig. 4
			418			$V_{DS} = 20\text{ V}, I_D = 530\text{ A}, T_{VJ} = 150\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 150\text{ }^{\circ}\text{C}$	$E_{On}$		6.6 6.0 6.0		mJ	$V_{DD} = 600\text{ V},$ $I_D = 530\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(OFF)} = 0.5\text{ }\Omega, R_{G(ON)} = 0.5\text{ }\Omega,$ $L = 13.6\text{ }\mu\text{H}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 150\text{ }^{\circ}\text{C}$	$E_{Off}$		8.9 9.0 9.0				
Internal Gate Resistance	$R_{G(int)}$		1.68		$\Omega$	$f = 100\text{ kHz}, V_{AC} = 25\text{ mV}$	
Input Capacitance	$C_{iss}$		38.9		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
Output Capacitance	$C_{oss}$		2.6				
Reverse Transfer Capacitance	$C_{rss}$		48.5				
Gate to Source Charge	$Q_{GS}$		384		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V},$ $I_D = 530\text{ A},$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	$Q_{GD}$		462				
Total Gate Charge	$Q_G$		1362				
FET Thermal Resistance, Junction to Case	$R_{thJC}$		0.075		$^{\circ}\text{C}/\text{W}$		Fig. 17

## Diode Characteristics (Per Position) ( $T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	$V_F$		2.0		V	$V_{GS} = -4\text{ V}, I_F = 530\text{ A}, T_{VJ} = 25\text{ }^{\circ}\text{C}$	Fig. 7
			2.6			$V_{GS} = -4\text{ V}, I_F = 530\text{ A}, T_{VJ} = 150\text{ }^{\circ}\text{C}$	
Reverse Recovery Time	$t_{rr}$		25.5		ns	$V_{GS} = -4\text{ V}, I_{SD} = 530\text{ A}, V_R = 800\text{ V}$ $di/dt = 18.0\text{ A/ns}, T_{VJ} = 150\text{ }^{\circ}\text{C}$	Fig. 32
Reverse Recovery Charge	$Q_{rr}$		4.8		$\mu\text{C}$		
Peak Reverse Recovery Current	$I_{rrm}$		324		A		
Reverse Recovery Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 150\text{ }^{\circ}\text{C}$	$E_{rr}$		1.9 2.2 2.2		mJ	$V_{DS} = 600\text{ V}, I_D = 530\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ext)} = 0.5\text{ }\Omega,$ $L = 13.6\text{ }\mu\text{H}$	Fig. 14 Note 1
Diode Thermal Resistance, JCT. to Case	$R_{thJC}$		0.078		$^{\circ}\text{C}/\text{W}$		Fig. 18

Note:

<sup>1</sup> SiC Schottky diodes do not have reverse recovery energy but still contribute capacitive energy.



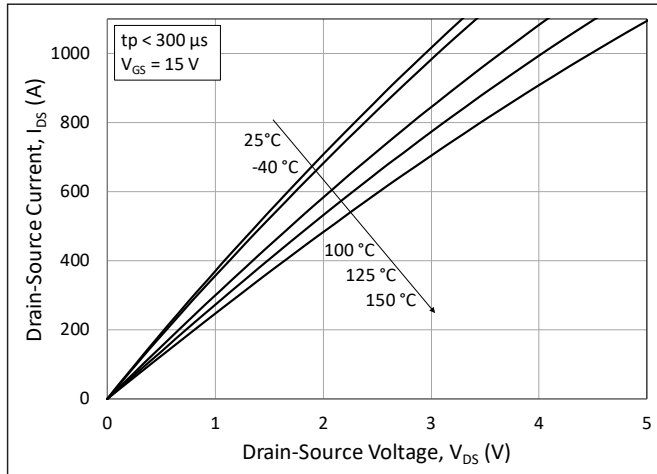
## Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Package Resistance, M1 (High-Side)	$R_{3-1}$		0.90		m $\Omega$	$T_C = 25\text{ }^\circ\text{C}$ , $I_{SD} = 530\text{ A}$ , Note 2	
			1.26			$T_C = 125\text{ }^\circ\text{C}$ , $I_{SD} = 530\text{ A}$ , Note 2	
Package Resistance, M2 (Low-Side)	$R_{1-2}$		0.97	$T_C = 25\text{ }^\circ\text{C}$ , $I_{SD} = 530\text{ A}$ , Note 2			
			1.36	$T_C = 125\text{ }^\circ\text{C}$ , $I_{SD} = 530\text{ A}$ , Note 2			
Stray Inductance	$L_{Stray}$		11.1		nH	Between DC- and DC+, $f = 10\text{ MHz}$	
Case Temperature	$T_C$	-40		125	$^\circ\text{C}$		
Mounting Torque	$M_S$		4	5	5.5	N-m	Baseplate, M6-1.0 bolts
			4	5	5.5		Power Terminals, M6-1.0 bolts
Weight	$W$		300		g		
Case Isolation Voltage	$V_{isol}$	5			kV	AC, 50 Hz, 1 minute	
Clearance Distance			9		mm	Terminal to Terminal	
			30			Terminal to Baseplate	
Creepage Distance			30			Terminal to Terminal	
			40			Terminal to Baseplate	

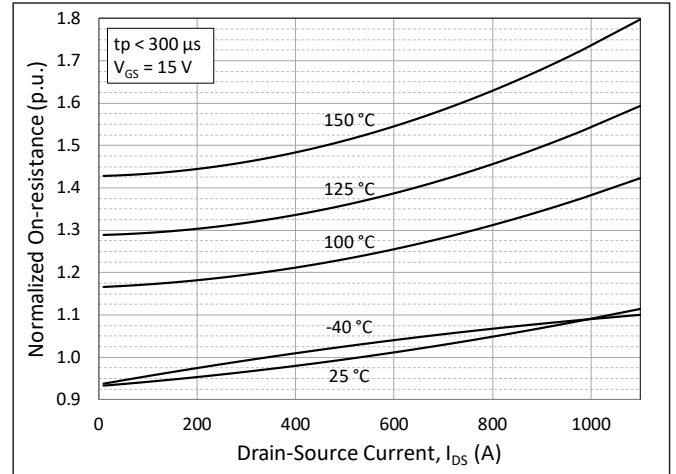
Note:

<sup>2</sup>Total Effective Resistance (Per Switch Position) = MOSFET  $R_{DS(on)}$  + Switch Position Package Resistance

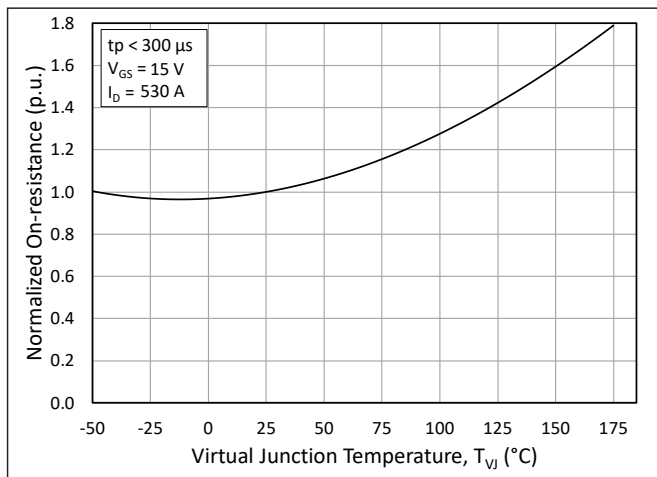
### Typical Performance



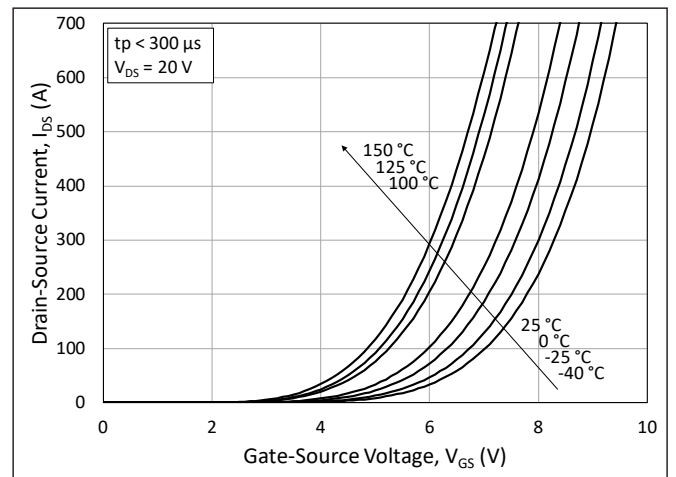
**Figure 1.** Output Characteristics for Various Junction Temperatures



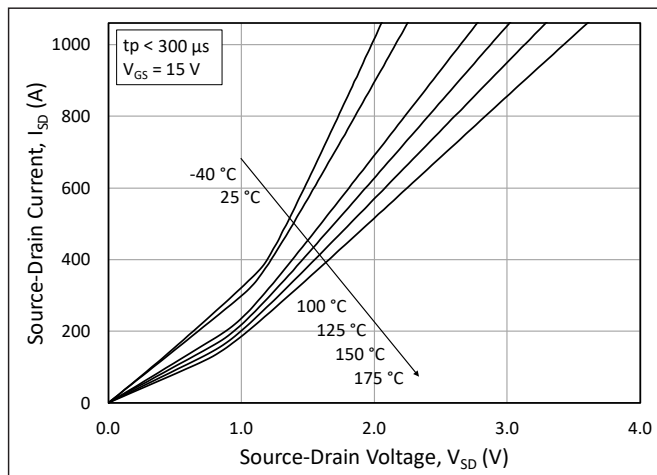
**Figure 2.** Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures



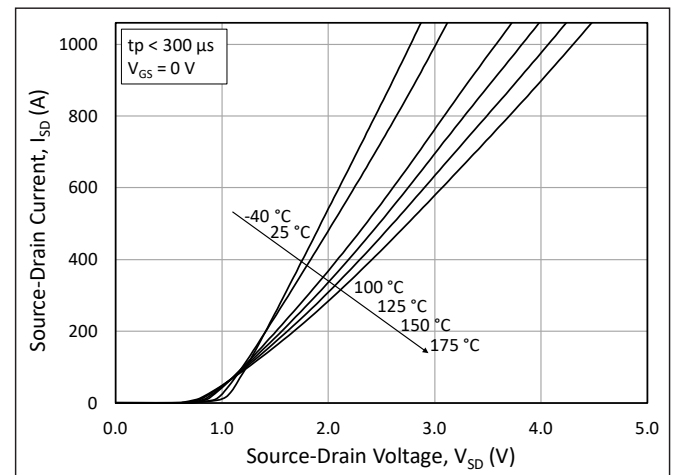
**Figure 3.** Normalized On-State Resistance vs. Junction Temperature



**Figure 4.** Transfer Characteristic for Various Junction Temperatures



**Figure 5.** 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 15\text{ V}$



**Figure 6.** 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 0\text{ V}$  (Diode)



Typical Performance

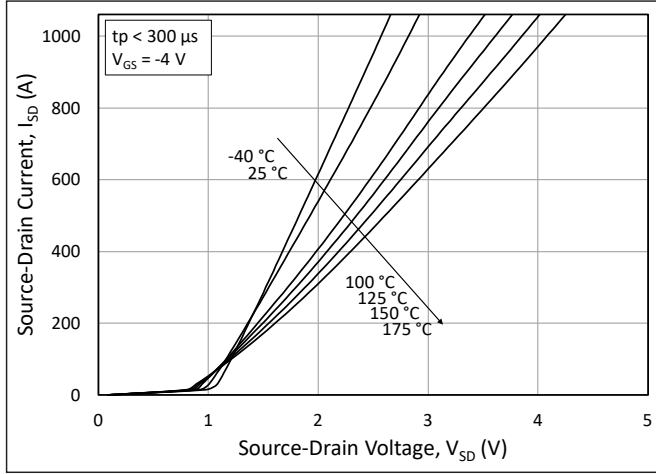


Figure 7. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = -4$  V (Diode)

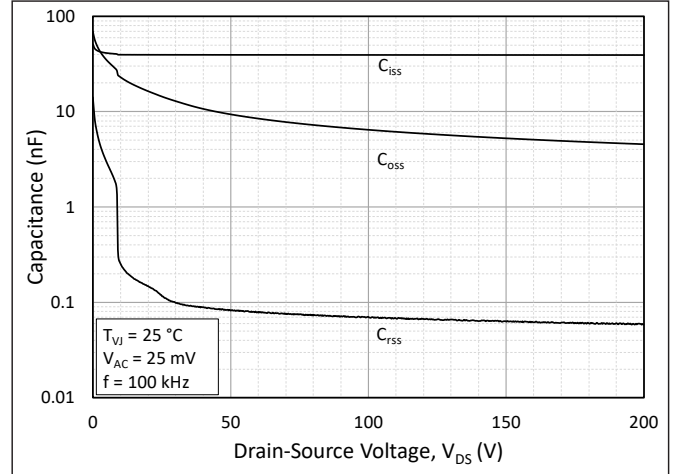


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

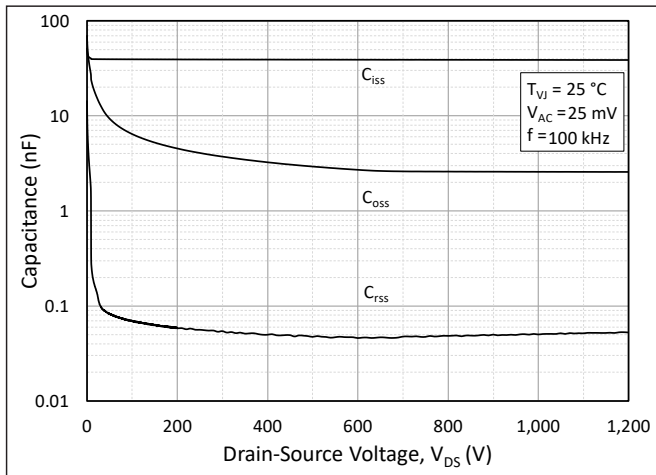


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

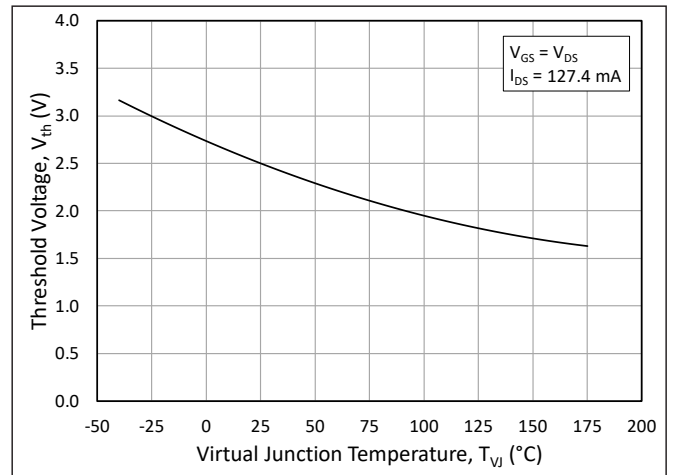


Figure 10. Threshold Voltage vs. Junction Temperature

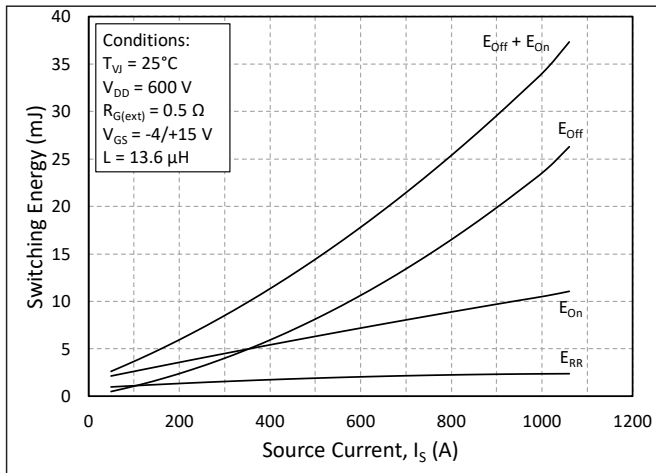


Figure 11. Switching Energy vs. Drain Current ( $V_{DS} = 600$  V)

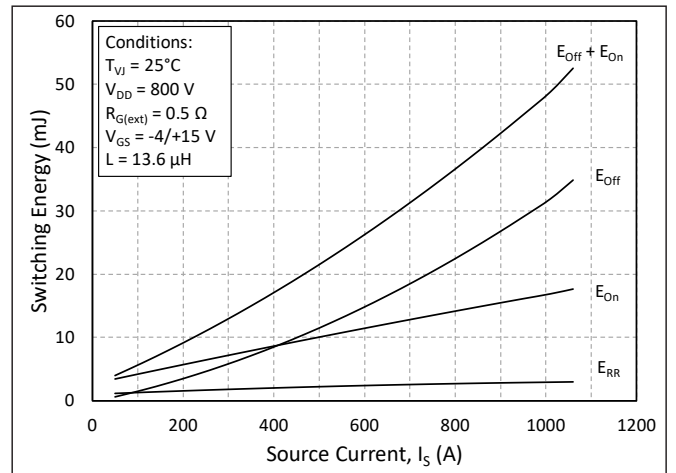


Figure 12. Switching Energy vs. Drain Current ( $V_{DS} = 800$  V)



Typical Performance

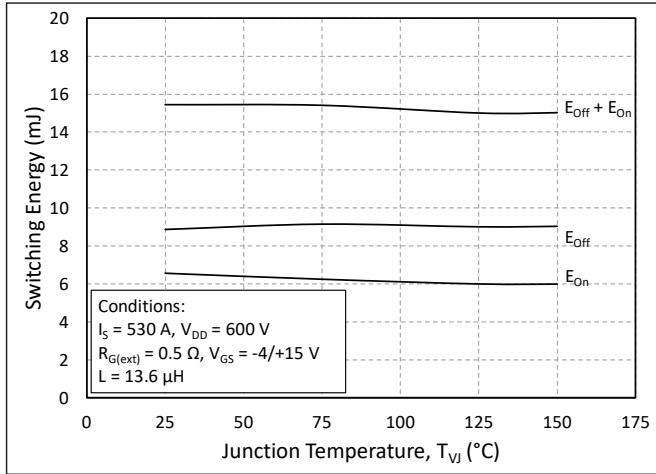


Figure 13. MOSFET Switching Energy vs. Junction Temperature

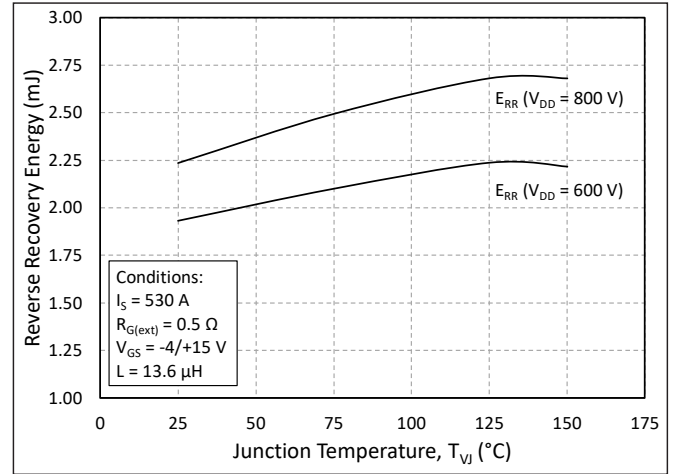


Figure 14. Reverse Recovery Energy vs. Junction Temperature

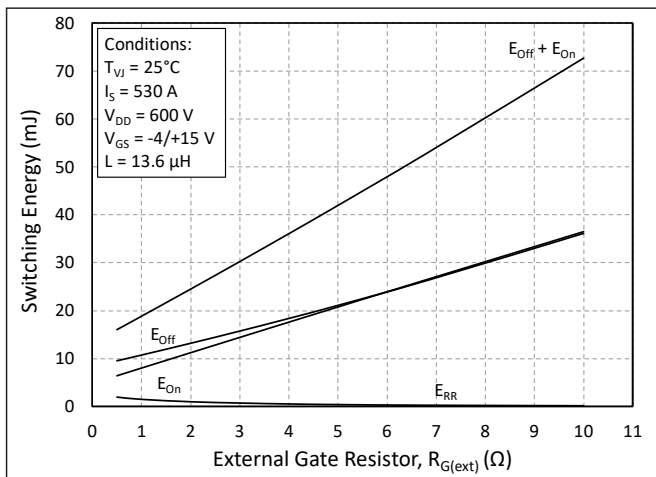


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

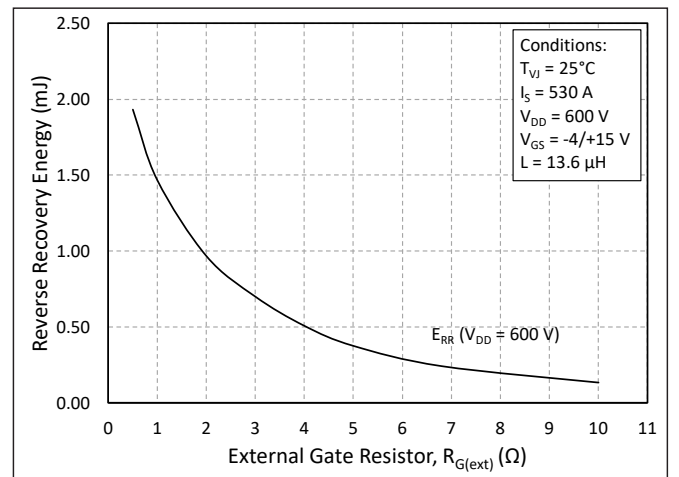


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

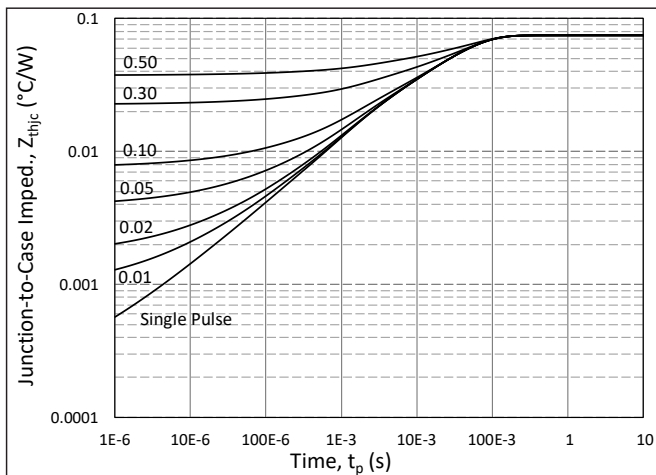


Figure 17. MOSFET Junction to Case Transient Thermal Impedance,  $Z_{thjc}$  (°C/W)

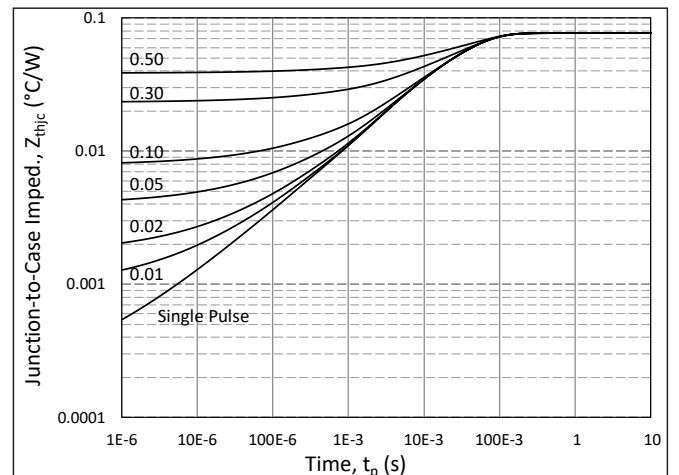


Figure 18. Diode Junction to Case Transient Thermal Impedance,  $Z_{thjc}$  (°C/W)



Typical Performance

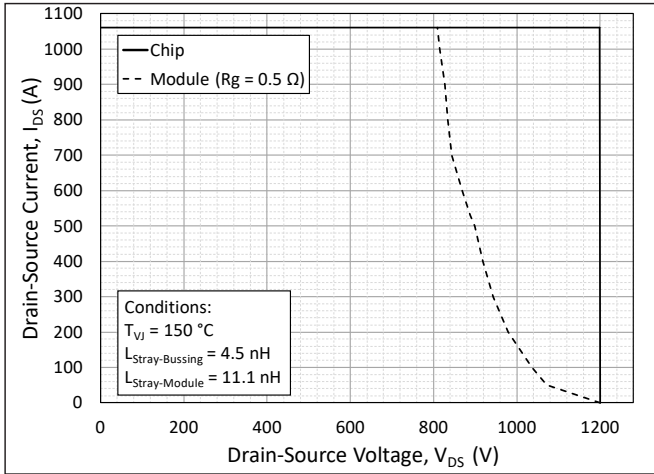


Figure 19. Switching Safe Operating Area

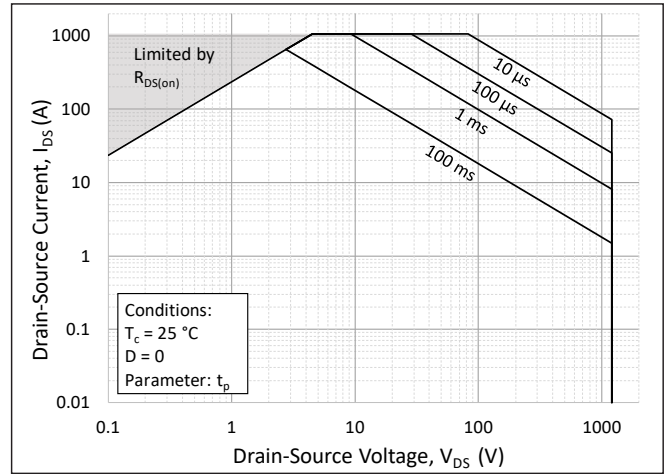


Figure 20. Forward Bias Safe Operating Area (FBSOA)

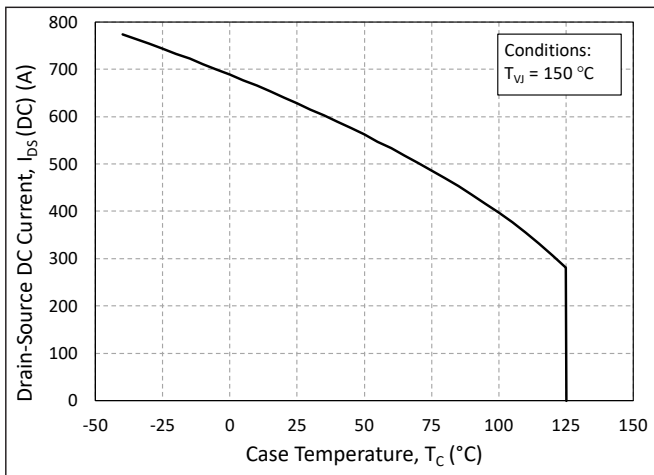


Figure 21. Continuous Drain Current Derating vs. Case Temperature

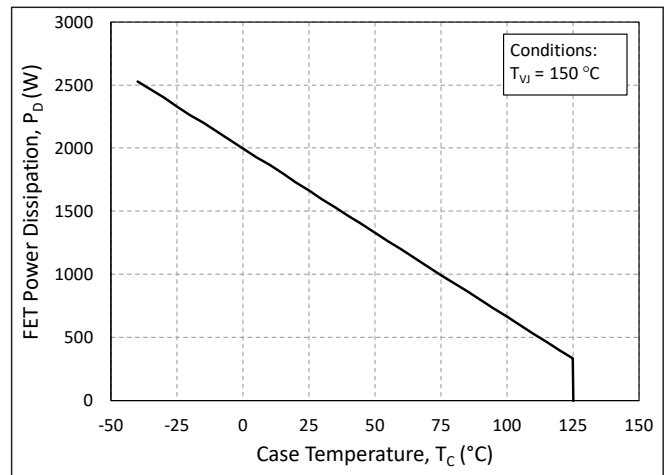


Figure 22. Maximum Power Dissipation Derating vs. Case Temperature

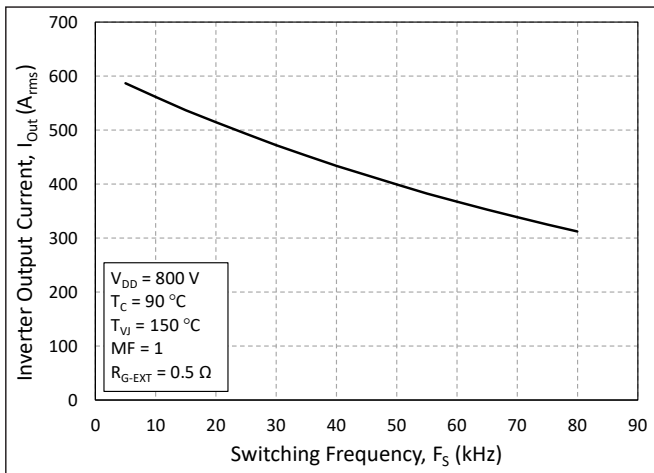


Figure 23. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

### Timing Characteristics

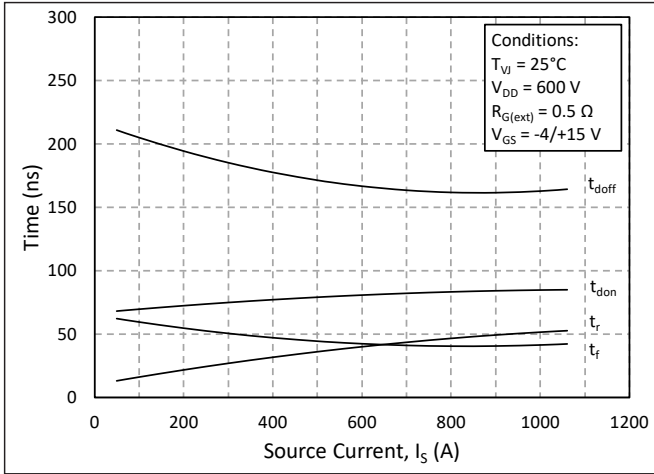


Figure 24. Timing vs. Source Current

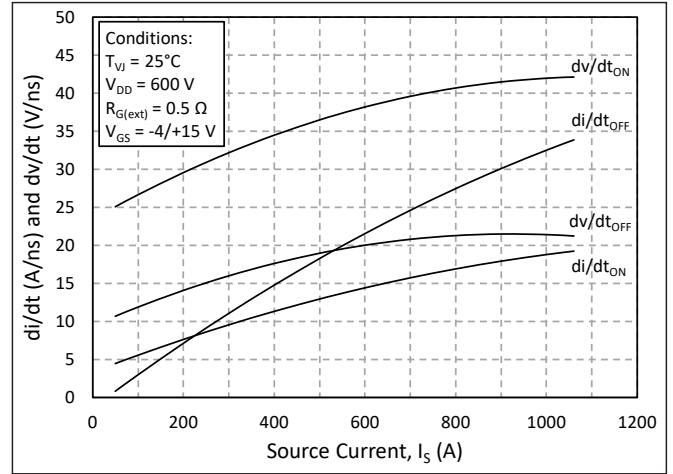


Figure 25.  $dv/dt$  and  $di/dt$  vs. Source Current

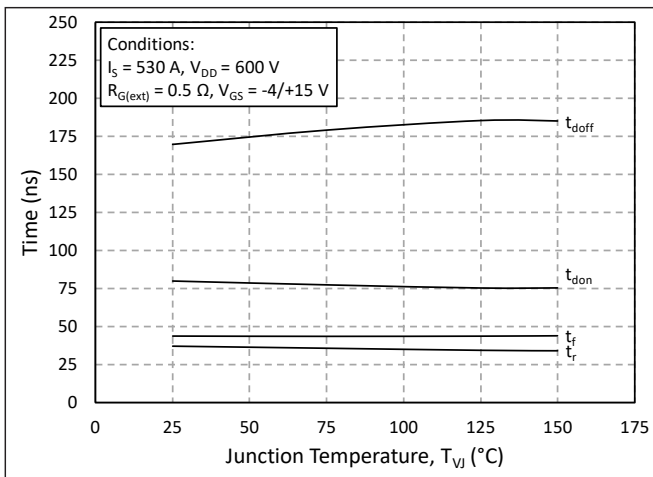


Figure 26. Timing vs. Junction Temperature

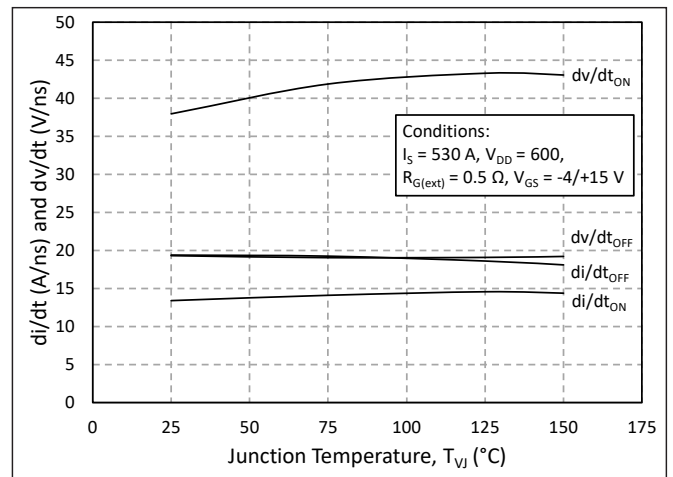


Figure 27.  $dv/dt$  and  $di/dt$  vs. Junction Temperature

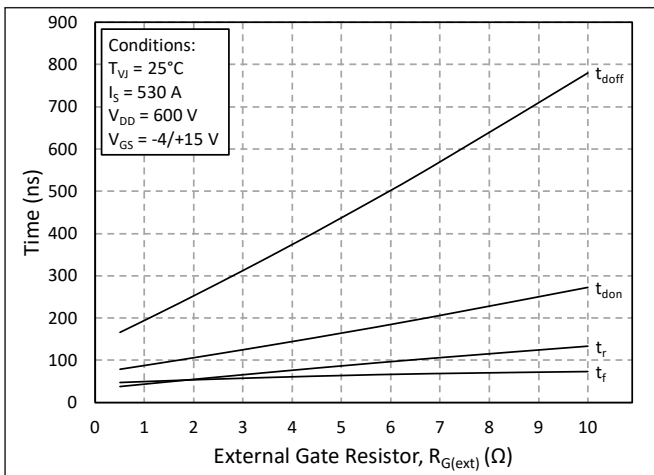


Figure 28. Timing vs. External Gate Resistance

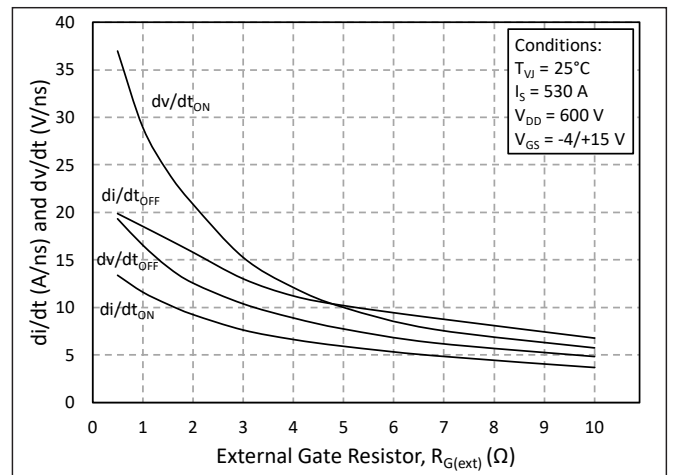
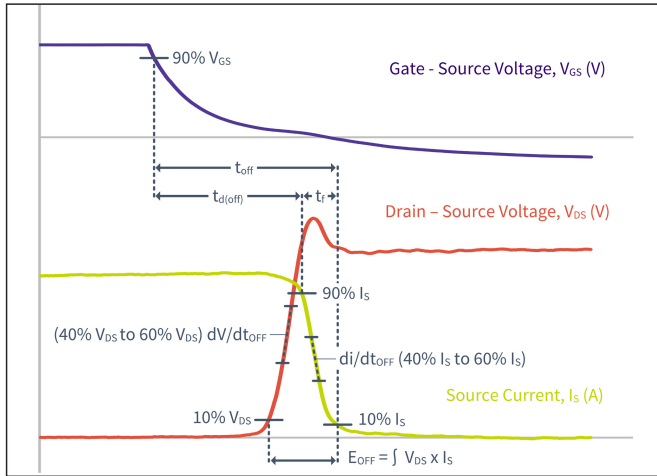


Figure 29.  $dv/dt$  and  $di/dt$  vs. External Gate Resistance

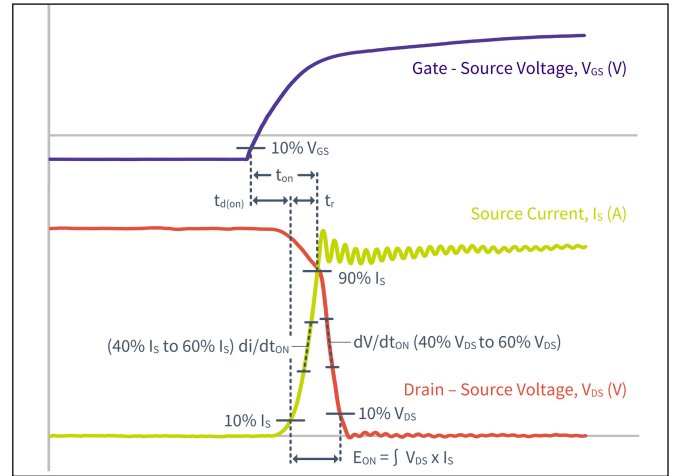




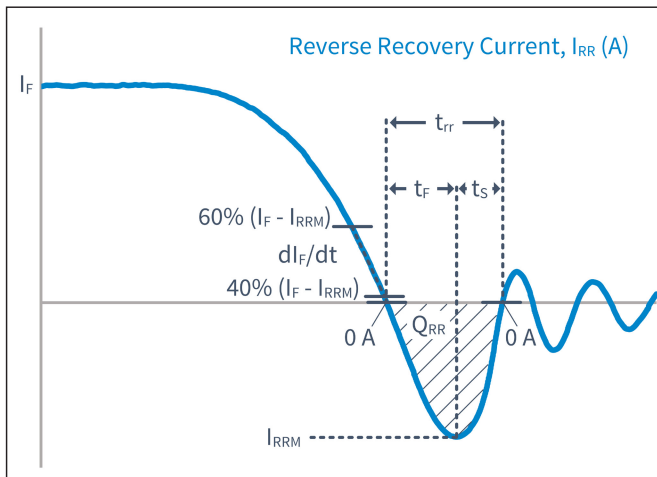
**Definitions**



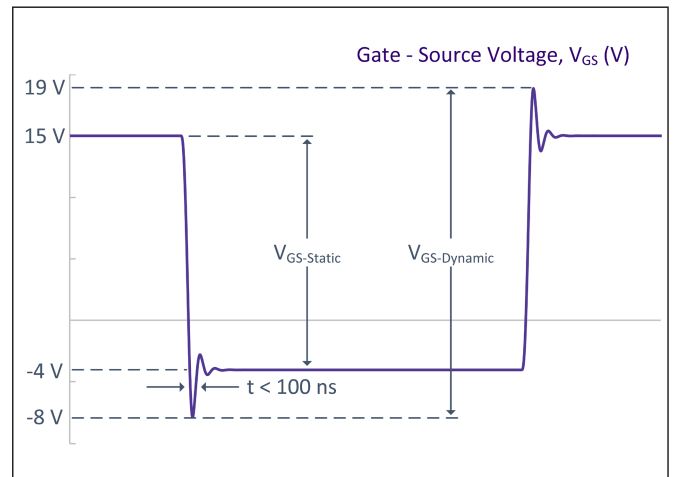
**Figure 30. Turn-off Transient Definitions**



**Figure 31. Turn-on Transient Definitions**



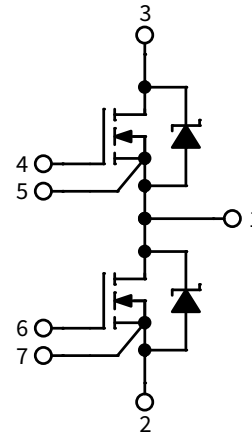
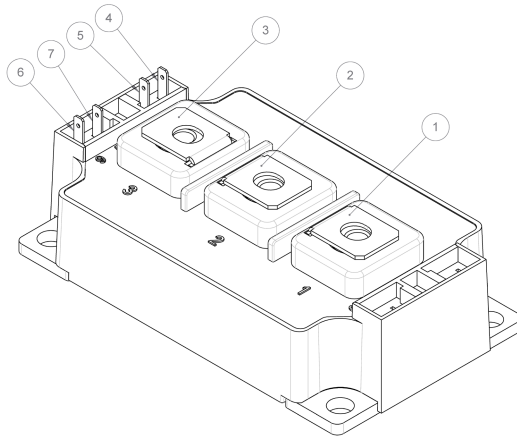
**Figure 32. Reverse Recovery Definitions**



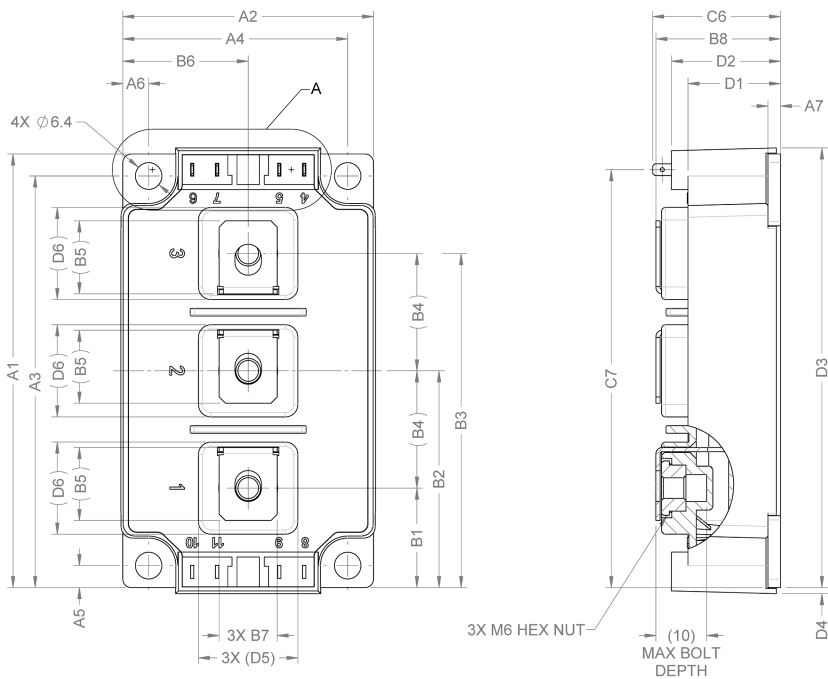
**Figure 33. V<sub>GS</sub> Transient Definitions**



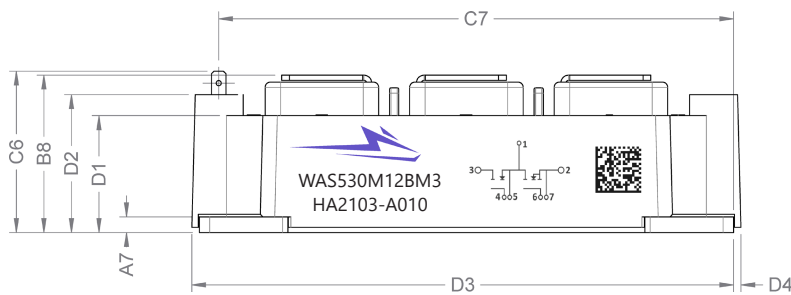
### Schematic and Pin Out



### Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	103.5	±0.30
A2	60.44	±0.30
A3	98.25	±0.30
A4	54.22	±0.30
A5	5.25	±0.30
A6	6.22	±0.30
A7	3	±0.30
B1	23.75	±0.40
B2	51.75	±0.40
B3	79.75	±0.40
B4	(28)	REF.
B5	(17.43)	REF.
B6	30.23	±0.40
B7	(14)	REF.
B8	30.03	±0.40
C1	16.73	±0.40
C2	22.73	±0.40
C3	37.73	±0.40
C4	43.73	±0.40
C5	2.8	±0.40
C6	30.8	±0.50
C7	99.75	±0.40
C8	(6)	REF.
C9	(15)	REF.
D1	22.3	±0.30
D2	26.3	±0.30
D3	104.95	±0.30
D4	1.45	±0.40
D5	(24)	REF.
D6	(22)	REF.





## Supporting Links & Tools

### Evaluation Tools & Support

- [WAS530M12BM3 PLECS Model](#)
- [KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 and BM3 Module](#)
- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)

### Dual-Channel Gate Driver Board

- [CGD1200HB2P-BM3: Dual Channel Differential Isolated Half Bridge Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

### Application Notes

- [CPWR-AN35: 62mm Module Thermal Interface Material Application Note](#)
- [CPWR-AN34: 62mm Module Mounting Guide Application Note](#)
- [CPWRAN12: Understanding the Effects of Parasitic Inductance Part 1.](#)
- [CPWRAN13: Understanding the Effects of Parasitic Inductance Part 2.](#)