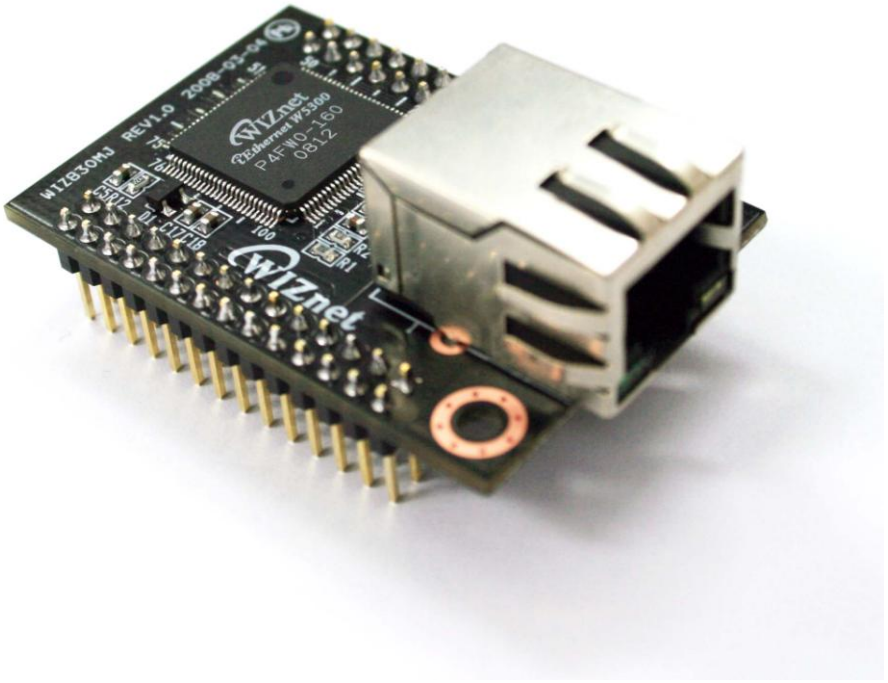
WIZ830MJ Datasheet

(Ver. 1.3)



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Document History Information

Revision	Data	Description
Ver.1.0	June 04, 2008	Release with WIZ830MJ Launching
Ver.1.1	July 29, 2008	Modified dimensions(Symbol B and C).
Ver.1.2	March 4, 2010	Pin number of A[9:0] modified in Chapter 2.3
Ver.1.3	January 28, 2013	Hardware revision(Rev1.1) Changed just partlist at this revision

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Table of Contents

1. Introduction

WIZ830MJ is the network module that includes W5300 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5300 and Transformer. The WIZ830MJ is an ideal option for users who want to develop their Internet enabling systems rapidly.
For the detailed information on implementation of Hardware TCP/IP, refer to the W5300 Datasheet.

WIZ830MJ consists of W5300 and MAG-JACK.

- TCP/IP, MAC protocol layer: W5300
- Physical layer: Included in W5300
- Connector: MAG-JACK(RJ45 with Transformer)

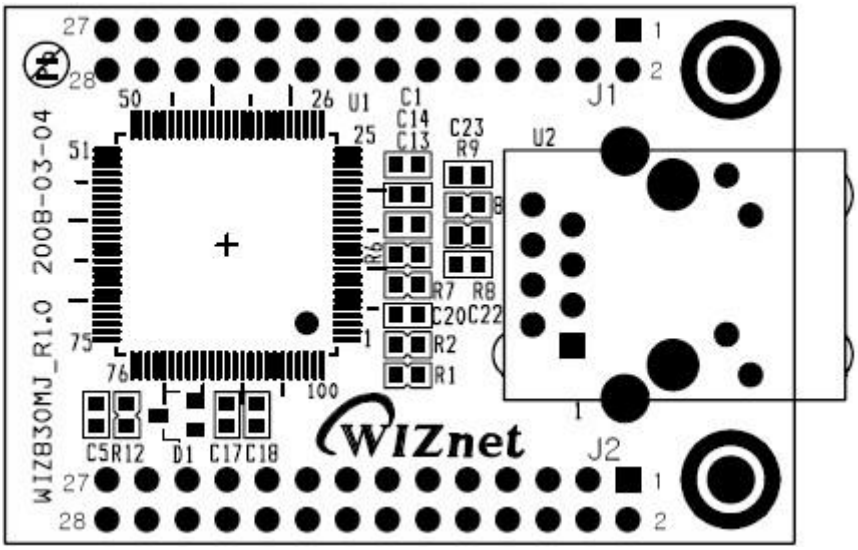
1.1. Features

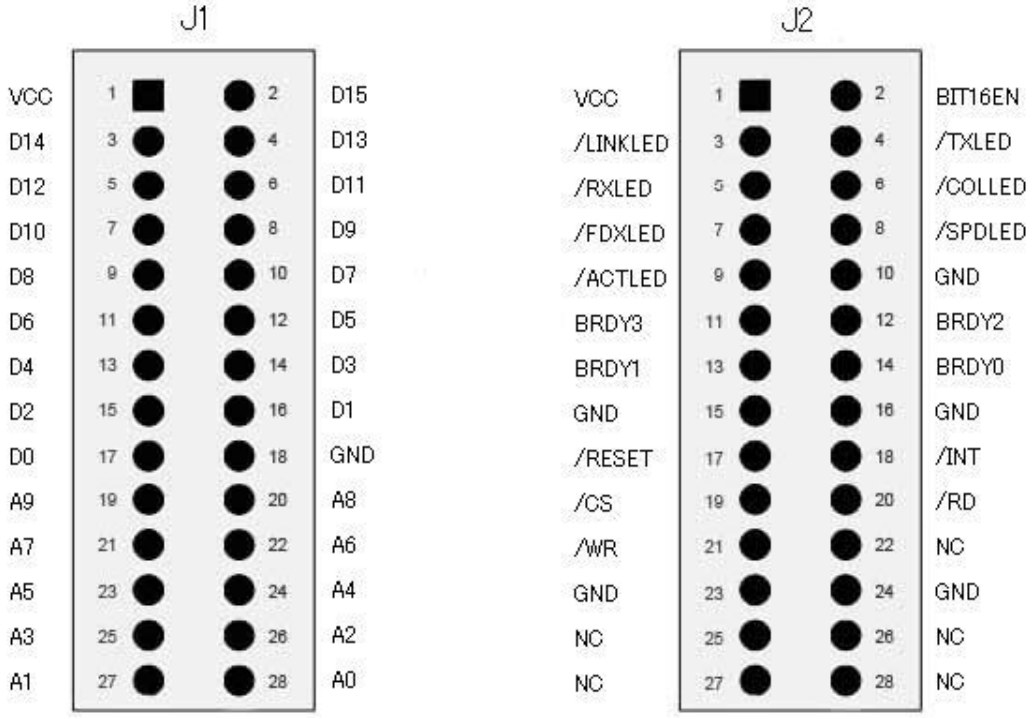
- Supports 10/100 Base TX
- High network performance : Up to 50Mbps
- Supports half/full duplex operation
- Supports auto-negotiation and auto cross-over detection
- IEEE 802.3/802.3u Compliance
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 8 independent connections simultaneously
- Supports MCU bus Interface
- Supports Direct/Indirect mode bus access
- Supports 16/8 bit data bus width
- Supports memory-to-memory DMA (only 16bit Data bus width & slave mode)
- Supports Socket API for easy application programming
- Supports hybrid TCP/IP stack(software and hardware TCP/IP stack)
- Supports PPPoE connection (with PAP/CHAP Authentication mode)
- More flexible allocation internal TX/RX memory according to application throughput
- Interfaces with two 2.54mm pitch 2 x 14 header pin

1.2. Block Diagram

2. Pin Assignments & descriptions

2.1. Pin Assignments





I : Input **O : Output**
I/O : Bi-directional Input and output **P : Power**

2.2. Power & Ground

Symbol	Type	Pin No.	Description
VCC	**P**	J1:1, J2:1	**Power** : 3.3 V power supply
GND	**P**	J1:18, J2:10, J2:15, J2:16, J2:23, J2:24	**Ground**

2.3. MCU Interfaces

Symbol	Type	Pin No.	Description
A[9:0]	**I**	J1:19 ~ J1:28	**Address** Used as Address[9-0] pin
D[15:8]	**I/O**	J1:2 ~ J1:9	**Data** 16 bit-wide high data bus In case of using 8 bit data bus, there are driven as High-Z
D[7:0]	**I/O**	J1:10 ~ J1:17	**Data** 16 bit-wide low data bus
/CS	**I**	J2:19	**Module Select** : Active low. /CS of W5300
/RD	**I**	J2:20	**Read Enable** : Active low. /RD of W5300
/WR	**I**	J2:21	**Write Enable** : Active low /WR of W5300
/INT	**O**	J2:18	**Interrupt** : Active low After reception or transmission it indicates that the W5300 requires MCU attention. By writing values to the Interrupt Register(IR) of W5300 the interrupt will be cleared by host. All interrupts can be masked by writing values to the IMR of W5300 (Interrupt Mask Register). For more details refer to the W5300 Datasheet
BIT16EN	I	J2:2	**16/8 bit data bus select**. High : 16 bit data bus Low : 8 bit data bus.

2.4. Network Indicator LED Signals

Symbol	Type	Pin No.	Description
/LINKLED	**O**	J2:3	**Link LED** It indicates the link status of media(10/100M).
/TXLED	O	J2:4	**Transmit activity LED :** Transmit Enable It notifies the output of transmit data through TXOP/TXON (Transmit Activity).
/RXLED	O	J2:5	**Receive activity LED :** Transmit Data It notifies the input of receive data from RXIP/RXIN (Receive Activity)
/COLLED	O	J2:6	**Collision LED :** Transmit Data It notifies when collisions occur. It is valid at half-duplex, and is ignored at full-duplex.
/FDXLED	O	J2:7	**Full duplex LED :** Transmit Data It outputs low at the full-duplex and outputs high at the halfduplex according to auto-negotiation or manual configuration of OP_MODE[2:0].
/SPDLED	O	J2:8	**Link speed LED :** Transmit Data It is asserted low at the 100Mbps and high at the 10Mbps according to auto-negotiation or manual configuration of OP_MODE[2:0].
/ACTLED	O	J2:9	**Activity LED** It notifies the output of transmit data through TXOP/TXON or the input of receive data from RXIP/RXIN.

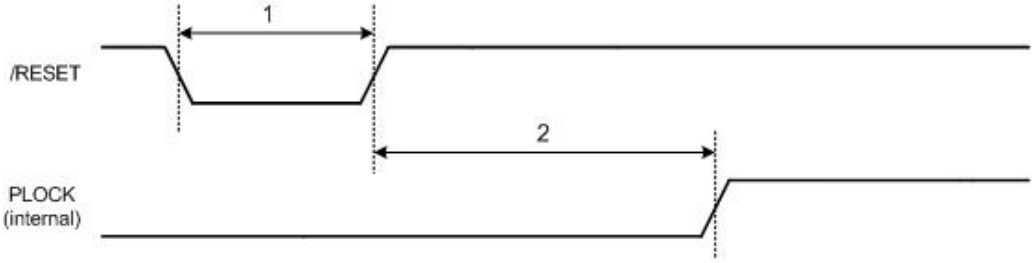
2.5. Miscellaneous Signals

Symbol	Type	Pin No.	Description
/RESET	**I**	J2:17	**Reset :** This pin is active low input to initialize or re-initialize W5300. RESET should be held at least 2us after low assert, and wait for at least 10ms after high de-assert in order for PLL logic to be stable
BRDY[3:0]	O	J2:11 ~ J2:14	**Buffer Ready Indicator** BRDYn monitors TX/RX memory status of each socket. For more details refer to the W5300 Datasheet
NC	-	J2 : 22, J2:25, J2:26, J2:27, J2:28	Not Connect

3. Timing Diagrams

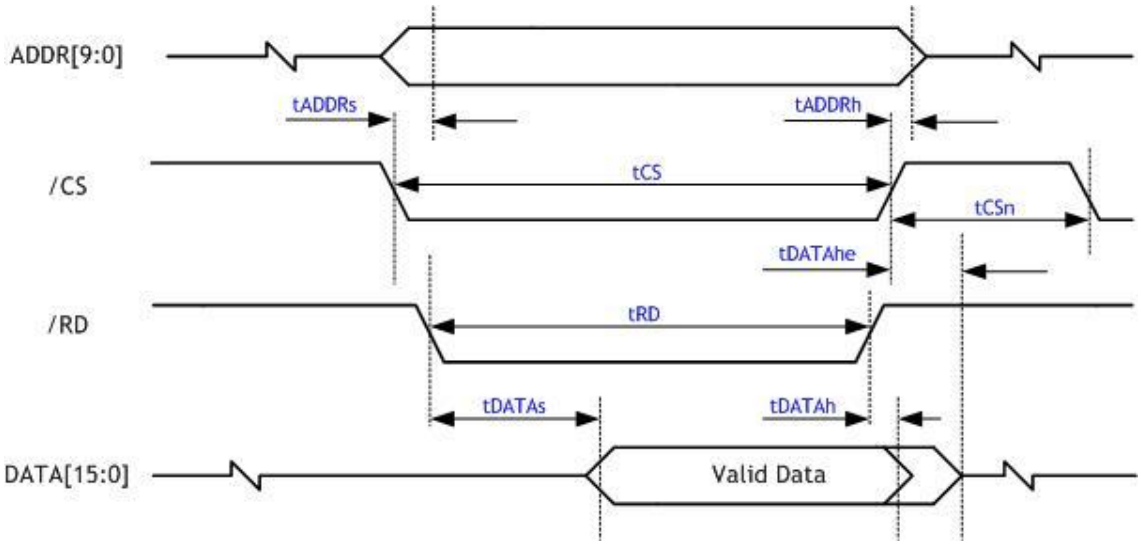
WIZ830MJ provides following interfaces of W5300.
-. Direct/Indirect mode bus access

3.1. Reset Timing



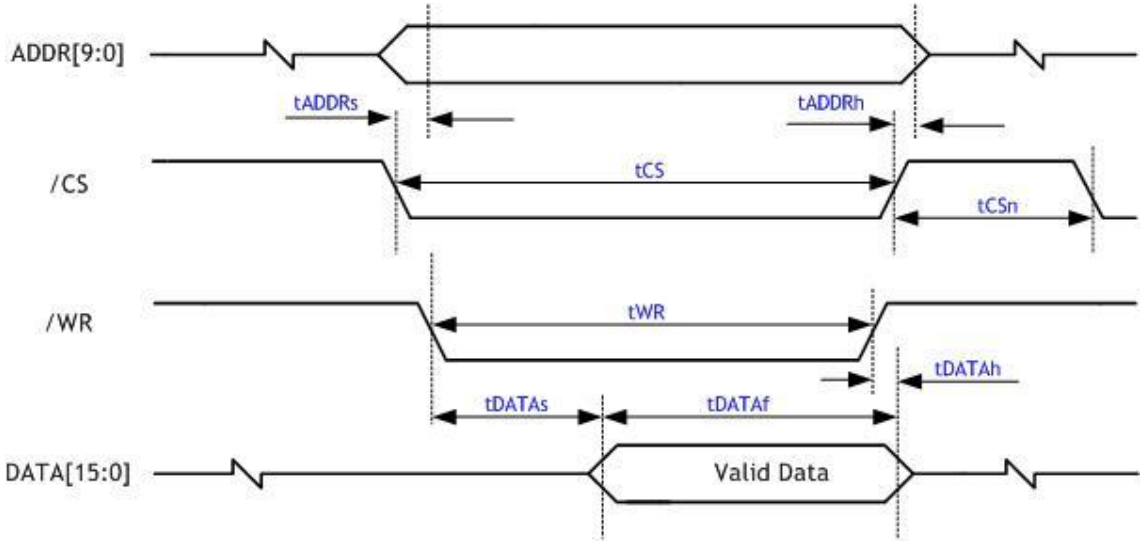
	Description	Min	Max
1	Reset Cycle Time	2 us	-
2	PLL Lock-in Time	50us	10 s

3.2. Register / Memory READ Timing



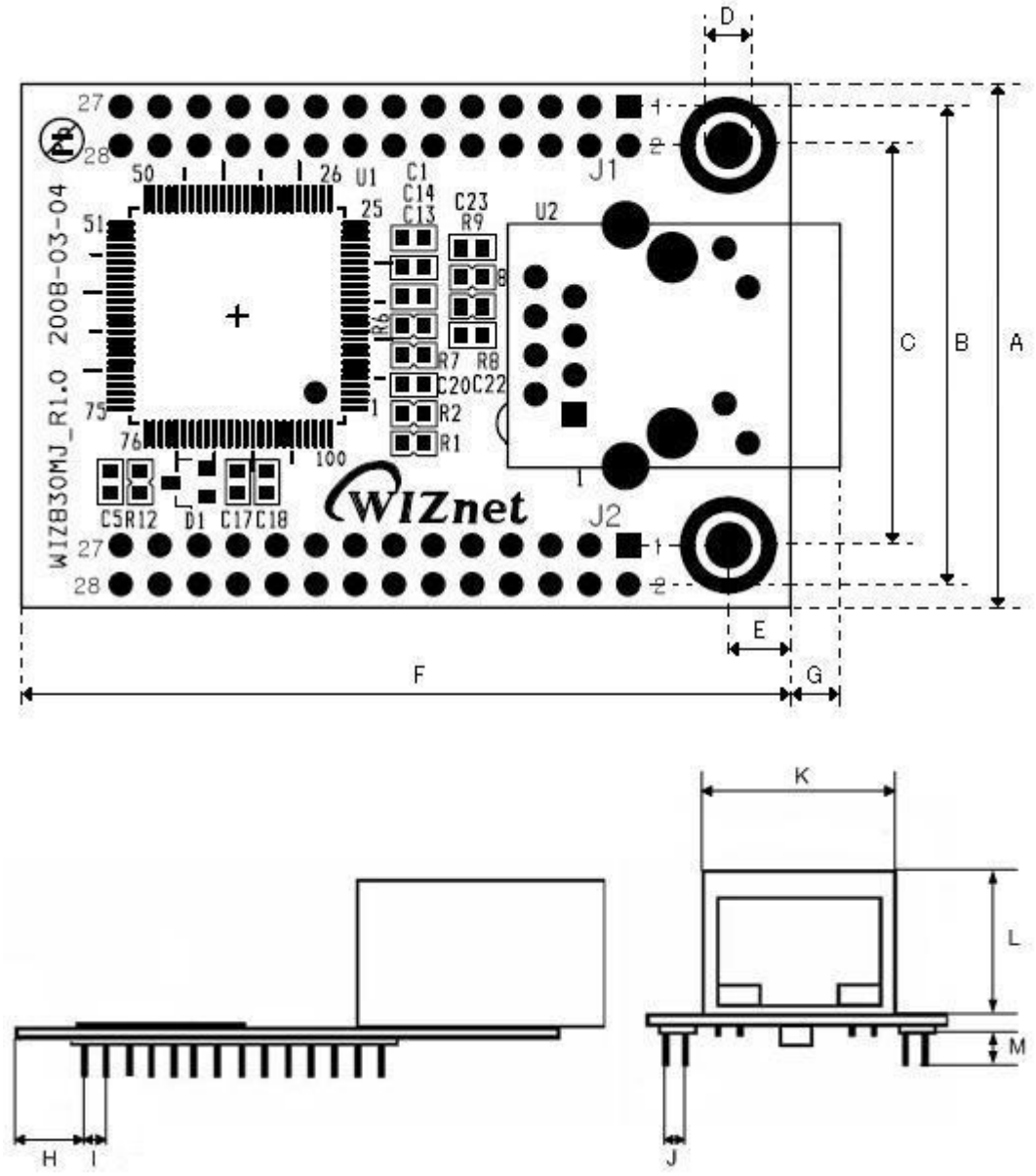
	Description	Min	Max
tADDRs	Address Setup Time after /CS and /RD low	-	7ns
tADDRh	Address Hold Time after /CS and /RD high	-	-
tCS	/CS Low Time	65ns	-
tCSn	/CS Next Assert Time	28ns	-
tRD	/RD Low Time	65ns	-
tDATAs	DATA Setup Time after /RD low	42ns	-
tDATAh	DATA Hold Time after /RD and /CS high	-	7ns
tDATAhe	DATA Hold Extension Time after /CS high	-	2XPLL_CLK

3.3. Register / Memory WRITE Timing



Description		Min	Max
tADDRs	Address Setup Time after /CS and /WR low	-	7ns
tADDRh	Address Hold Time after /CS or /RD high	-	-
tCS	/CS low Time	50ns	-
tCSn	/CS next Assert Time	28ns	
tWR	/WR low Time	50ns	
tDATAs	Data Setup Time after /WR low	7ns	7ns + 7XPLL_CLK
tDATAf	Data Fetch Time	14ns	tWR – tDATAs
tDATAh	Data Hold Time after /WR high	7ns	-

4. Dimensions



Symbols	Dimensions (mm)	Symbols	Dimensions (mm)
A	34.00	H	6.50
B	30.48	I	2.54
C	25.40	J	2.54
D	3.00	K	15.90
E	4.00	L	13.50
F	50.00	M	6.00
G	3.30	-	-

5. Schematic