Wireless charging IC (WLC) 15-W transmitter for automotive applications

General description

WLC1515 is a highly integrated, Qi 1.3.x certifiable wireless power transmitter with an integrated buckboost controller. WLC1515 is ideal for up to 15-W charging applications.

WLC1515 has integrated gate drivers for the BuckBoost and inverter power supplies that are necessary for wireless transmitter applications. WLC1515 supports a wide input voltage range and offers many programmable features for creating distinct wireless transmitter solutions.

WLC1515 is a highly programmable wireless power transmitter solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128KB flash, 16KB RAM, and 32KB ROM. It also includes various analog and digital peripherals such as ADC, PWMs, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals enables scalable multi-coil wireless charging solutions for free positioning transmitter designs.

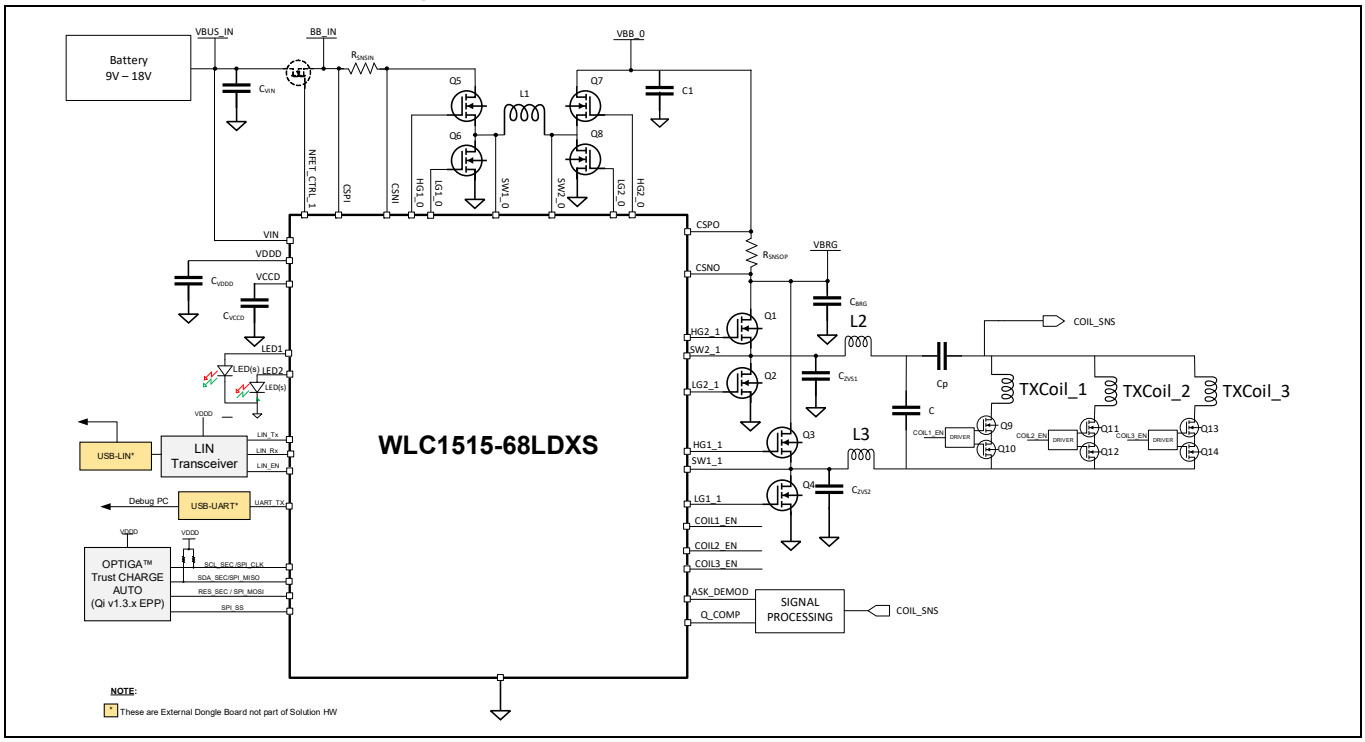
Potential applications

- Wireless charging pads for extended power profile (EPP) (15W) and basic power profile (BPP) (5W)
- Portable accessories
- In-cabin wireless charging application
- Automotive wireless charger

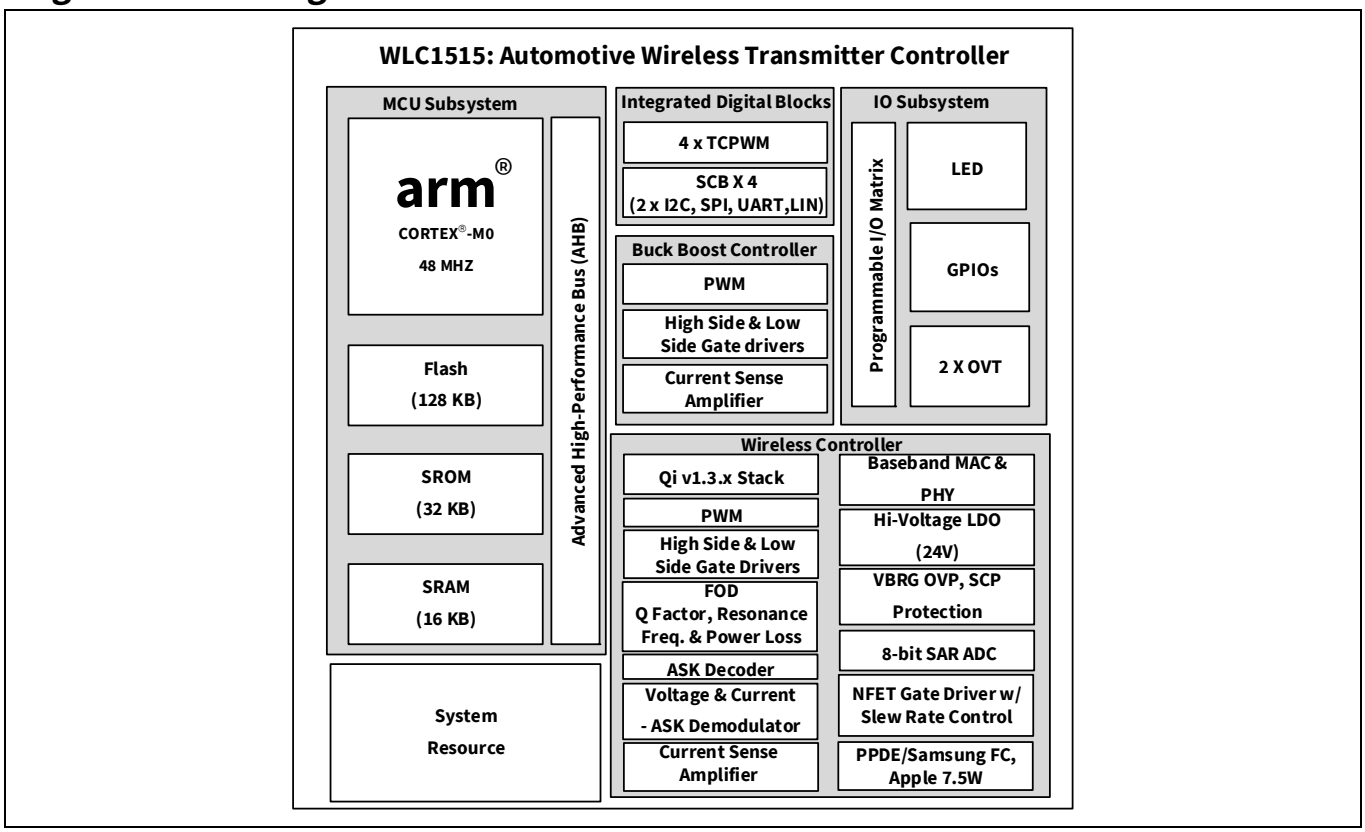
Features

- Qi v1.3.x extended power profile (EPP) and basic power profile (BPP) transmitter (MP-A13 and similar)
- Free positioning
  - Multiple coils (single coil, double coils, and three coils)
- AEC-Q100 qualified
- Integrated buckboost controller for VBRIDGE (VBRG)
- Integrated gate drivers for buckboost converter and inverter
- Integrated Q factor detection
- Integrated FSK modulator
- Integrated ASK decoder
- Integrated FOD by power loss, Qfactor, and resonance frequency
- Wide input voltage range: 4.5V-24V
- Communication ports: I^2C, UART, SPI, and LIN
- **Protection**
  - Overcurrent protection (OCP), overvoltage protection (OVP)
  - Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
- **Temperature range**
  - Supports automotive ambient temperature range (–40°C to +105°C) with 125°C operating junction temperature
- **Package**
  - 68-pin QFN, wettable flank, AEC-Q100

Functional block diagram



Logic block diagram



Note
1. Customers need to acquire their own licensing for Samsung FC.

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1 Application diagram for 15W automotive transmitter solution with MP-A13 Tx coil

Figure 1 illustrates a typical application of WLC1515 for 15W, Qi v1.3.x certifiable transmitter for fixed frequency and voltage control-based MP-A13 Qi transmitter coil. The input power to the system is through an input connector, powering the buckboost converter. The buckboost converter powers the full bridge inverter which in turn drives the transmitter coil. The WLC1515 controls the inverter bridge voltage (VBRG) using the buckboost converter to regulate the power flow to the transmitter coil powering the receiver. The WLC1515 gives control signal to connect one coil to resonant circuits at a time. The WLC1515 provides two dedicated output pin LED0, and LED1 to indicate the status of the Wireless power transmitter. The WLC1515 provides internal device thermal management (DIE temperature) as well as external device thermal management function with an external NTC thermistor connector between TEMP_FB_1 and TEMP_FB_2 to GND as shown in **Figure 1**. A dual opamp is used for converting the amplitude shift key (ASK) modulated power signal into binary signal. WLC1515 uses a digital logic for decoding the binary signals. The OPTIGA™ Trust Security IC is interfaced over I2C/ SPI for authentication requirements per Qi v1.3.x.

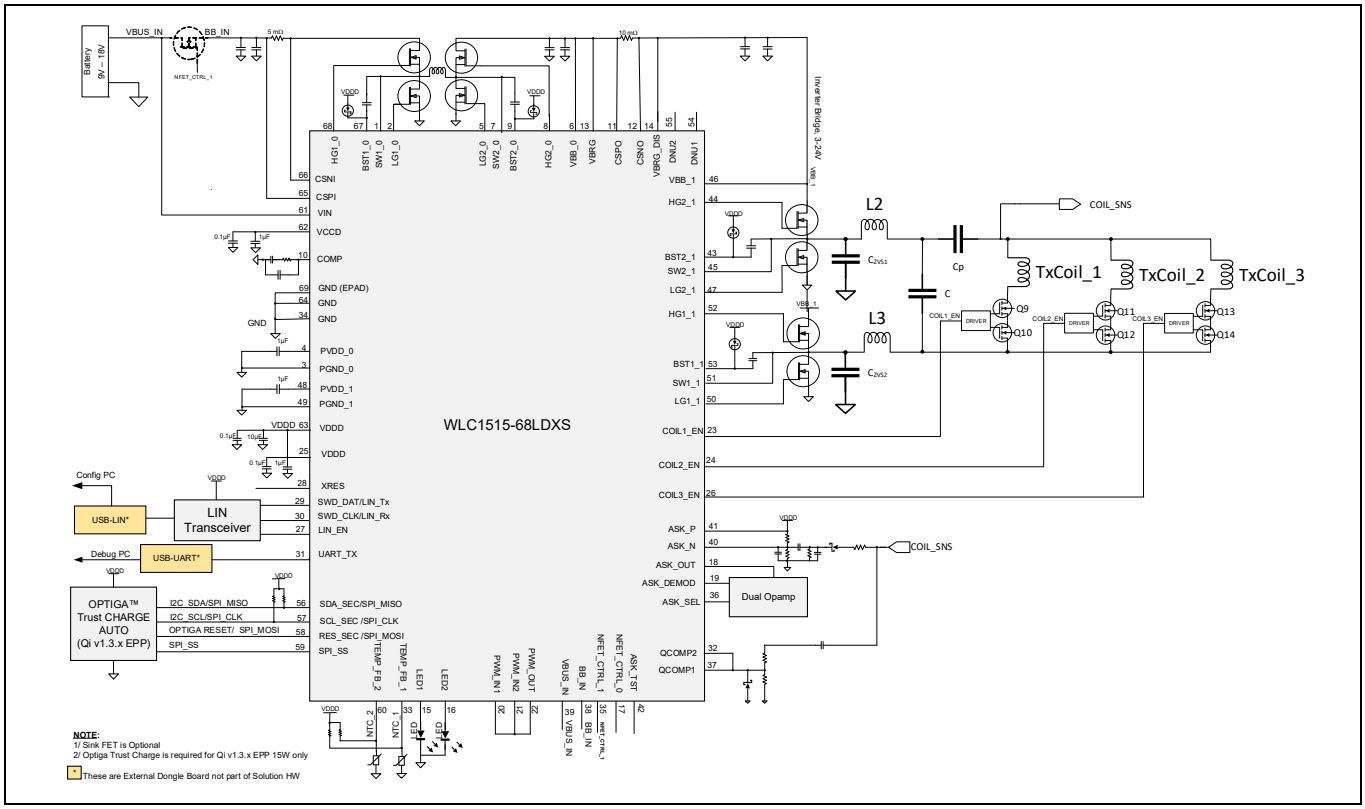


Figure 1 Application diagram for 15W transmitter solution with MP-A13 Tx coil

2 Pin information

Table 1 WLC1515 pinouts

Pin#	WLC1515		Description
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter	
1	SW1_0		Negative power rail of DC-DC converter bank 1's buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
2	LG1_0		Buck low-side gate driver output of (DC-DC bank 1). Connect to the buck (input) side sync (low-side) FET gate. Use a wide trace to minimize inductance of this connection.
3	PGND_0		Ground for gate driver (DC-DC). Connect all grounds (GND) and PGND pins (PNGD_0 and PGND_1) together. Connect directly PCB ground plane and exposed pad (EPAD).
4	PVDD_0		Supply of low-side gate driver of DC-DC converter bank 1. Connect to V_{DDD}. Use 1 µF and 0.1 µF bypass capacitors as close to the WLC1515 IC as possible.
5	LG2_0		Boost low-side gate driver output of DC-DC bank 1. Connect to the boost (output) side control (low-side) FET gate. Use a wide trace to minimize inductance of this connection.
6	VBB_0		Input rail of inverter bridge, connected to output of the buckboost converter. Connect this to the buckboost side terminal of current sense resistor for inverter bridge input current sensing. Use a dedicated (Kelvin) trace for this connection.
7	SW2_0		Negative power rail of DC-DC converter bank 1's boost high-side gate driver. This is also connected to one input terminal of RCP of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
8	HG2_0		Boost high-side gate driver output of DC-DC converter bank 1. Connect to the boost (output) side sync (high-side) FET gate. Use a wide trace to minimize inductance of this connection.
9	BST2_0		Boosted power supply of DC-DC bank 1's boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from V_{DDD} to BST2_0. Also, connect a bootstrap capacitor from this pin to SW2_0.
10	COMP		Error amplifier (EA) output for buckboost controller. Connect the RC compensation network to GND.
11	CSPO		Positive input of current sensing amplifier (CSA) of inverter bridge input current. Connect to positive terminal of the output current sense resistor (VBB_0).
12	CSNO		Negative input of current sensing amplifier of inverter bridge input current. Connect to negative terminal of the current sense resistor.
13	VBRG		Feedback pin for buckboost output voltage. Connect it to buckboost output before inverter bridge input current sense resistor.
14	VBRG_DIS		Inverter input power supply voltage. Connect to buckboost output before inverter bridge input current sense resistor. Used as weak discharge of VBRG.
15	LED_1		LED1 for 15W MP-A13 application/configurable GPIO. Float this pin if it is not used.
16	LED_2		LED2 for 15W MP-A13 application/configurable GPIO. Float this pin if it is not used.
17	NFET_CTRL_0		NFET gate driver output. Float this pin if it is not used.

Table 1 WLC1515 pinouts *(continued)*

Pin#	WLC1515		Description
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter	
18	ASK_OUT		ASK voltage/current sensing path. IC output for ASK signal processing.
19	ASK_DEMOD		Input for ASK signal decoding. Connect external ASK comparator output to this pin. Short this pin to pin-36 (ASK_SEL).
20	GD_OVR_HB_1	PWM_IN1	Inverter gate driver input signal for inverter bank 1. Short this pin to pin-22. PWM_OUT.
21	GD_OVR_HB_2	PWM_IN2	Inverter gate driver input signal for inverter bank 2. Short this pin to pin-22 PWM_OUT.
22	PWM_OUT		Inverter PWM signal output used for the inverter gate drive inputs. Short this pin to pin 20 (PWM_IN1) and pin 21 (PWN_IN2).
23	GPIO1	COIL1_EN	Default Coil1_EN / configurable GPIO.
24	GPIO2	COIL2_EN	Default Coil2_EN / configurable GPIO.
25	VDDD		V_{DDD} 5V LDO output from V_{IN}. Connect a ceramic bypass capacitor (recommended value 1µF) from this pin to GND close to the IC. Connect all V_{DDD} pins together.
26	GPIO3	COIL3_EN	Default Coil3_EN / configurable GPIO.
27	GPIO4	LIN_EN	Configurable GPIO / LIN transceiver enable. Float this pin if it is not used.
28	XRES		External reset – active low, internally pulled-up (~6kΩ). Float this pin if it is not used.
29	GPIO5	SWD_DAT/LIN_TX	Used for I^2C/SWD register access or programming/LIN transceiver Tx / configurable GPIO.
30	GPIO6	SWD_CLK/LIN_RX	Used for I^2C/SCL register access or programming/LIN transceiver Rx / configurable GPIO.
31	GPIO7	UART_TX	Default UART Tx for debug/configurable GPIO. Float this pin if it is not used.
32	Q_COMP_2		Q-factor based foreign object detection (FOD) pre-charge measurement input for frequency counting. Short this pin to pin 37 (QCOMP1).
33	GPIO8	TEMP_FB_1	Tx coil 1 temperature measurement via thermistor monitoring for 15W MP-A13 application/configurable GPIO. Float this pin if it is not used.
34	GND		Ground. Connect directly to the EPAD and to ground plane
35	NFET_CTRL_1	NC	NFET gate driver output. Float this pin if it is not used.
36	ASK_SEL		Input for ASK signal decoding. Short this pin to pin-19 (ASK_DEMOD).
37	QCOMP_1		Q-factor based FOD pre-charge measurement input for peak voltage detect. Short this pin to pin 32 (QCOMP2).
38	BB_IN		Input voltage to buckboost (DC-DC) controller. Connect to connector's positive pin. If EMI filter/choke is used after connector then connect it to output of the EMI filter/choke.
39	VBUS_IN		Input of feedback voltage of error amplifier of DC-DC bank 1 Connect to the connector positive node between the output current sense resistor and the VBUS provider NFET.
40	ASK_N		Negative input of ASK voltage sensing signal input to internal amplifier.
41	ASK_P		Positive input of ASK voltage sensing signal input to internal amplifier.
42	ASK_TST		ASK voltage sensing comparator output. Float this pin if it is not used.

Table 1 WLC1515 pinouts *(continued)*

Pin#	WLC1515		Description
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter	
43	BST2_1		Bootstrap power supply for (inverter bank 2) inverter high-side gate driver. Connect a capacitor (recommended value 0.1µF) from this pin to SW2_1. Also, connect a Schottky diode from VDDD to BST2_1.
44	HG2_1		High-side gate driver for inverter FET (inverter bank 2). Connect to the Inverter bank 2, high-side FET gate. Use a wide trace to minimize inductance of this connection.
45	SW2_1		Inverter switching node for inverter bank 2. Connect this pin to the inverter bank 2 switching node with a short and wide trace.
46	VBB_1		Inverter input voltage sense. Connect to inverter input voltage, after the current sense resistor. Use a dedicated (Kelvin) trace for this connection.
47	LG2_1		Low-side gate driver for inverter FET (inverter bank 2). Connect to the inverter bank 2 low side FET gate.
48	PVDD_1		Connect to VDDD pin. Connect bypass capacitors (recommended values 1µF and 0.1µF) as close to the IC as possible.
49	PGND_1		Ground for inverter gate driver. Connect directly to PCB ground plane and EPAD. Connect all GND and PGND pins together.
50	LG1_1		Low-side gate driver for inverter FET (inverter bank 1). Connect to the inverter bank 1 Low side FET gate.
51	SW1_1		Inverter switching node for inverter bank 1. Connect this pin to the Inverter bank 1 switching node with a short and wide trace.
52	HG1_1		High-side gate driver for inverter FET (inverter bank 1). Connect to the inverter bank 1 high side FET gate.
53	BST1_1		Bootstrap power supply for (inverter bank 1) inverter high-side gate driver. Connect a capacitor (recommended values 0.1µF) from this pin to SW1_1. Also, connect a Schottky diode from VDDD to BST1_1.
54	CSNI_1	DNU1	Negative input of input current sense amplifier for inverter. Float this pin if it is not used.
55	CSPI_1	DNU2	Positive input of input current sense amplifier for inverter. Float this pin if it is not used.
56	GPIO9	SDA_SEC / SPI_MISO	Used for interfacing as Master, with OPTIGA™ Trust I^2C SDA or With OPTIGA™ Trust SPI MISO. The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
57	GPIO10	SCL_SEC /SPI_CLK	Used for interfacing with OPTIGA™ Trust I^2C SCL or With OPTIGA™ Trust SPI CLK. The pin is configured for open drain connection, connect an external pull-up resistor. Float this pin if it is not used.
58	GPIO11	RES_SEC/SPI_MOSI	RESET for OPTIGA™ Trust IC (I2C Version) / MOSI for OPTIGA™ Trust IC Chip select for OPTIGA™ TRUST IC(SPI Version)/ Configurable GPIO.
59	GPIO12	SPI_SS	Configured for using OPTIGA™ Trust in low power mode. Configurable GPIO.
60	GPIO13	TEMP_FB_2/CLK_IN	Tx coil 2 temperature measurement via thermistor monitoring for 15W MP-A13 application/External Clock / configurable GPIO. Float this pin if it is not used.
61	VIN		4.5V–24V input supply. Connect a decoupling capacitor (recommended value 0.1µF) from this pin to GND close to this pin.
62	VCCD		1.8V LDO output for Arm®-M0 power and 1.8V references. Connect a decoupling capacitor (recommended value 0.1µF) from this pin to ground. Not for external use or loading.
63	VDDD		VDDD 5V LDO output from VIN. Connect a ceramic bypass capacitor (recommended value 1µF) from this pin to GND close to the IC. Connect all VDDD pins together.

Table 1 WLC1515 pinouts *(continued)*

Pin#	WLC1515		Description
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter	
64	GND		Ground. Connect directly to the EPAD and to ground plane.
65	CSPI_0		Positive input of input current sense amplifier (DC-DC). Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
66	CSNI_0		Negative input of input current sense amplifier t (DC-DC). Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
67	BST1_0		Bootstrap power supply for buck (DC-DC) high side gate driver. Connect a capacitor (recommended value 0.1µF) from this pin to SW1_0. Also, connect a Schottky diode from VDDD to BST1_0.
68	HG1_0		High-side gate driver output of buck converter (DC-DC bank 1). Connect to the buck high-side FET gate. Use a wide trace to minimize inductance of this connection.
69	EPAD		Exposed ground pad. Connect directly to ground plane and pins 34 and 64.

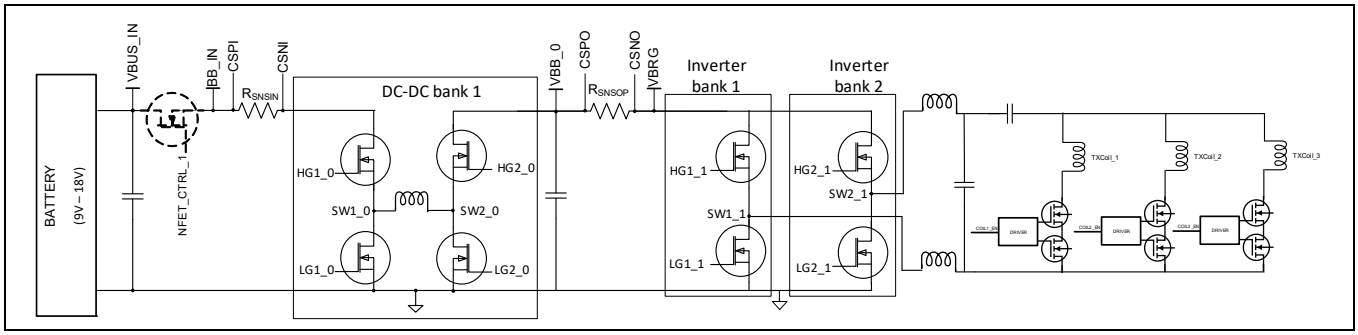


Figure 2 WLC1515 key pin mapping with buckboost and inverter power supplies[2]

Note

2. Refer **Figure 2** for an overview of key WLC1515 pin mapping to power input, current sense and gate drivers of buckboost and inverter power supplies.

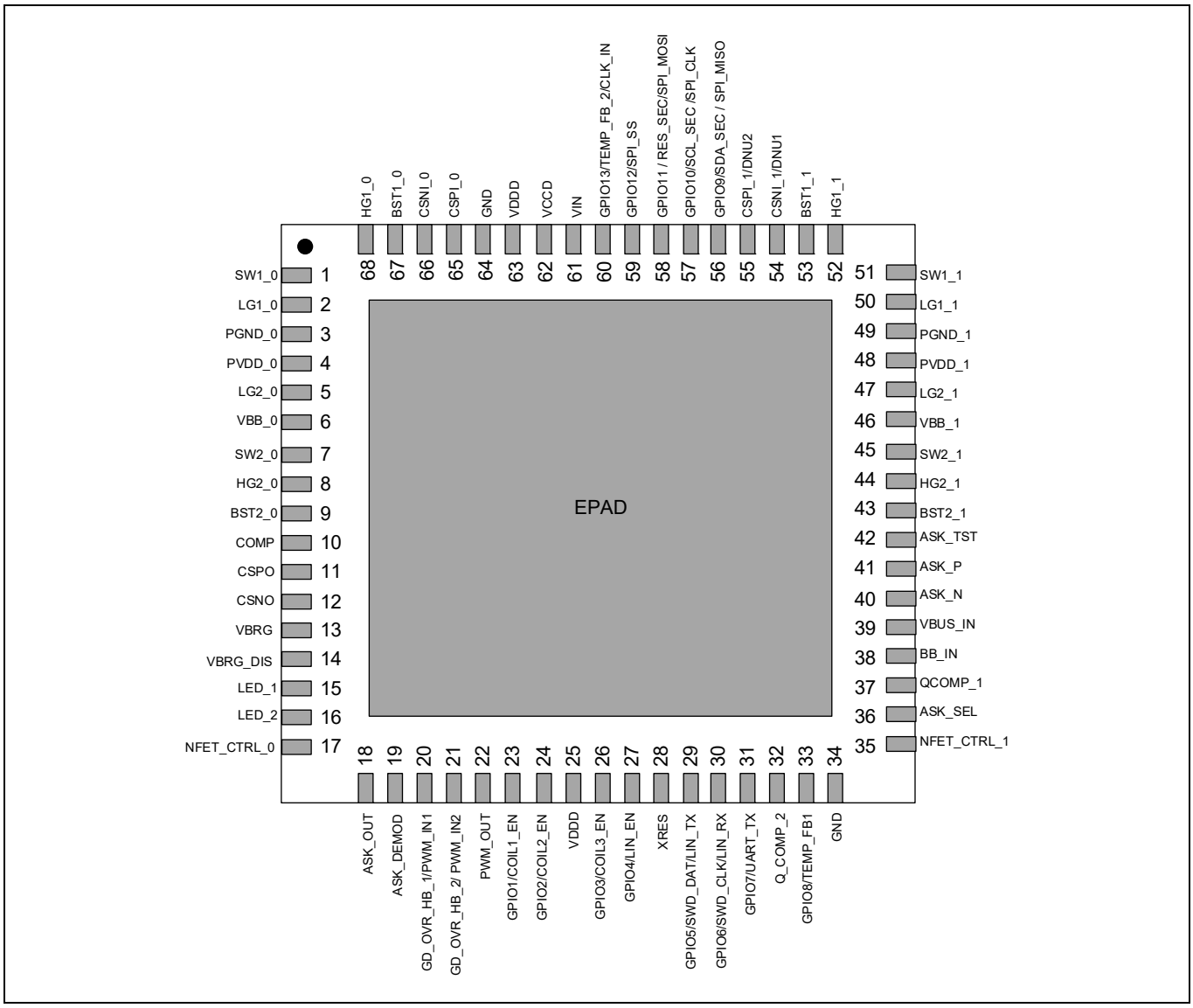


Figure 3 WLC1515-68LDXS pinout

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[3]

Exceeding maximum ratings may shorten the useful life of the device.

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Parameter	Description	Min	Typ	Max	Unit	Description
VIN	Maximum input supply voltage	–	–	40	V	–
VDDD, PVDD	Maximum supply voltage relative to VSS			6		
VBUS	Maximum VBRG_DIS voltage relative to VSS			24		
LED_X, ASK_SEL	Maximum voltage on LED_X and ASK_SEL pins			24		
QCOMP1	Maximum voltage on QCOMP1 pins	–0.7		24		Current limited to 1mA for -0.7V minimum specification.
QCOMP2	Input to QCOMP2	–0.7		VDDD + 0.5		
GPIO	Inputs to GPIO	–0.5		VDDD + 0.5		–
IGPIO	Maximum current per GPIO	–25		25	mA	
IGPIO_INJECTION	GPIO injection current, Max for VIH > VDDD, and Min for VIL < VSS	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge (ESD) human body model (HBM)	2000		–	V	Applicable for all pins except LED_1, LED_2, ASK_SEL, QCOMP1 pins.
ESD_HBM_LED_X	ESD HBM for LED_1 and LED_2 pins for both ports	1100				Only applicable to LED_1, LED_2, ASK_SEL, QCOMP1 pins
ESD_CDM	ESD charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
TJ	Junction temperature	–40		125	°C	

Note

3. Usage above the absolute maximum conditions listed in **Table 2** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3 Pin based absolute maximum ratings

Pin#	WLC1515		Absolute minimum (V)	Absolute maximum (V)
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter		
1	SW1_0		-0.7	35
2	LG1_0[5]		-0.5	PVDD+0.5
3	PGND_0		-0.3	0.3
4	PVDD_0			VDD
5	LG2_0[5]		-0.5	PVDD+0.5
6	VBB_0		-0.3	24
7	SW2_0			
8	HG2_0 (w.r.t SW2_0)[4, 5]		-0.5	PVDD+0.5
9	BST2_0 (w.r.t SW2_0)[4, 5, 6]		0	
10	COMP[5]		-0.5	
11	CSPO		-0.3	24
12	CSNO			
13	VBRG			
14	VBRG_DIS			
15	LED_1		-0.5	
16	LED_2			
17	NFET_CTRL_0			32
18	ASK_OUT[4]			PVDD+0.5
19	ASK_DEMOD[4]			
20	GD_OVR_HB_1[4]	PWM_IN1		
21	GD_OVR_HB_2 [4]	PWM_IN2		
22	PWM_OUT[4]			
23	GPIO1[4]	COIL1_EN		
24	GPIO2[4]	COIL2_EN		
25, 63	VDDD		-0.3	6
26	GPIO3[4]	COIL3_EN	-0.5	PVDD+0.5
27	GPIO4[4]	LIN_EN		
28	XRES[4]			
29	GPIO5[4]	SWD_DAT/LIN_TX		
30	GPIO6[4]	SWD_CLK/LIN_RX		
31	GPIO7[4]	UART_TX		
32	Q_COMP_2[4, 7]		-0.7	
33	GPIO8[4]	TEMP_FB_1	-0.5	
34,64	GND		-0.3	0.3
35	NFET_CTRL_1	NC	-0.5	32

Notes
4. Maximum voltage cannot exceed 6 V.
5. Maximum absolute voltage w.r.t GND must not exceed 40V.
6. Minimum absolute voltage w.r.t GND must not be lower than -0.3V.
7. Current limited to 1mA for -0.7V minimum specification only.

Table 3 Pin based absolute maximum ratings *(continued)*

Pin#	WLC1515		Absolute minimum (V)	Absolute maximum (V)
	Pin name	Example pin assignment for 15W 3-Coil MP-A13 transmitter		
36	ASK_SEL		-0.5	24
37	QCOMP_1[7]		-0.7	
38	BB_IN		-0.3	
39	VBUS_IN			
40	ASK_N			
41	ASK_P			
42	ASK_TST[4]		-0.5	PVDD+0.5
43	BST2_1 (w.r.t SW2_1)[4, 5, 6]		0	
44	HG2_1(w.r.t SW2_1)[4, 5]		-0.5	
45	SW2_1		-0.7	24
46	VBB_1		-0.3	
47	LG2_1[4]		-0.5	PVDD+0.5
48	PVDD_1		-0.3	VDDD
49	PGND_1			0.3
50	LG1_1[4]		-0.5	PVDD+0.5
51	SW1_1		-0.7	35
52	HG1_1 (w.r.t SW1_1)[4, 5]		-0.5	PVDD+0.5
53	BST1_1(w.r.t SW1_1)[4, 5, 6]		0	
54	CSNI_1	DNU1	-0.3	40
55	CSPI_1	DNU2		
56	GPIO9[4]	SDA_SEC / SPI_MISO	-0.5	PVDD+0.5
57	GPIO10[4]	SCL_SEC /SPI_CLK		
58	GPIO11[4]	RES_SEC/SPI_MOSI		
59	GPIO12[4]	SPI_SS		
60	GPIO13[4]	TEMP_FB_2 / CLK_IN		
61	VIN		-0.3	40
62	VCCD			2
65	CSPI_0			40
66	CSNI_0			
67	BST1_0(w.r.t SW1_0)[4, 5, 6]		0	PVDD+0.5
68	HG1_0(w.r.t SW1_0)[4, 5]		-0.5	
69	EPAD		-0.3	0.3

Notes
4. Maximum voltage cannot exceed 6 V.
5. Maximum absolute voltage w.r.t GND must not exceed 40V.
6. Minimum absolute voltage w.r.t GND must not be lower than -0.3V.
7. Current limited to 1mA for -0.7V minimum specification only.

3.2 Device-level specifications

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

3.3 DC specifications

Table 4 DC specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	VIN	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	VIN_BB	Buckboost operating input supply voltage	5.5		24		
SID.PWR#2	VDDD_REG	VDDD output with VIN 5.5 to 24V, Max load = 150mA	4.6		5.5		
SID.PWR#3	VDDD_MIN	VDDD output with VIN 4V to 5.5V, Maximum load = 20mA	V_{IN} – 0.2		–		
SID.PWR#20	VBRG	VBRG valid range	3.3		21.5		
SID.PWR#5	VCCD	Regulated output voltage (for Core Logic)	–	1.8	–		
SID.PWR#16	CEFC_VCCD	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic or greater
SID.PWR#17	CEXC_VDDD	Power supply decoupling capacitor for VDDD	–	10	–	µF	
SID.PWR#18	CEXV	Bootstrap supply capacitor (BST1_0, BST1_1, BST2_0, BST2_1)		0.1			
SID.PWR#24	IDD_ACT	Supply current at 0.4MHz switching frequency		85		mA	T_A = 25°C, V_{IN} = 12V. CC IO IN Transmit or Receive, no I/O sourcing current, no VBRG load current, CPU at 24MHz, two PD ports active. buckboost converter ON, 3-nF gate driver capacitance.

3.3.1 CPU

Table 5 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	FCPU	CPU input frequency	–	–	48	MHz	–40°C ≤ T_A ≤ +105°C, All VDDD
SID.PWR#19	TDEEPSLEEP	Wakeup from Deep Sleep mode		35	–	µs	–
SYS.XRES#5	TXRES	External reset pulse width	5	–			
SYS.FES#1	T_PWR_RDY	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

3.3.2 GPIO

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 6 GPIO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	VIH_CMOS	Input voltage HIGH threshold	0.7 × VDDD	–	–	V	CMOS input
SID.GIO#10	VIL_CMOS	Input voltage LOW threshold	–		0.3 × VDDD		
SID.GIO#7	VOH	Output voltage HIGH level	VDDD – 0.6		–		IOH = –4 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#8	VOL	Output voltage LOW level	–		0.6		IOL = 10 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–40°C ≤ TA ≤ +105°C
SID.GIO#3	Rpd	Pull-down resistor when enabled					
SID.GIO#4	IIL	Input leakage current (absolute value)	–	–	2	nA	+25°C TA, 3-V VDDD
SID.GIO#5	CPIN_A	Maximum pin capacitance			22	pF	–40°C ≤ TA ≤ +105°C, Capacitance on DP, DM pins
SID.GIO#6	CPIN	Maximum pin capacitance		3	7		–40°C ≤ TA ≤ +105°C, All VDDD, All other I/Os
SID.GIO#11	VIHTTL	LVTTL input	2	–	–	V	–40°C ≤ TA ≤ +105°C
SID.GIO#12	VILTTL		–		0.8		
SID.GIO#13	VHYSTTL	Input hysteresis, LVTTL, VDDD > 2.7 V	100	–	–	mV	VDDD > 2.7 V
SID.GIO#14	VHYSCMOS	Input hysteresis CMOS	0.1 × VDDD				–
GPIO AC specifications							
SID.GIO#16	TRISEF	Rise time in Fast Strong mode	2	–	12	ns	Cload = 25 pF, –40°C ≤ T_A ≤ +105°C
SID.GIO#17	TFALLF	Fall time in Fast Strong mode					
SID.GIO#18	TRISES	Rise time in Slow Strong mode	10		60		
SID.GIO#19	TFALLS	Fall time in Slow Strong mode					
SID.GIO#20	F_{GPIO_OUT1}	GPIO FOUT; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO FOUT; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Slow Strong mode.	–	–	7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ V_{DDD} ≤ 5.5 V.			16		–40°C ≤ T_A ≤ +105°C
GPIO OVT DC specifications							
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply

Table 6 GPIO specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5	–	8.5	kΩ	–40°C ≤ T_A ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value					
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C T_A, 3-V VDDD
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ T_A ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO #33	GPIO_20VT_Voh	GPIO_20VT output voltage high level.	VDDD – 0.6		–	V	IOH = -4 mA
SID.GPIO_20VT_GIO #36	GPIO_20VT_Vol	GPIO_20VT output voltage low level.	–		0.6		IOL = 8 mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ TA ≤ +105°C, All VDDD
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LVTTL		–		0.8		
SID.GPIO_20VT_GIO #43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100		–	mV	
SID.GPIO_20VT_GIO #45	GPIO_20VT_I-TOT_GPIO	GPIO_20VT maximum total sink pin current to ground	–		95	mA	V(GPIO_20VT pin) > VDDD
GPIO OVT AC specifications							
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in Fast Strong mode	1	–	15	ns	All VDDD, Cload = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in Fast Strong mode					
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in Slow Strong mode	10		70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT fall time in Slow Strong mode					
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–	–	33	MHz	
SID.GPIO_20VT_GIO# 50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V ≤ VDDD ≤ 5.5V. Slow Strong mode.			7		
SID.GPIO_20VT_GIO# 52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V			8		All VDDD

3.3.3 XRES and POR

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 7 XRES specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
XRES DC specifications							
SID.XRES#1	VIH_XRES	Input voltage HIGH threshold on XRES pin	0.7 × VDDD	–	–	V	CMOS input
SID.XRES#2	VIL_XRES	Input voltage LOW threshold on XRES pin	–		0.3 × VDDD		
SID.XRES#3	CIN_XRES	Input capacitance on XRES pin			7	pF	–
SID.XRES#4	VHYSXRES	Input voltage hysteresis on XRES pin		0.05 × V_{DDD}	–	mV	
Imprecise POR (IPOR) specifications							
SID185	VRISEIPOR	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–40°C <T_A < +105°C, All V_{DDD}
SID186	VFALLIPOR	POR falling trip voltage	0.70		1.4		
Precise POR (POR) specifications							
SID190	VFALLPPOR	Brown-out detect (BOD) trip voltage in Active/Sleep modes	1.48	–	1.62	V	–40°C < T_A < +105°C, All VDDD
SID192	VFALLDPSLP	BOD trip voltage in Deep Sleep mode	1.1		1.5		

3.4 Digital peripherals

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted. The following specifications apply to the Timer/counter/PWM peripherals in the Timer mode.

3.4.1 Inverter pulse-width modulation (PWM) for GPIO pins

Table 8 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.TCPWM.1	PWM_OUT	Operating frequency	85	127.7	600	kHz	PWM_OUT pin
SID.TCPWM.3	TPWMEXT	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.4	TCRES	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5	PWMRES	PWM resolution					Minimum pulse width of PWM output

3.4.2 I²C, UART, SWD interface, SPI, and LIN

Table 9 Communication interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
Fixed I2 C AC specifications							
SID153	FI2C1	Bit rate	–	–	1	Mbps	–
Fixed UART AC specifications							
SID16	FUART	Bit rate	–	–	1	Mbps	–
SWD interface specifications							
SID.SWD#1	F_SWDCLK1	3.0V ≤ V_{DDIO} ≤ 5.5V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	
SID.SWD#3	T_SWDI_HOLD				–		
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		
Fixed SPI AC specifications							
SID166	FSPI	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–
Fixed SPI Master mode AC specifications							
SID167	TDMO	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO valid before SClock capturing edge	20		–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0				Referred to slave capturing edge
Fixed SPI Slave mode AC specifications							
SID170	TDMI	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after Sclock driving edge	–		48 + (3 × TCPU)		TCPU = 1/FCPU
SID171A	TDSO_EXT	MISO valid after Sclock driving edge in Ext Clk mode					–
SID172	THSO	Previous MISO data hold time	0		–		
SID172A	TSSELSCK	SSEL valid to first SCK Valid edge	100				

3.4.3 Memory

Table 10 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (erase and program)	–	–	20	ms	–40°C ≤ TA ≤ +85°C, All V_{DDD}
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_ PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32KB)			35		
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	$FLASH_{ENPB}$	Flash write endurance	100k		–	cycles	25°C < T_A < 55°C, All V_{DDD}
SID182	F_{RET1}	Flash retention, T_A < 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A < 85°C, 10K P/E cycles	10				

3.5 System resources

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

3.5.1 Internal main oscillator clock

Table 11 IMO, ILO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
IMO AC specifications							
SID.CLK#13	FIMOTOL	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	3.0 V < VDDD < 5.5 V. –40°C < TA < 105°C
SID226	TSTARTIMO	IMO start-up time			7	µs	–40°C < TA < +105°C, All VDDD
SID.CLK#1	FIMO	IMO frequency	24		48	MHz	
ILO AC specifications							
SID234	TSTARTILO1	ILO start-up time	–	–	2	ms	–40°C < TA < +105°C, All VDDD
SID238	TILODUTY	ILO duty cycle	40	50	60	%	
SID.CLK#5	FILO	ILO frequency	20	40	80	kHz	–

3.5.2 ADC

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 12 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	-1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	-2.5		2.5		Reference voltage generated from VDDD
SID.ADC.4	Gain Error	Gain error	-1.5		1.5		Reference voltage generated from bandgap
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}		V_{DDDmax}	V	Reference voltage generated from VDDD
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from Deep Sleep reference

3.5.3 Current sense amplifier (CSA) / ASK amplifier (ASK_P and ASK_N)

Table 13 CSA/ASK amplifier specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
HS CSA DC specifications							
SID.HSCSA.7	Csa_SCP_Acc1	CSA short circuit protection (SCP) at 6A with 5/10/20mΩ sense resistor	-10	–	10	%	Active mode
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10A with 5/10/20mΩ sense resistor	-10		10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1A with 5/10/20mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5/10/20mΩ sense resistor	123	130	137		
SID.HSCSA.13	Csa_CBL_MON_Acc2	Vsense > 10mV	–	±3.5	–		CSA sense accuracy. Active mode. 3.0V < V_{DDD} < 5.5V. T_A = 25°C.
CSA AC specifications							
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3nF NFET gate

3.5.4 VIN UV/OV

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 14 VIN UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold accuracy, 4V-11V	-3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold accuracy, 11V-21.5V	-3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold accuracy, 3V-3.3V	-4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold accuracy, 3.3V-4.0V	-3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold accuracy, 4.0V-21.5V	-3		3		

3.5.5 Voltage regulation - VBRG

Table 15 VBRG specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
VBRG discharge specifications							
SID.VBUS.DISC.1	R_DIS1	20V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5V
SID. VBUS.DISC.2	R_DIS 2	20V NMOS ON resistance for DS = 2	250		1000		
SID. VBUS.DISC.3	R_DIS 4	20V NMOS ON resistance for DS = 4	125		500		
SID. VBUS.DISC.4	R_DIS 8	20V NMOS ON resistance for DS = 8	62.5		250		
SID. VBUS DISC.5	R_DIS 16	20V NMOS ON resistance for DS = 16	31.25		125		
SID. VBUS.DISC.6	VBRG_stop_error	Error percentage of final V_{BRG} value from setting	–		10	%	When V_{BRG} is discharged to 5V
Voltage regulation DC specifications							
SID.DC.VR.1	VBB	VBB output voltage range	3.0	–	22	V	–
SID.DC.VR.2	VR	VBB voltage regulation accuracy	-5	±3	+5	%	
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	
SID.VREG.1	TSTART	Total startup time for the regulator supply outputs	–		200	µs	Specification for VDDD LDO

3.5.6 NFET gate driver specifications

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 16 NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
NFET gate driver DC specifications							
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on NFET_CTRL to turn off external NFET.
NFET gate driver AC specifications							
SID.GD.3	T_{ON}	NFET_CTRL Low to High (1V to VBUS + 1V) with 3nF external capacitance.	2	5	10	ms	VBRG = 5V
SID.GD.4	T_{OFF}	NFET_CTRL High to Low (90% to 10%) with 3nF external capacitance.	–	7	–	µs	VBRG = 21.5V

3.5.7 BuckBoost PWM controller

Table 17 BuckBoost PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
PWM controller specifications							
PWM.1	FSW	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	
PWM.3	Ratio_Buck_BB	Buck to buckboost ratio		1.16		–	
PWM.4	Ratio_Boost_BB	Boost to buckboost ratio		0.84			
GD1	Fsw Gd Ovr	Inverter switching frequency	85		600	kHz	Pins PWM_IN1 and PWM_IN2 are connected to pin PWM_OUT.
BuckBoost controller gate driver specifications							
DR.1	R_HS_PU	Top-side gate driver on-resistance - gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance - gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance - gate pull-up		2			

Table 17 BuckBoost PWM controller specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DR.4	R_LS_PD	Bottom-side gate driver on-resistance - gate pull-down	–	1.5	–	Ω	–
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
DR.9	Tr_LS	Bottom-side gate driver rise time		25			
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

3.5.8 Thermal

All specifications are valid for –40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted.

Table 18 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

4 Functional overview

4.1 Wireless power transmitter

WLC1515 supports wireless power transfer between power transmitter (TX) and power receiver (RX), based on inductive power transfer technology (IPT). The Tx runs an alternating electrical current through the Tx coil(s) to generate an alternating magnetic field in accordance with Faraday's law. This magnetic field is mutually coupled to the Rx coil inside the power receiver and is transformed back into an alternating electrical current that is rectified and stored on a Vrect capacitor bank to power the Rx load.

Before the power transfer begins, the Rx and Tx communicate with each other to establish that a valid Rx device has been placed and they negotiate the level of power to be transferred during the charging cycle. The digital communication used by Tx and Rx is in-band communication. The communication from Tx to Rx is frequency shift key (FSK) modulation and from Rx to Tx is amplitude shift key (ASK) modulation. The WLC1515 solution supports the Qi v1.3.x standard up to 15W. The WLC1515 operates in both BPP or EPP depending on the capabilities of the Rx that gets placed by the user.

WLC1515 offers a highly integrated wireless power transmitter solution with the Qi v1.3.x standard. This includes ready to use firmware stack with a robust demodulation scheme for continuous power transfer and reliable FOD to ensure safety. WLC1515 firmware stack comes with a high level of configurable options to enable differentiation by application using the configuration utility tool.

4.2 WPC system control

WLC1515 controls the wireless power system as per the Qi standard version 1.3.x. The system control covers power transfer, system monitoring, and various phases of operation under BPP or EPP receivers depending on the Rx type placed onto the Tx pad.

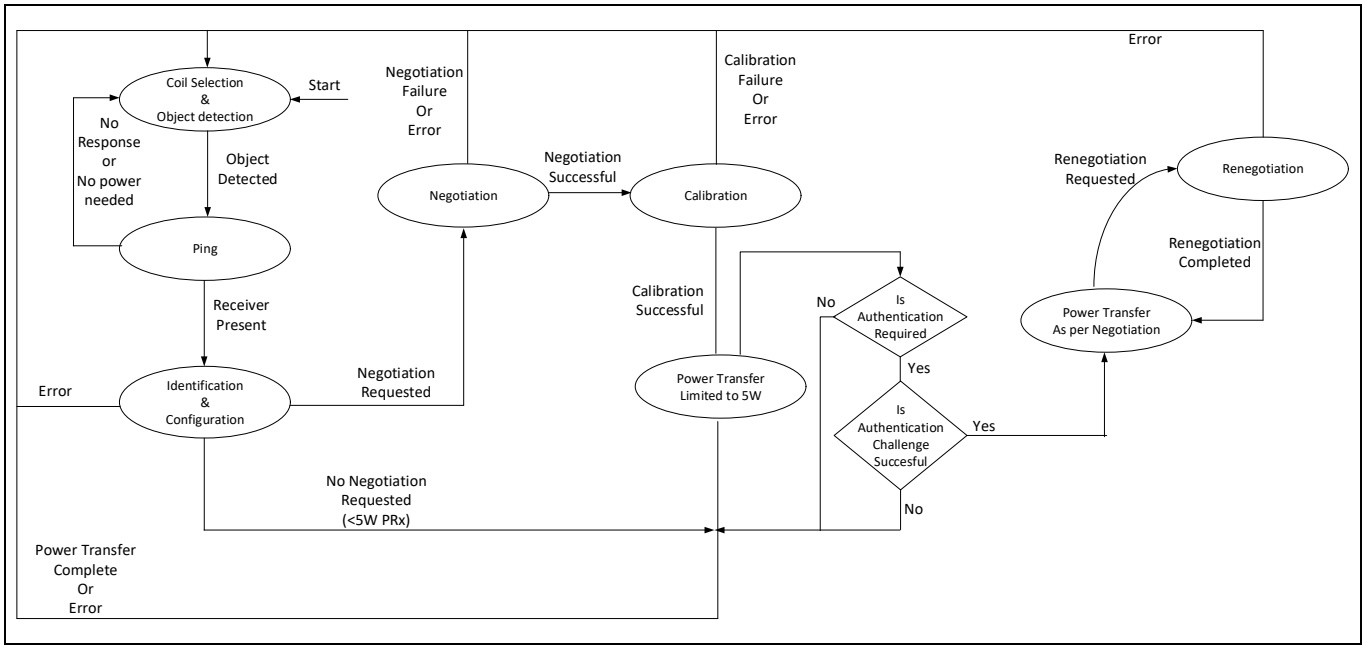


Figure 4 WPC system control flow chart (negotiation, calibration and authentication are for EPP only)[8]

Note

8. The **Functional overview** section only describes the Qi specification. However, IC can support wireless charging proprietary power delivery extensions Samsung FC (PPDE).

4.2.1 Coil selection and object detection phase

The Tx monitors the interface surface using low energy signals (analog ping or Q-factor) to detect objects' placement and removal. The Analog Ping energy is limited such that impedance changes above the Tx coil may be detected without powering or waking up the receiver. The WLC1515 sets the Bridge (VBRG) voltage powering the inverter to a low voltage to generate sufficient energy to measure for any interface impedance changes without transferring any power during the selection phase. The WLC1515 switches the coil for every five analog pings.

4.2.2 Digital ping phase

In this phase, the Tx sends a power signal that is sufficient to power the receiver and prompt a response. This signal is called Digital Ping and the magnitude and length of time are predefined by the WPC Tx specifications. The Digital Ping phase ends when no response is detected or the Rx responds with a signal strength packet (SSP). When the Tx receives a valid SSP, the Digital Ping is extended and the system proceeds to the Identification and Configuration phase.

4.2.3 Identification and configuration phase

In this phase, the Tx identifies whether the Rx belongs to BPP or EPP profile. Additionally, in this phase, the Tx obtains configuration information such as the maximum amount of power that the Rx may require at its output. The power transmitter uses this information to create a Power Transfer Contract.

If the receiver is a BPP type then the power transmitter enters into the power transfer phase at the completion of the ID and Config phase as shown in **Figure 8** or with EPP receivers it proceeds to the negotiation phase if requested by the Rx.

4.2.4 Negotiation

In this phase, the EPP power receiver negotiates with the power transmitter to fine-tune the power transfer contract. For this purpose, the power receiver sends negotiation requests to the power transmitter, which the power transmitter can grant or deny.

In compliance with Q-factor FOD, the Tx will compare the Q-factor reported by the Rx with its own measurement to determine if the Q-factor of the coil is appropriate for the Rx that has been placed (EPP only). If the Tx Q-factor reading is too low it will flag a QFOD alarm and return to the selection phase.

4.2.5 Calibration

When this phase is requested, the Tx will ACK the request and commence with the EPP Rx to enable and enter the calibration phase to calibrate for transmitter power losses at two fixed receiver loads. This system's power loss information will be used by the Tx to detect the presence of foreign objects on the interface surface during the power delivery phase.

4.2.6 Authentication

Post successful calibration, Tx enters into power transfer mode limited to 5W. In this mode, Rx can request and challenge Tx for authentication. In case of successful authentication, Tx proceeds with negotiated power delivery. If authentication challenge is not successful then Tx continues to be in power transfer mode, limited to 5W. WLC1515 provides an I^2C/SPI port for interfacing with OPTGA™ Trust Charge IC to enable authentication.

4.2.7 Renegotiation phase

In this phase, the EPP Rx can request to adjust the power transfer contract. This phase may be aborted prematurely without changing the power transfer contract.

4.2.8 Power transfer phase

In this phase, the Tx transfers power to the Rx and the power level is determined by the control error packets (CEP) and limited by the guaranteed power contract. Power loss FOD is also enabled and utilized to prevent excessive power loss which could result in FO heating.

1. CEP: These packets are used by the Tx to adjust the amount of power being sent. The CEP may be positive, negative, or 0. The Tx adjusts its operating point based on the value of the CEP. The CEP packet must be received every 1.8s (configurable) or power will be withdrawn along with other constraints that specify when a CEP may be sent by the Rx as defined in the WPC specifications.
2. Received power packet (RPP): The packet (8 bits for BPP and 24 bits for EPP) contains power received by receiver. The RPP is used by the Tx to determine if the power loss is safe or excessive based on the FOD thresholds contained in the FW.
3. End power transmit (EPT): The Rx may send an EPT packet anytime to inform Tx to withdraw/terminate the power delivery. The Tx will end the power transfer immediately if an EPT packet is received.

The Rx and Tx communicate with each other by modulating the carrier wave used to transfer power. The following sections describe the communication layer used and defined by the WPC.

4.2.9 Bidirectional in-band communication interface

The Qi standard requires bi-directional in-band communication between Tx and Rx. The communication from Tx to Rx is FSK and is implemented by the Tx alternating the carrier wave frequency. The communication from Rx to Tx is ASK and is created by modulating the load on the Rx side causing a reflection to appear on the Tx which is filtered and decoded.

4.3 Communication from Tx to Rx - FSK

The power transmitter communicates to the power receiver using frequency shift keying, in which the power transmitter modulates the operating frequency of the power signal.

In FSK, the Tx changes its operating frequency between the current operating frequency (f_{OP}) to an alternate frequency (f_{MOD}) in the modulated state. The difference between these two frequencies is characterized by two parameters that are determined during the initial ID and config stage of the wireless power connection:

- Polarity: This parameter determines whether the difference between f_{MOD} and f_{OP} is positive or negative.
- Depth: This parameter determines the magnitude of the difference between f_{OP} and f_{MOD} in Hertz (Hz).

The Tx uses a differential bi-phase encoding scheme to modulate data bits to the carrier wave. For this purpose, the Tx aligns each data bit to segments of 512 cycles of the carrier wave frequency.

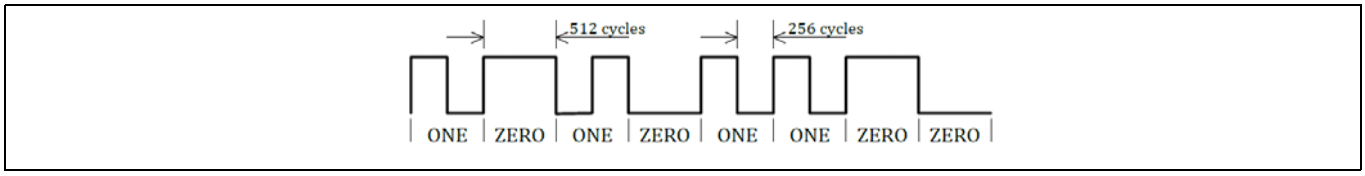


Figure 5 Example of differential bi-phase encoding - FSK

4.4 Communication from Rx to Tx - ASK

In the ASK communication scheme, the Rx modulates the amount of power that it draws from the Tx power signal. The Tx detects this through as a modulation of the Tx current and/or voltage and uses a demodulation scheme to convert the modulated signal into a binary signal.

The Rx shall use a differential bi-phase encoding scheme to modulate data bits onto the power signal. For this purpose, the power receiver shall align each data bit to a full period t_{CLK} of an internal clock signal, such that the start of a data bit coincides with the rising edge of the clock signal. This internal clock (INTCLK) signal shall have a frequency fCLK = 2kHz ±4%. tCLK is time period of the INTCLK clock.

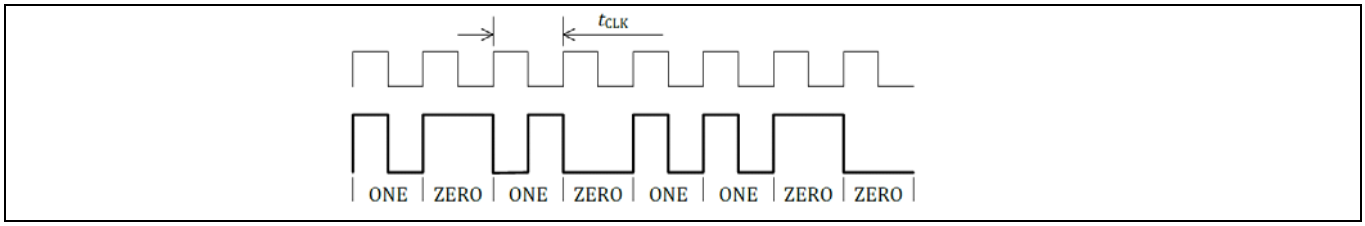


Figure 6 Example of differential bi-phase encoding - ASK

When the Tx receives a modulated signal from the Rx the information is decoded and the Tx will react to the packet according to the type and the WPC specification.

4.5 Demodulation

The WLC1515 ASK demodulating and decoding scheme works by detecting voltage and current variations in the Tx coil caused by the Rx modulation signal. The voltage path for ASK uses an external band pass filter to filter the demod signal out of the carrier wave. The current sense uses the bridge current sense resistor and an integrated differential amplifier to sense the ASK variations. Both ASK sensing paths can be multiplexed to the external Opamp filter and comparator to improve communication in low signal-to-noise environments or conditions.

Figure 7 shows the demodulation path used for current and voltage sensing of the modulation signal for packet decoding.

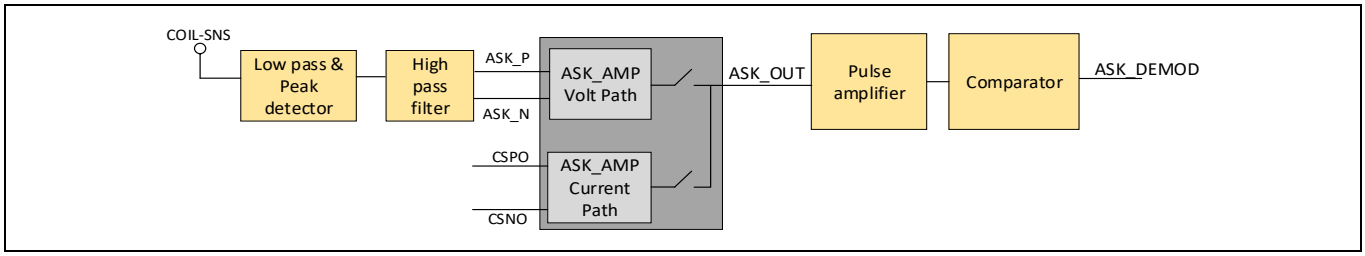


Figure 7 WLC1515 voltage and current demodulation path for ASK

4.6 Inverter

The WLC1515 uses the integrated buckboost controller to generate the bridge voltage used to power the full-bridge inverter that powers the Tx resonance tank to deliver power to the Rx. The inverter supports a wide input operating voltage range (3V to 22V) for power transfer. The integrated gate drivers of the WLC1515 are designed to control a full bridge or half-bridge Inverter depending on the WPC specification type and operating scenario. The inverter is capable of operating at switching frequencies between 85kHz and 600kHz but are typically limited to 110kHz to 148kHz. During the power transfer phase, the inverter responds to Rx CEP packets by adjusting the operating frequency or adjusting the bridge voltage. The power control method (variable voltage or variable frequency) is determined by the WPC specification but may be altered in order to promote better interoperability and user experience.

4.7 Rx detection

During the selection phase, the Tx will periodically poll the interface to detect impedance changes in order to quickly send a Digital Ping within 0.5s of a user placing an Rx. During this phase, the WLC1515 is able to distinguish between large ferrous objects (such as keys or coins) and regular Rx devices using Q factor, input current, or shifts in resonance frequency to attempt FOD before power transfer. In case of marginally high input current or resonance shifts, the Tx will commence to Digital Ping in order to guarantee a connection with a valid Rx is made in a timely manner. The typical sequence of operations used to scan the interface for Rx placement (or removal if an EPT is received during power transfer) is shown in **Figure 8**.

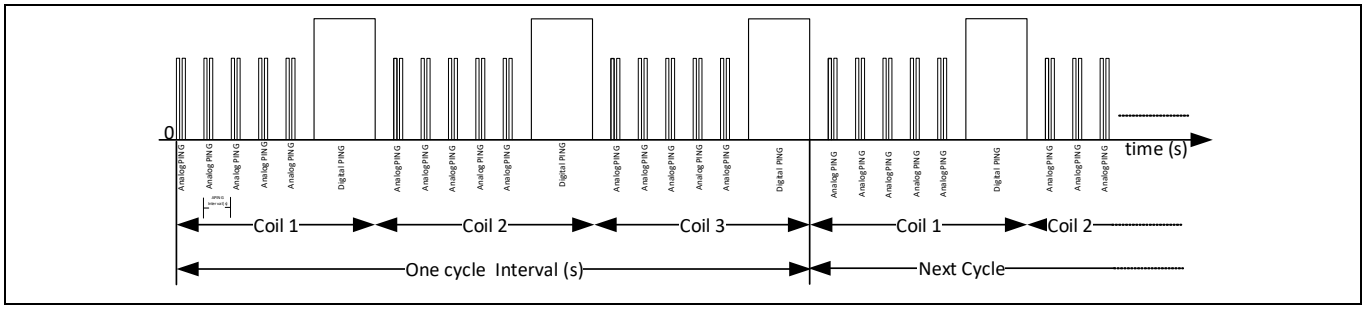


Figure 8 Typical selection phase Rx detection timing diagram

Figure 9 describes the process used during the selection phase for quick Rx detection and connection.

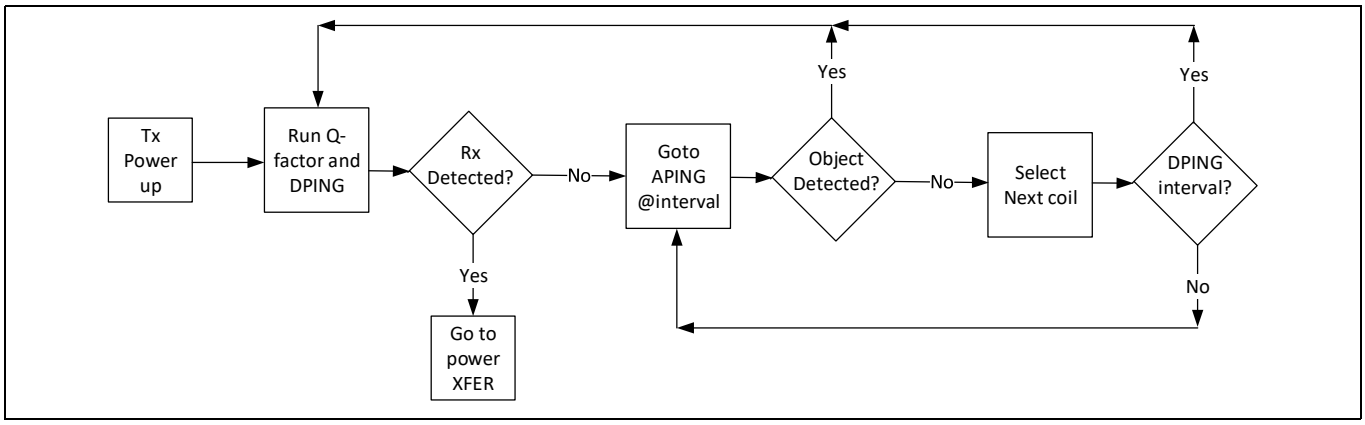


Figure 9 Typical selection phase flow chart for Rx detection and connection

The Rx detection in **Figure 9** also covers foreign object detection. The foreign object is identified by using Q factor. In case of foreign object detection, the process flow proceeds to analog ping (APNG). Further details about foreign object detection is covered in **Foreign object detection (FOD)**.

4.7.1 Foreign object detection (FOD)

WLC1515 supports enhanced FOD as per Qi v1.3.x standard. This includes FOD based on Q factor, resonance frequency, power loss, and over temperature (if a thermistor is used).

4.7.2 Q factor FOD and resonance frequency FOD

WLC1515 offers integrated Q factor and resonance frequency measurements for QFOD pre-power delivery. The measurements are made using the internal comparators QCOMP1 and QCOMP2 and the simple external components to charge the resonance capacitor and then discharge by shorting the LC tank and observing the resulting oscillation and voltage decay. The measurement of the Q factor is performed directly before every digital ping. The number of cycle count 'N' between two coil voltages V1 and V2 and period between corresponding rising edge pulses are used for Q factor and resonance frequency measurement as shown in **Figure 10**.

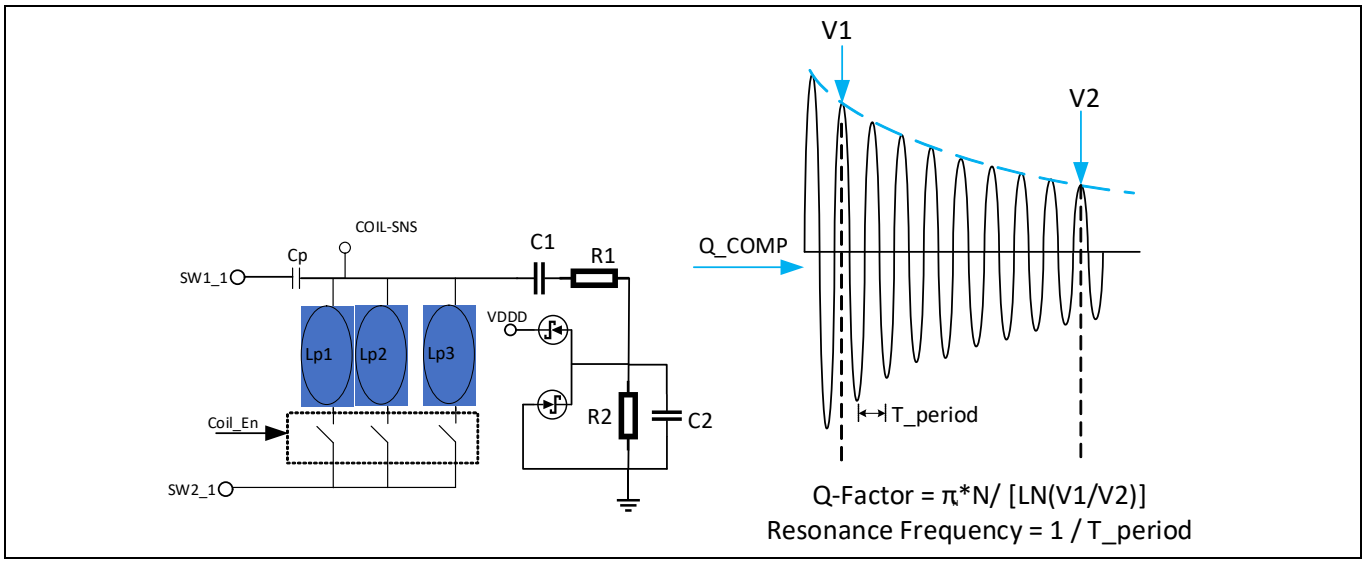


Figure 10 WLC1515 Q factor measurement schematic and signal

4.7.3 Power loss FOD

WLC1515 supports power loss FOD during power transfer. The power loss FOD uses the Tx power measured at the buck output and is the product of the bridge voltage and the bridge current (current is sensed at inputs CSPO_0 and CSNO_0). This result for Tx power is further adjusted by tuning FOD coefficients to account for inverter losses and friendly metal losses. After computing the calibrated Tx power the result is compared against the latest RPP value sent by the Rx. If the difference between Tx_Power_Calibrated and RPP exceeds the Ploss threshold then an FOD event is logged. To prevent erroneous disconnects and improve user experience the WLC1515 will only disconnect the power for Ploss FOD in the event that three consecutive Ploss threshold breaches occur. The FOD coefficients and the Ploss thresholds are configurable to adapt to the system design.

4.7.4 Over temperature FOD

The WLC1515 is able to monitor interface temperature if an external NTC thermistor is connected and placed in contact with the Tx coil. This can be enabled to disconnect the Tx from the Rx in the event that the Tx coil temperature exceeds a configurable threshold.

4.8 BuckBoost regulator

The WLC1515 buckboost regulator can be configured to operate in buckboost mode, buck-only mode, or boost-only mode. While the buckboost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. The buckboost regulator powers the inverter at the input node, VBRG, to enable power transfer per Qi. The WLC1515buckboost regulator requires input and output bypass capacitors as well as four FETs and an inductor. The necessary external components and connections are shown in **Figure 11**. The buckboost also offers current protection using a cycle-by-cycle current sense amplifier connected across resistance CSR, integrated high and low side gate drivers, and automatic PWM generation for output voltage control. The effective capacitance and inductor have been deliberately selected to optimize buckboost performance and any substitutions should be made using equivalent components as those found in the reference schematic and using hardware design guidelines.

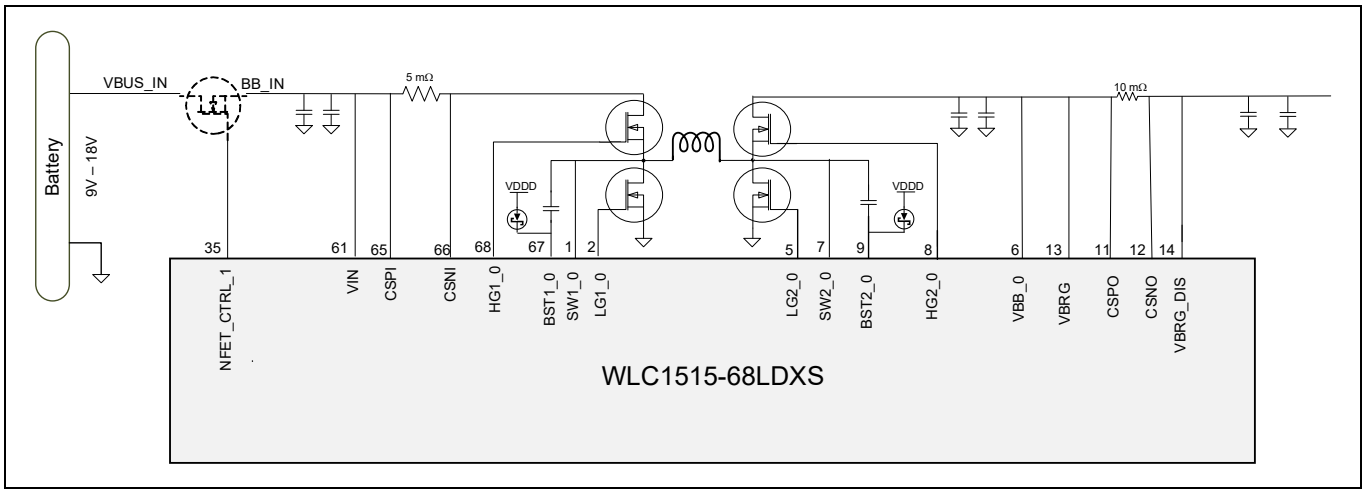


Figure 11 WLC1515 typical buckboost regulator schematic for VBRG generation

4.9 BuckBoost operating modes

4.9.1 BuckBoost converter

4.9.1.1 BuckBoost controller operation regions

The input-side CSA's output is compared with the output of the error amplifier to determine the pulse width of the PWM. The PWM block compares the input voltage and output voltage to determine the buck, boost, and buckboost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VBUS vs VBRG thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

4.9.1.1.1 Buck region operation (VBUS >> VBRG)

When the VBRG voltage is significantly higher than the required VBUS voltage, WLC1515 operates in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 12**.

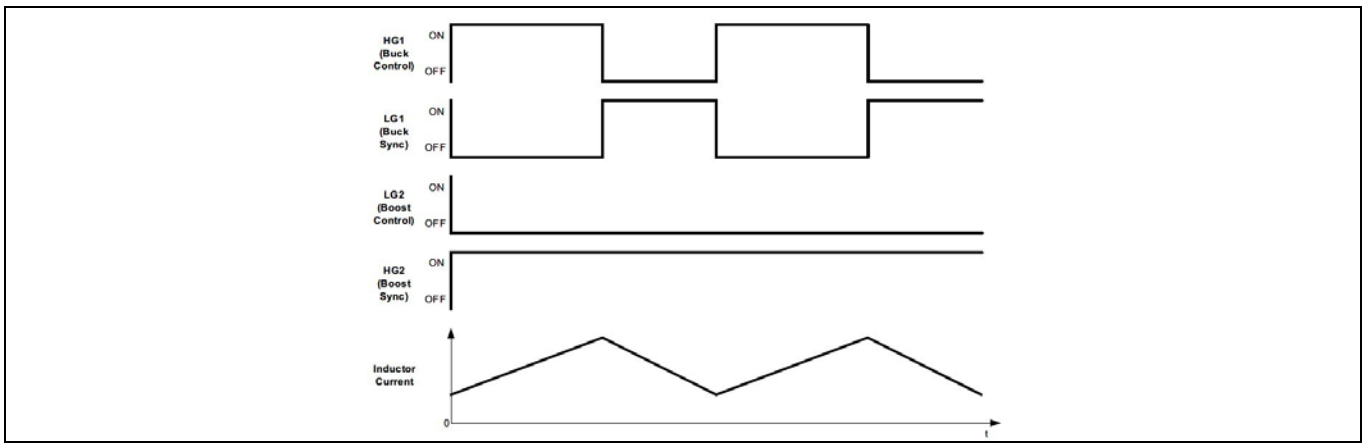


Figure 12 Buck operation waveforms

4.9.1.2 Boost region operation (VBUS << VBRG)

When the VBRG voltage is significantly lower than the required VBUS voltage, WLC1515 operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 13**.

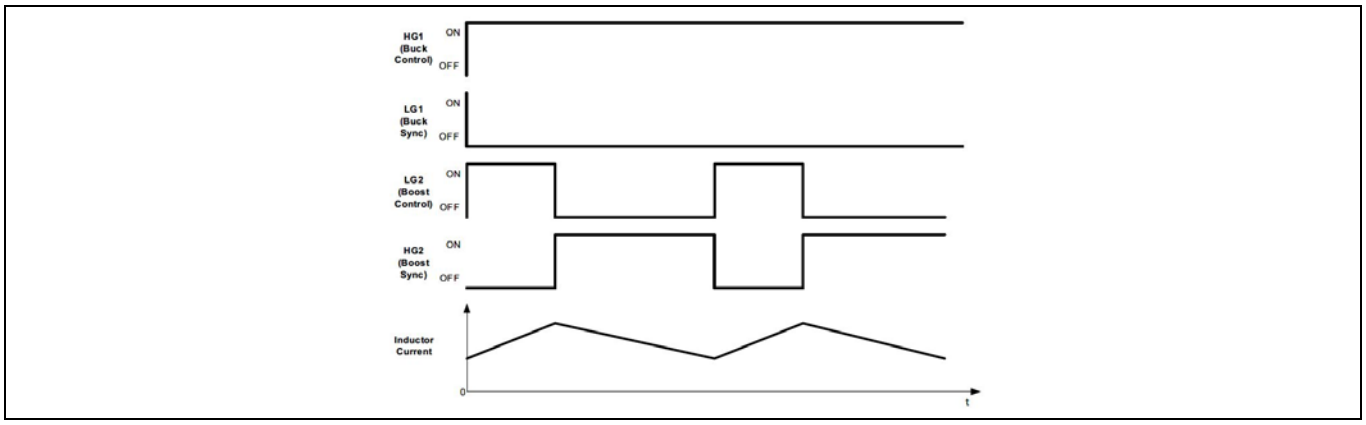


Figure 13 Boost operation waveforms

4.9.1.3 BuckBoost region 1 operation (VBUS ~> VBRG)

When the VBUS voltage is slightly higher than the required VBRG voltage, WLC1515 operate in the buckboost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 14**.

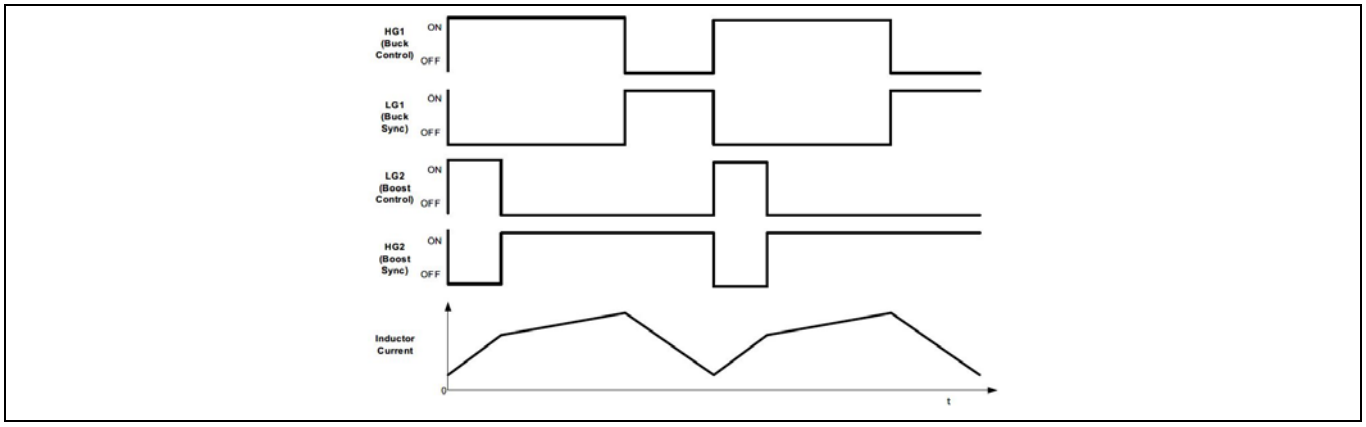


Figure 14 BuckBoost region 1 (VBUS ~> VBRG) operation waveforms

4.9.1.4 BuckBoost region 2 operation (VBUS ~< VBRG)

When the VBUS voltage is slightly lower than the required VBRG voltage, WLC1515 operate in the buckboost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 15**.

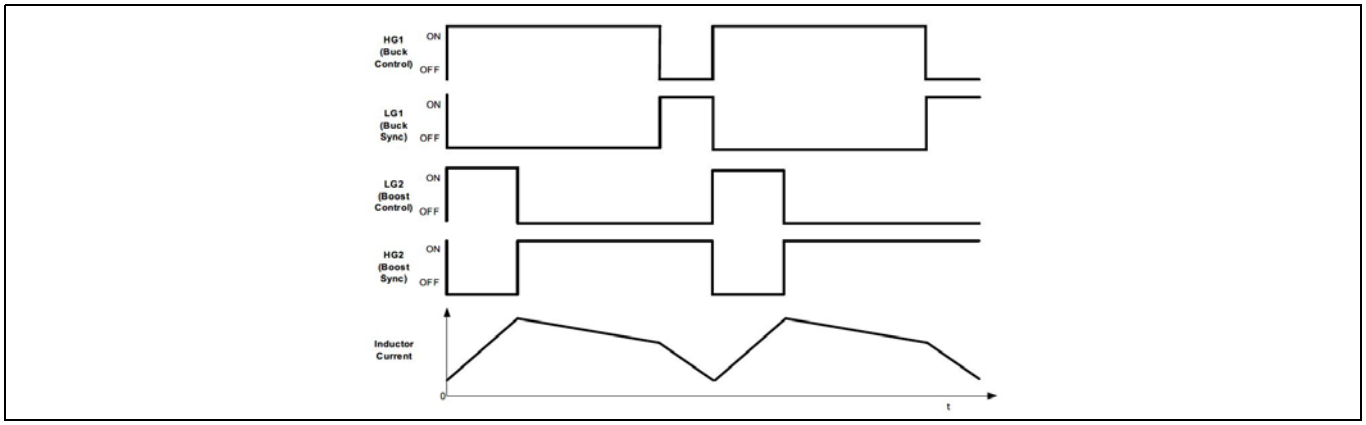


Figure 15 BuckBoost region 2 (VBUS ~< VBRG) operation waveforms

4.9.1.5 Switching frequency and spread spectrum.

WLC1515 offers programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

4.9.2 Pulse-width modulator (PWM)

The WLC1515 generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design. The WLC1515's buckboost primary operating mode when the buck, boost, and buck and boost is loaded by the inverter and power transfer is in progress. The WLC1515 have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: PSM and FCCM.

4.9.3 Pulse skipping mode (PSM)

In pulse-skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, the WLC1515 monitors the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the WLC1515 devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

4.9.4 Forced-continuous-conduction mode (FCCM)

In forced-continuous-conduction mode (FCCM), the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

4.9.5 Overvoltage protection (OVP)

The WLC1515 offers two types of overvoltage protections. The device monitors and limits VBUS and VBRG. In case of a VBUS overvoltage event detected, WLC1515 can be configured to shut down input voltage using NFET_CTRL_1. In case of VBRG over voltage events, the buckboost regulator is immediately shut down. The IC can be re-enabled after a physical disconnect and reconnect. The over-voltage fault thresholds are configurable.

4.9.6 Overcurrent protection (OCP)

The WLC1515 protects the inverter from over-current and short-circuit faults by monitoring the bridge current and continuously inspecting for over-current events using the internal CSAs that check the voltage on the current sense resistor. Similar to OVP, the OCP and SCP fault thresholds and response times are configurable as well. The IC can be re-enabled after a physical disconnect and reconnect.

4.9.7 MCU

The Cortex®-M0 in WLC1515 device is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. The device utilizes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode. Additionally, the WLC1515 device has 128-KB Flash and 32-KB ROM for nonvolatile storage. ROM stores libraries for device drivers such as I^2C, SPI, LIN, and so on. The main wireless power firmware is stored in Flash memory to provide the flexibility to store code for all wireless power features and enable the use of configuration tables. The device may be reset anytime by toggling the XRES pin to force a full hardware and software reset.

The WLC1515 devices support external clock (EXTCLK) or INTCLK for the MCU and all internal sub-systems that require clocks. To use the internal clock, float the CLK_IN pin. To use the optional external clock, provide a single ended clock to the CLK_IN pin oscillating at 48MHz.

The TCPWM block of the WLC1515 device has four timers, counters, or PWM (TCPWM) generators. These timers are used by FW to run the wireless power Tx system as required by WPC. The WLC1515 device also has a watchdog timer (WDT) that can be used by FW for various timeout events.

4.9.8 ADC

The WLC1515 device has 8-bit SAR ADCs available for general purpose analog-to-digital conversion applications within the chip and system. The ADCs are accessed from the GPIOs or directly on power supply pins through an on-chip analog mux. See the **"Electrical specifications"** on page 11 for detailed specifications of the ADCs.

4.9.9 Serial communications block (SCB)

The WLC1515 devices have four SCB blocks that can be configured for I^2C, SPI, UART, or LIN. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. I^2C is compatible with the standard Philips I2C specification V3.0. These blocks operate at speeds of up to 1Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for Receive and Transmit to decrease the time needed to interface by the MCU also reducing the need for clock stretching caused by the CPU not having read data on time.

4.9.10 I/O subsystem

The WLC1515 devices have 13 GPIOs but many of them have dedicated functions for 15W MP-A13 applications such as I2C comm, LED and temperature sensing in the wireless power application and cannot be repurposed. The GPIOs output states have integrated controls modes that can be enabled by FW which include: weak pull-up with strong pull-down, strong pull-up with weak pull-down, open drain with strong pull-down, open drain with strong pull-up, strong pull-up with strong pull-down, disabled, or weak pull-up with weak pull-down and offer selectable slew rates for dV/dt output control. When GPIOs are used as inputs they can be configured to support different input thresholds (CMOS or LVTTL).

During POR, the GPIO blocks are forced to the disable state preventing any excess currents from flowing.

4.9.11 LDOs (VDDD and VCCD)

The WLC1515 has two integrated LDO regulators. The VDDD LDO is powered by VIN and provides 5V for the GPIOs, gate drivers, and other internal blocks. The total load on VDDD LDO must be less than 150mA including internal consumption. VDDD LDO will be externally loaded as shown in the reference schematic. For connecting any additional external load on it, contact Infineon technical support. The VDDD 5V supply is externally routed to various pins and they should all be externally shorted together. The VCCD LDO is a 1.8V LDO regulator and is powered by VDDD. Do not externally load VCCD. Both LDOs must have ceramic bypass capacitors placed from each pin to ground close to the WLC1515 device.

5 Programming the WLC1515 device

Generally, the WLC1515 devices are programmed over the SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the WLC1515 device application firmware can be updated via the appropriate bootloader interface. Infineon strongly recommends customers to use the configuration utility to turn off the Application FW Update over I^2C interface in the firmware that is updated into WLC1515's flash before mass production.

5.1 Programming the device Flash over SWD interface

The WLC1515 family of devices can be programmed using the SWD interface. Infineon provides the **CY8CKIT-005 MiniProg4 Kit** which can be used to program the flash and debug firmware. The Flash is programmed by downloading the information from a *hex* file.

As shown in **Figure 16**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to the VDDD pins of the WLC1515 device. If the WLC1515 device is powered using an onboard power supply, it can be programmed using the "Reset Programming" option. For more details, refer the WLCXXXX programming specifications.

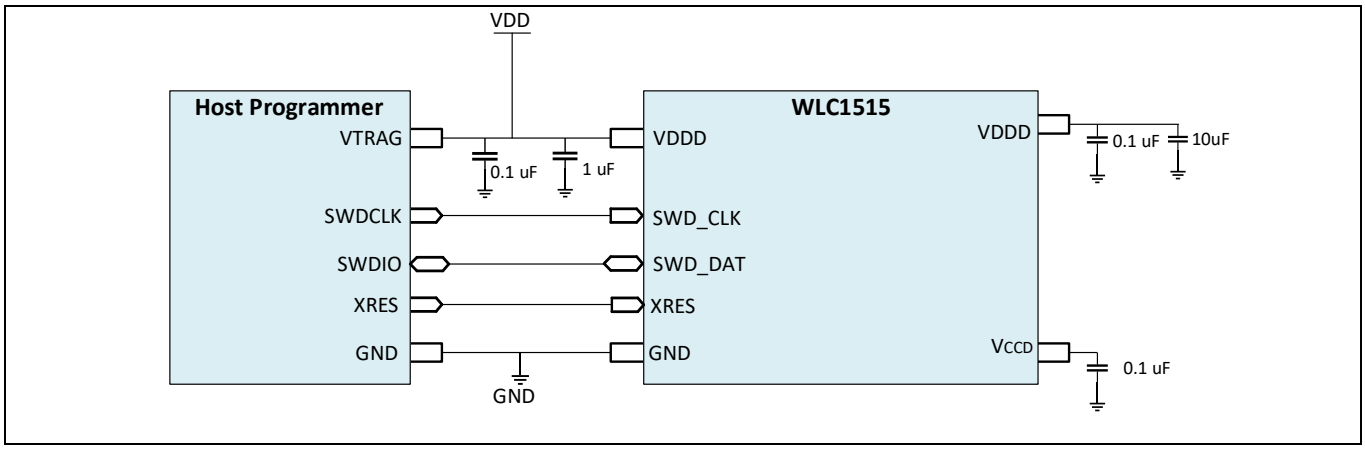


Figure 16 Connecting the programmer to WLC1515

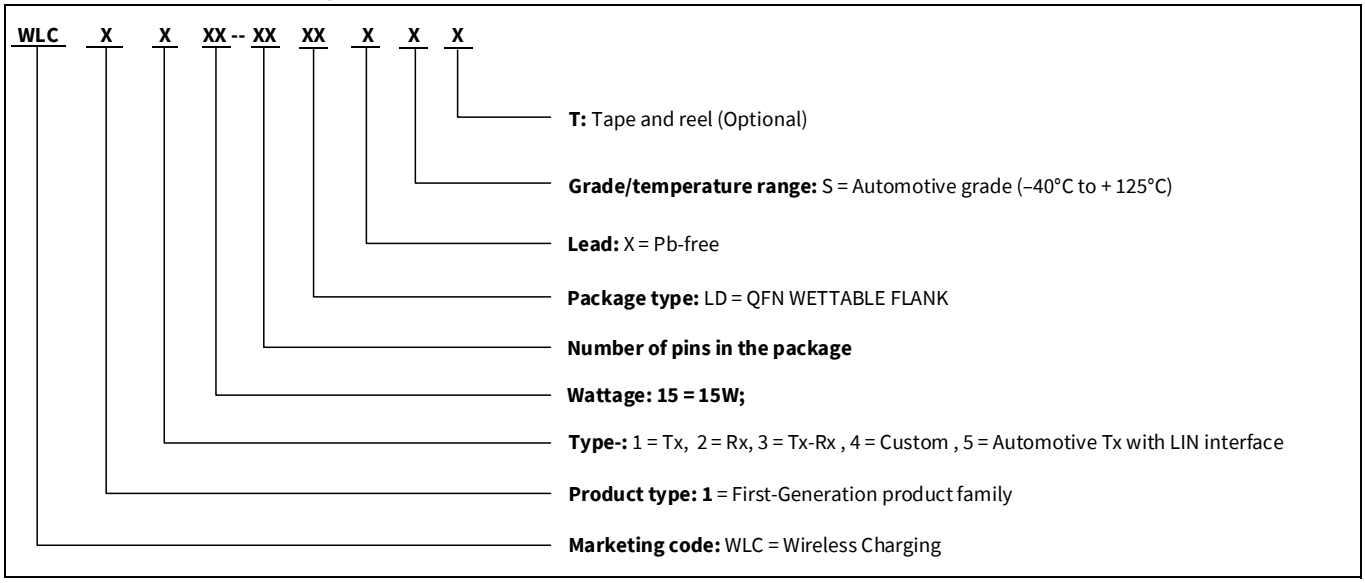
6 Ordering information

Table 19 lists the WLC1515 ordering part numbers and applications.

Table 19 WLC1515 ordering part numbers

MPN	Power	Application
WLC1515-68LDXS	15W	Qi v1.3.x EPP Tx
WLC1515-68LDXST		Qi v1.3.x EPP Tx - Tape and reel option

6.1 Ordering code definitions



7 Packaging

Table 20 Package characteristics

Parameter	Description	Test conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θJA		–	–	12.1	°C/W
T_{JC}	Package θJC				3.1	

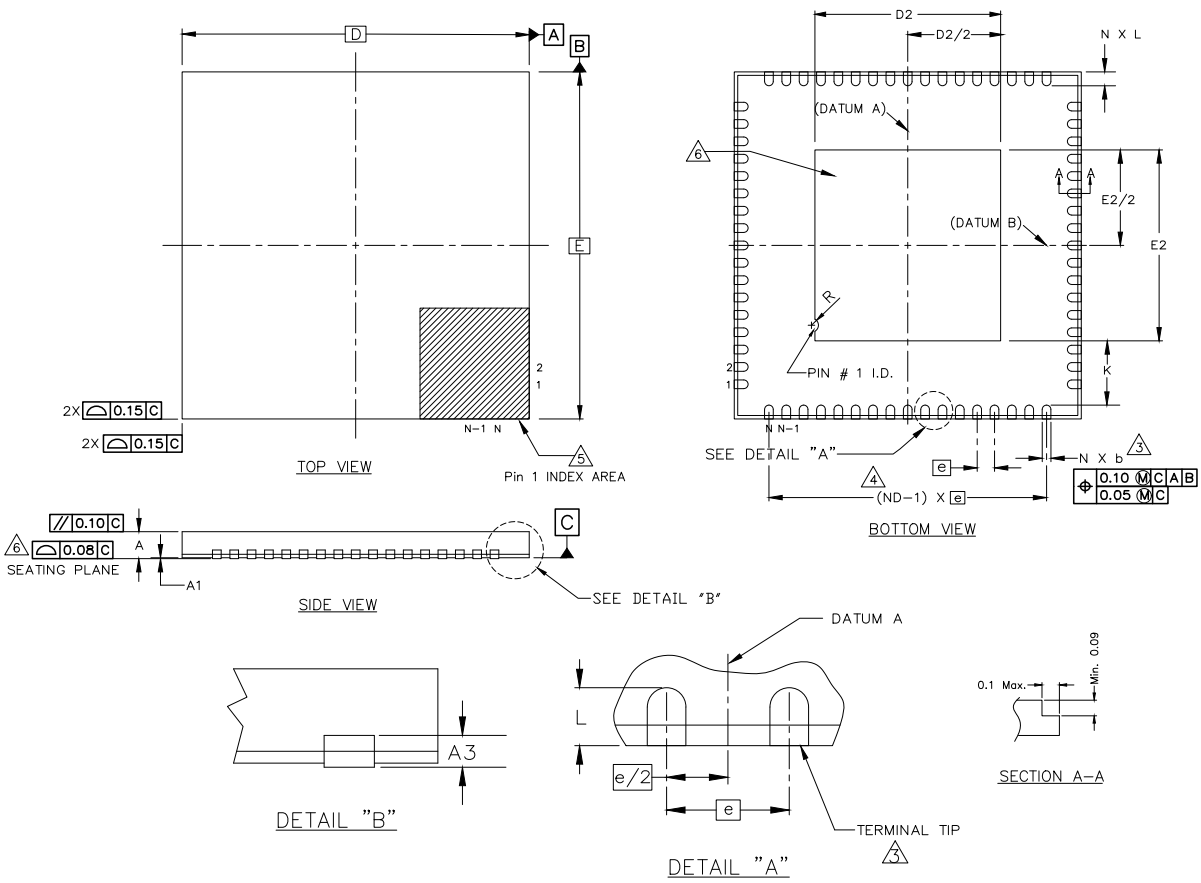
Table 21 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
68-pin QFN	260°C	30 seconds

Table 22 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3

8 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		68	
ND		17	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	5.25	5.35	5.45
E2	5.40	5.50	5.60
D		10.00 BSC	
E		10.00 BSC	
A	-	-	1.00
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.35 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-29306 *A

Figure 17 68-pin QFN (10 × 10) package outline

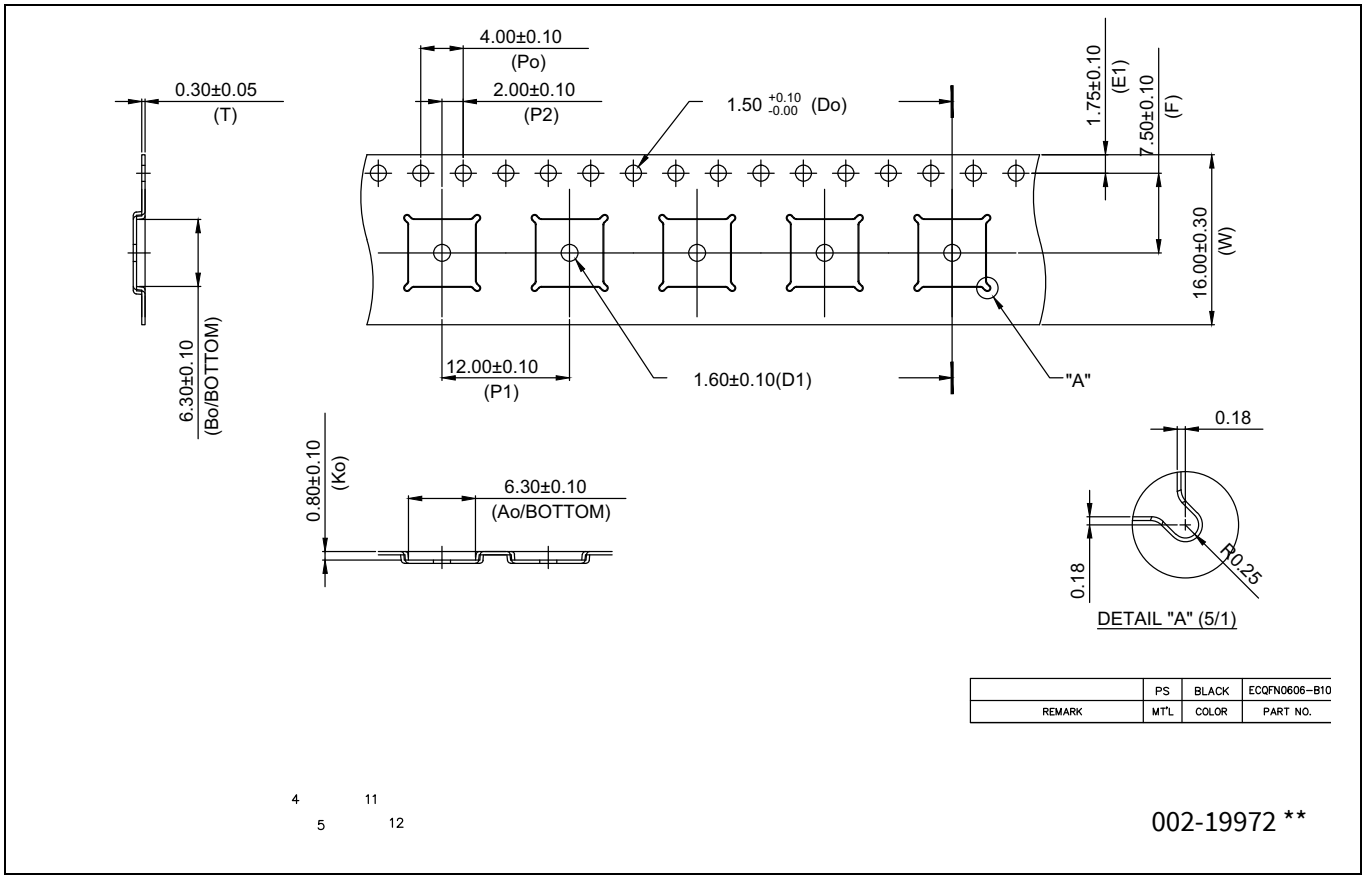


Figure 18 Carrier tape, QFN0606 (HWA SHU)

9 Acronyms

Table 23 Acronyms used in this document

Acronym	Description
ACK	Acknowledge
ADC	Analog-to-digital converter
Arm®	Advanced RISC machine, a CPU architecture
ASK	Amplitude shift key
BB	BuckBoost
BPP	Basic power profile
BMC	BiPhase mark code
CEP	Control error packet
CC	Configuration channel
CSA	Current sense amplifier
DCM	Discontinuous-conduction mode
EA	Error amplifier
EPP	Extended power profile
EPT	End power transfer
ESD	Electrostatic discharge
FET	Field effect transistor
FCCM	Forced-continuous-conduction mode
FOD	Foreign object detection
FO	Foreign object
FSK	Frequency shift key
FW	Firmware
GPIO	General-purpose I/O
HBM	Human body model
HS	High speed
I^2C	Inter-integrated circuit
IC	Integrated circuit
IMO	Internal main oscillator
IPT	Inductive power transfer technology
LDO	Linear drop out
LIN	Local Interconnect Network
MCU	Microcontroller unit
NTC	Negative temperature coefficient
NVIC	Nested vectored interrupt controller
OCP	Overcurrent protection
Opamp	Operational amplifier
OTP	Over temperature protection
OV	Overvoltage
OVP	Overvoltage protection

Table 23 Acronyms used in this document

Acronym	Description
PCB	Printed circuit board
POR	Power-on reset
PPDE	proprietary power delivery extensions
PPS	Programmable power supply
PSM	Pulse-skipping mode
PWM	Pulse-width modulator
QFOD	Q factor FOD
RPP	Received power packet
RCP	Reverse current protection
Rx	Power receiver
SAR	Successive approximation register
SCP	Short circuit protection
SPI	Serial peripheral interface
SSP	Signal strength packet
SWD	Serial wire debug, a test protocol
TCPWM	Timer/counter pulse-width modulation
Tx	Power transmitter
UART	Universal asynchronous receiver transmitter
UFP	Upstream facing port
UV	Undervoltage
WDT	Watchdog timer
WIC	Wakeup interrupt controller
WPC	Wireless power consortium
ZCD	Zero-crossing detector

10 Document conventions

10.1 Units of measure

Table 24 Units of measure

Symbol	Unit of measure
°C	degree Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
LSB	least significant bit
MHz	megahertz
MΩ	mega-ohm
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
%	percent
pF	picofarad
s	second
V	volt
W	watt

Revision history

Document revision	Date	Description of changes
*A	2023-05-18	Release to web.