

X9251

Single Supply/Low Power/256-Tap/SPI Bus, Quad Digitally-Controlled (XDCP™) Potentiometer

FN8166  
Rev 7.00  
January 14, 2021

The [X9251](#) integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile Data Registers that can be directly written to and read by the user. The content of the WCR controls the position of the wiper. At power-up, the device recalls the content of the default Data Registers of each DCP (DR00, DR10, DR20, and DR30) to the corresponding WCR.

The XDCP can be used as a three terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

**Features**

- Four potentiometers in one package
- 256 resistor taps–0.4% resolution
- SPI serial interface for write, read, and transfer operations of the potentiometer
- Wiper resistance: 100Ω typical at V<sub>CC</sub> = 5V
- 4 Nonvolatile data registers for each potentiometer
- Nonvolatile storage of multiple wiper positions
- Standby current <5μA max
- V<sub>CC</sub>: 2.7V to 5.5V operation
- 50kΩ version of total resistance
- 100 year data retention
- Single supply version of X9250
- Endurance: 100,000 data changes per bit per register
- 24 Ld TSSOP
- Low power CMOS
- Pb-free (RoHS compliant)

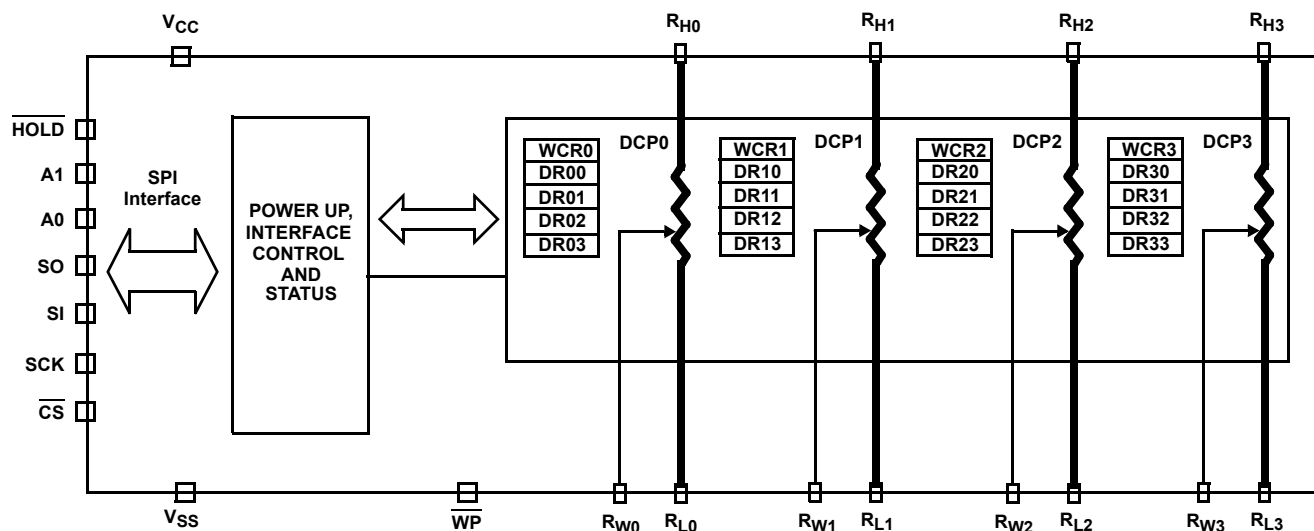


FIGURE 1. FUNCTIONAL DIAGRAM

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## Circuit Level Applications

- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

## System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

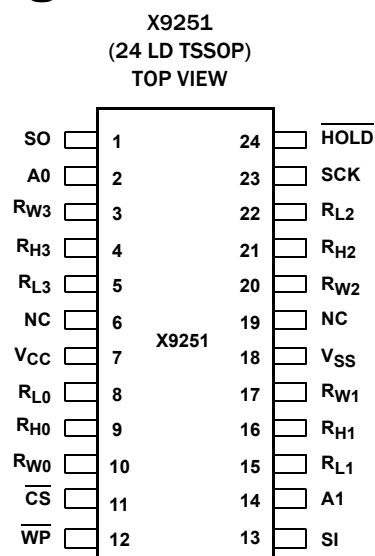
## Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | V <sub>CC</sub> LIMITS (V) | POTENTIOMETER ORGANIZATION (k $\Omega$ ) | TEMP RANGE (°C) | PACKAGE (Pb-Free)   | PKG. DWG. # |
|--------------------------|--------------|----------------------------|--|-----------------|---------------------|-------------|
| X9251UV24Z               | X9251UV Z    | 5 $\pm$ 10%                | 50                                       | 0 to +70        | 24 Ld TSSOP (4.4mm) | M24.173     |
| X9251UV24IZ              | X9251UV ZI   |                            |  | -40 to +85      | 24 Ld TSSOP (4.4mm) | M24.173     |
| X9251UV24Z-2.7           | X9251UV ZF   | 2.7 to 5.5                 |  | 0 to +70        | 24 Ld TSSOP (4.4mm) | M24.173     |
| X9251UV24IZ-2.7 (Note 1) | X9251UV ZG   |                            |  | -40 to +85      | 24 Ld TSSOP (4.4mm) | M24.173     |

### NOTES:

- Add "T1" suffix for tape and reel.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see product information page for [X9251](#). For more information on MSL, please see tech brief [TB363](#).

## Pin Configuration



## Pin Descriptions

| PIN   | SYMBOL          | FUNCTION   |
|-------|-----------------|--|
| 1     | SO              | Serial Data Output for SPI bus                           |
| 2     | A0              | Device Address for SPI bus (see <a href="#">Note 4</a> ) |
| 3     | RW3             | Wiper Terminal of DCP3                                   |
| 4     | RH3             | High Terminal of DCP3                                    |
| 5     | RL3             | Low Terminal of DCP3                                     |
| 7     | VCC             | System Supply Voltage                                    |
| 8     | RL0             | Low Terminal of DCPO                                     |
| 9     | RH0             | High Terminal of DCPO                                    |
| 10    | RW0             | Wiper Terminal of DCPO                                   |
| 11    | $\overline{CS}$ | SPI bus. Chip Select active low input                    |
| 12    | $\overline{WP}$ | Hardware Write Protect - active low                      |
| 13    | SI              | Serial Data Input for SPI bus                            |
| 14    | A1              | Device Address for SPI bus (see <a href="#">Note 4</a> ) |
| 15    | RL1             | Low Terminal of DCP1                                     |
| 16    | RH1             | High Terminal of DCP1                                    |
| 17    | RW1             | Wiper Terminal of DCP1                                   |
| 18    | VSS             | System Ground  |
| 20    | RW2             | Wiper Terminal of DCP2                                   |
| 21    | RH2             | High Terminal of DCP2                                    |
| 22    | RL2             | Low Terminal of DCP2                                     |
| 23    | SCK             | Serial Clock for SPI bus                                 |
| 24    | HOLD            | Device select. Pauses the SPI serial bus.                |
| 6, 19 | NC              | No Connect   |

### NOTE:

- A0 and A1 device address pins must be tied to a logic level.

## Functional Pin Descriptions

### Bus Interface Pins

#### SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted

out on this pin. Data is clocked out by the falling edge of the serial clock.

**SERIAL INPUT (SI)**

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the device registers are input on this pin. Data is latched by the rising edge of the serial clock.

**SERIAL CLOCK (SCK)**

The SCK input is used to clock data into and out of the X9251.

**HOLD ( $\overline{\text{HOLD}}$ )**

$\overline{\text{HOLD}}$  is used in conjunction with the  $\overline{\text{CS}}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{\text{HOLD}}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{\text{HOLD}}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{\text{HOLD}}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{\text{HOLD}}$  should be held HIGH at all times.

**DEVICE ADDRESS (A1 AND A0)**

The address inputs are used to set the two least significant bits of the slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9251. Device pins A1 and A0 must be tied to a logic level which specifies the internal address of the device, see [Figures 3, 4, 5, 6 and 7](#).

**CHIP SELECT ( $\overline{\text{CS}}$ )**

When  $\overline{\text{CS}}$  is HIGH, the X9251 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device is in the standby state.  $\overline{\text{CS}}$  LOW enables the X9251, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on  $\overline{\text{CS}}$  is required prior to the start of any operation.

**Potentiometer Pins** **$R_H$ ,  $R_L$** 

The  $R_H$  and  $R_L$  pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of  $R_H$  and  $R_L$  such that  $R_{H0}$  and  $R_{L0}$  are the terminals of DCPO and so on.

 **$R_W$** 

The wiper pins are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of  $R_W$  such that  $R_{W0}$  is the terminals of DCPO and so on.

**Supply Pins****SYSTEM SUPPLY VOLTAGE ( $V_{CC}$ ) AND SUPPLY GROUND ( $V_{SS}$ )**

The  $V_{CC}$  pin is the system supply voltage. The  $V_{SS}$  pin is the system ground.

**Other Pins****NO CONNECT**

No connect pins should be left floating. These pins are used for Renesas manufacturing and testing purposes.

**HARDWARE WRITE PROTECT INPUT ( $\overline{\text{WP}}$ )**

The  $\overline{\text{WP}}$  pin, when LOW, prevents nonvolatile writes to the Data Registers.

**Principles of Operation**

The X9251 is an integrated circuit incorporating four DCPs and their associated registers and counters, and a serial interface providing direct communication between a host and the potentiometers.

**DCP Description**

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer ( $R_H$  and  $R_L$  pins). The  $R_W$  pin is an intermediate node, equivalent to the wiper terminal of a mechanical potentiometer.

The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Counter Register (WCR).

## One of Four Potentiometers

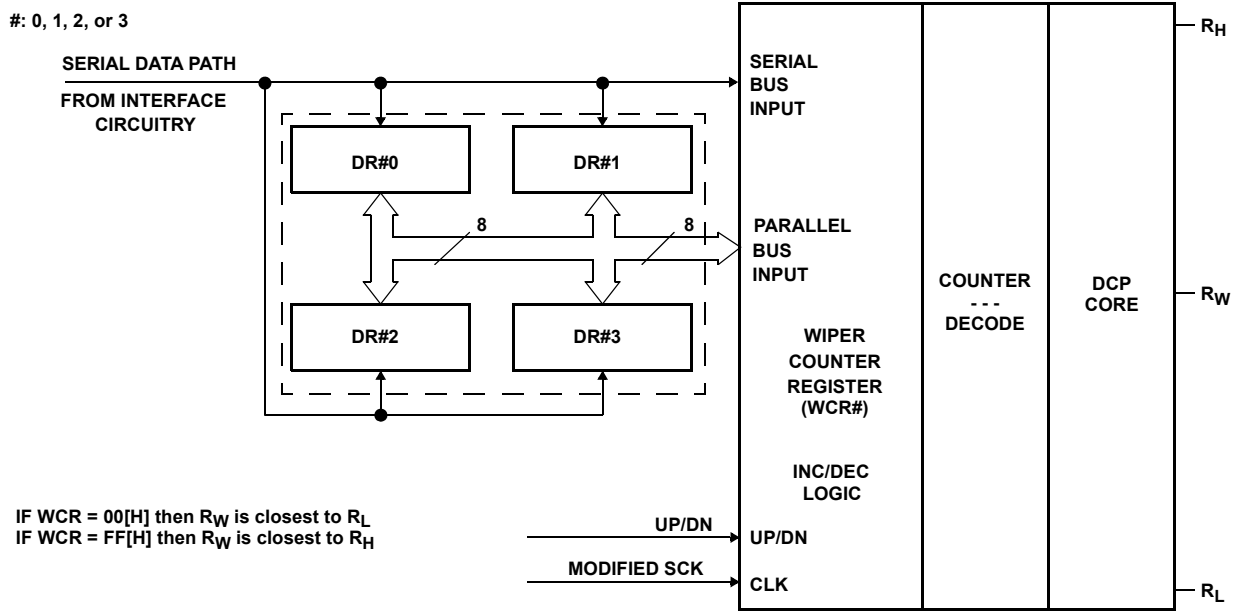


FIGURE 2. DETAILED POTENTIOMETER BLOCK DIAGRAM

### Power-Up and Down Recommendations

There are no restrictions on the power-up or power-down conditions of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that  $V_{CC}$  is always more positive than or equal to  $V_H$ ,  $V_L$ , and  $V_W$  (i.e.,  $V_{CC} \geq V_H, V_L, V_W$ ). The  $V_{CC}$  ramp rate specification is always in effect.

### Wiper Counter Register (WCR)

The X9251 contains four Wiper Counter Registers, one for each potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 wiper positions along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see [“Instruction Format” on page 10](#) for more details). Finally, it is loaded with the contents of its Data Register zero (DR#0) upon power-up (see [Figure 2](#)).

The wiper counter register is a volatile register; that is, its contents are lost when the X9251 is powered down. Although the register is automatically loaded with the value in DR#0 upon power-up, this may be different from the value present at

power-down. Power-up guidelines are recommended to ensure proper loadings of the DR#0 value into the WCR#.

### Data Registers (DR)

Each of the four DCPs has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and takes a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0 ~ 255).

### Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

- WIP = 1, indicates that high-voltage write cycle is in progress.
- WIP = 0, indicates that no high-voltage write cycle is in progress.

TABLE 1. WIPER COUNTER REGISTER, WCR (8-BIT), WCR[7:0]: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE)

| WCR7  | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0  |
|-------|------|------|------|------|------|------|-------|
| (MSB) |      |      |      |      |      |      | (LSB) |

TABLE 2. DATA REGISTER, DR (8-BIT), DR[7:0]: USED TO STORE WIPER POSITIONS OR DATA (NONVOLATILE)

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| (MSB) |       |       |       |       |       |       | (LSB) |

## Serial Interface

The X9251 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in, on the rising SCK.  $\overline{CS}$  must be LOW and the  $\overline{HOLD}$  and  $\overline{WP}$  pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three-state outputs. This can help to reduce system pin count.

### Identification Byte

The first byte sent to the X9251 from the host, following a  $\overline{CS}$  going HIGH to LOW, is called the Identification Byte. The most significant four bits of the Identification Byte are a Device Type Identifier, ID[3:0]. For the X9251, this is fixed as 0101 (refer to [Table 3](#)).

The least significant four bits of the Identification Byte are the Slave Address bits, AD[3:0]. For the X9251, A3 is 0, A2 is 0, A1 is the logic value at the input pin A1, and A0 is the logic value at the input pin A0. Only the device which Slave Address matches the incoming bits sent by the master executes the instruction. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to  $V_{CC}$  or  $V_{SS}$ .

### Instruction Byte

The next byte sent to the X9251 contains the instruction and register pointer information. The four most significant bits are used to provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCP. The least two significant bits point to one of four Wiper Counter Registers or DCPs. The format is shown below in [Table 4](#).

TABLE 3. IDENTIFICATION BYTE FORMAT

| DEVICE TYPE IDENTIFIER |     |     |     | SLAVE ADDRESS |    |                       |                       |
|------------------------|-----|-----|-----|---------------|----|-----------------------|-----------------------|
| ID3                    | ID2 | ID1 | ID0 | A3            | A2 | A1                    | A0                    |
| 0                      | 1   | 0   | 1   | 0             | 0  | Pin A1<br>Logic Value | Pin A0<br>Logic Value |
| (MSB)                  |     |     |     |               |    |                       | (LSB)                 |

TABLE 4. INSTRUCTION BYTE FORMAT

| INSTRUCTION OPCODE |    |    |    | REGISTER SELECTION |    | DCP SELECTION<br>(WCR SELECTION) |       |
|--------------------|----|----|----|--------------------|----|----------------------------------|-------|
| I3                 | I2 | I1 | I0 | RB                 | RA | P1                               | P0    |
| (MSB)              |    |    |    |                    |    |                                  | (LSB) |

### Data Register Selection

| REGISTER | RB | RA |
|----------|----|----|
| DR#0     | 0  | 0  |
| DR#1     | 0  | 1  |
| DR#2     | 1  | 0  |
| DR#3     | 1  | 1  |

#: 0, 1, 2, or 3

TABLE 5. INSTRUCTION SET

| INSTRUCTION                                 | INSTRUCTION SET |    |    |    |     |     |     |     | OPERATION   |
|---|-----------------|----|----|----|-----|-----|-----|-----|---|
|   | I3              | I2 | I1 | I0 | RB  | RA  | P1  | P0  |   |
| Read Wiper Counter Register                 | 1               | 0  | 0  | 1  | 0   | 0   | 1/0 | 1/0 | Read the contents of the Wiper Counter Register pointed to by P1, P0  |
| Write Wiper Counter Register                | 1               | 0  | 1  | 0  | 0   | 0   | 1/0 | 1/0 | Write new value to the Wiper Counter Register pointed to by P1, P0  |
| Read Data Register                          | 1               | 0  | 1  | 1  | 1/0 | 1/0 | 1/0 | 1/0 | Read the contents of the Data Register pointed to by P1, P0 and RB, RA  |
| Write Data Register                         | 1               | 1  | 0  | 0  | 1/0 | 1/0 | 1/0 | 1/0 | Write new value to the Data Register pointed to by P1, P0 and RB, RA  |
| XFR Data Register to Wiper Counter Register | 1               | 1  | 0  | 1  | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Data Register pointed to by P1, P0 and RB, RA to its associated Wiper Counter Register |

TABLE 5. INSTRUCTION SET (Continued)

| INSTRUCTION  | INSTRUCTION SET |    |    |    |     |     |     |     | OPERATION  |
|--|-----------------|----|----|----|-----|-----|-----|-----|--|
|  | I3              | I2 | I1 | I0 | RB  | RA  | P1  | P0  |  |
| XFR Wiper Counter Register to Data Register          | 1               | 1  | 1  | 0  | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Wiper Counter Register pointed to by P1, P0 to the Data Register pointed to by RB, RA             |
| Global XFR Data Registers to Wiper Counter Registers | 0               | 0  | 0  | 1  | 1/0 | 1/0 | 0   | 0   | Transfer the contents of the Data Registers pointed to by RB, RA of all four pots to their respective Wiper Counter Registers  |
| Global XFR Wiper Counter Registers to Data Register  | 1               | 0  | 0  | 0  | 1/0 | 1/0 | 0   | 0   | Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB, RA of all four pots |
| Increment/Decrement Wiper Counter Register           | 0               | 0  | 1  | 0  | 0   | 0   | 1/0 | 1/0 | Enable Increment/decrement of the Control Latch pointed to by P1, P0   |

NOTE: 1/0 = data is one or zero

## Instructions

Four of the nine instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer
- **Write Wiper Counter Register** – change current wiper position of the selected potentiometer
- **Read Data Register** – read the contents of the selected Data Register
- **Write Data Register** – write a new value to the selected Data Register
- **Read Status** – this command returns the contents of the WIP bit which indicates if the internal write cycle is in progress

The basic sequence of the three-byte instructions is illustrated in [Figure 4](#). These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action is delayed by  $t_{WRL}$ . A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the four potentiometer's WCR, and one of its associated registers, DRs; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (see [Figure 6](#)).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9251; either between the host and one of the data registers or directly

between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

## Increment/Decrement Command

The final command is Increment/Decrement (see [Figures 7](#) and [8](#)). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9251 has responded with an Acknowledge, the master can clock the selected wiper up and/or down in one segment steps, thereby providing a fine tuning capability to the host. For each SCK clock pulse ( $t_{HIGH}$ ) while SI is HIGH, the selected wiper moves one wiper position towards the  $R_H$  terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper moves one wiper position towards the  $R_L$  terminal. A detailed illustration of the sequence and timing for this operation are shown. See [“Instruction Format” on page 10](#) for more details.

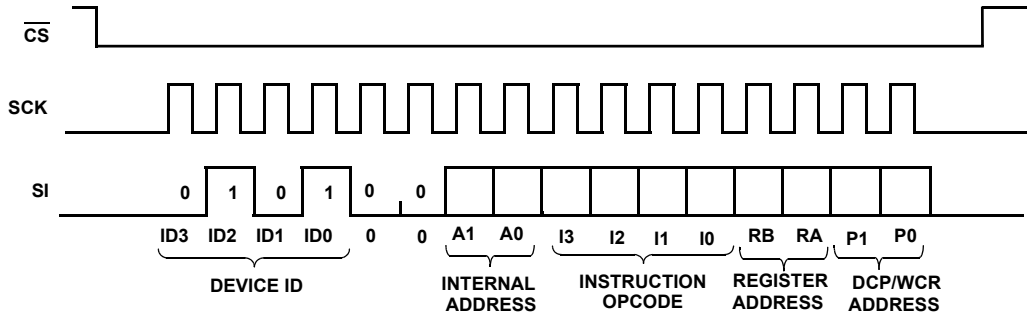


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

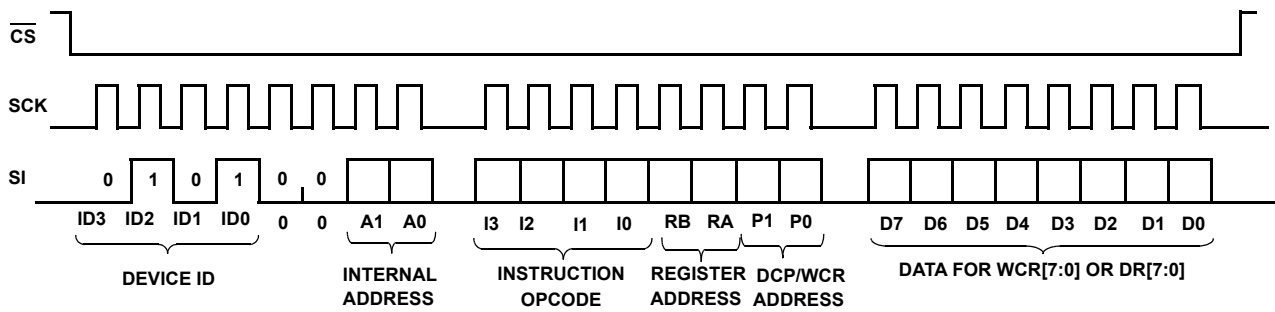


FIGURE 4. THREE-BYTE INSTRUCTION SEQUENCE SPI INTERFACE; WRITE CASE

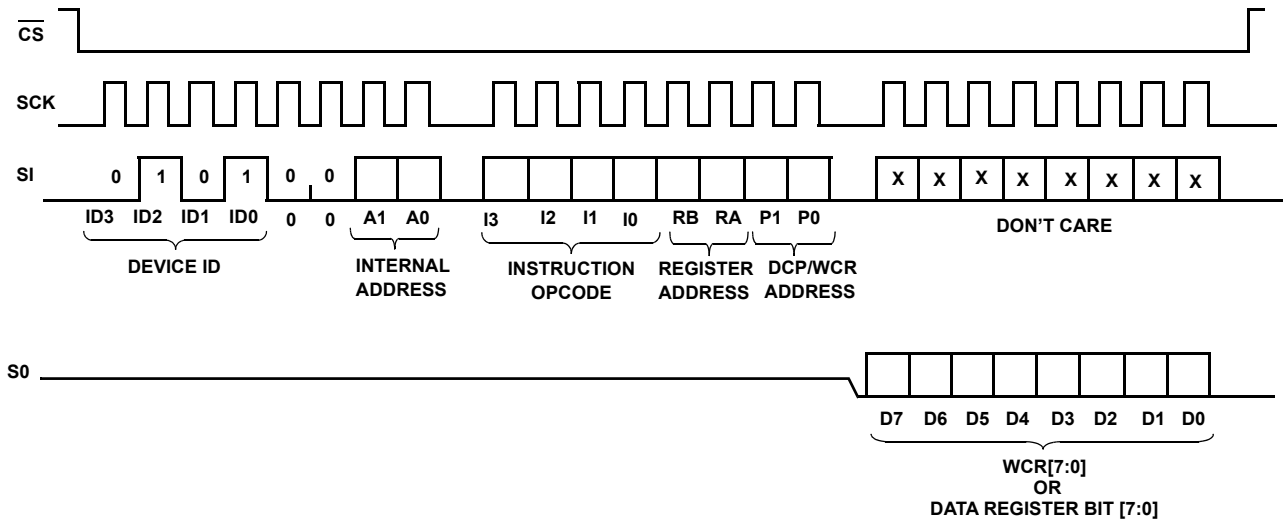


FIGURE 5. THREE-BYTE INSTRUCTION SEQUENCE SPI INTERFACE, READ CASE



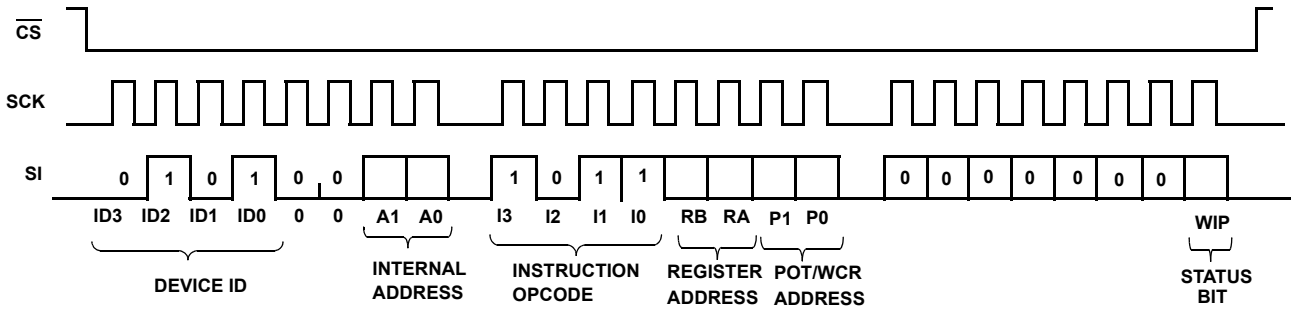


FIGURE 6. THREE-BYTE INSTRUCTION SEQUENCE (READ STATUS REGISTER)

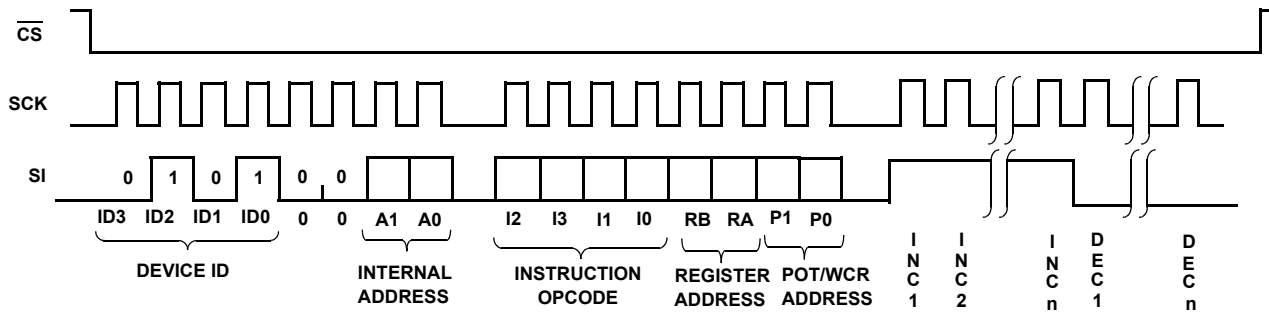


FIGURE 7. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

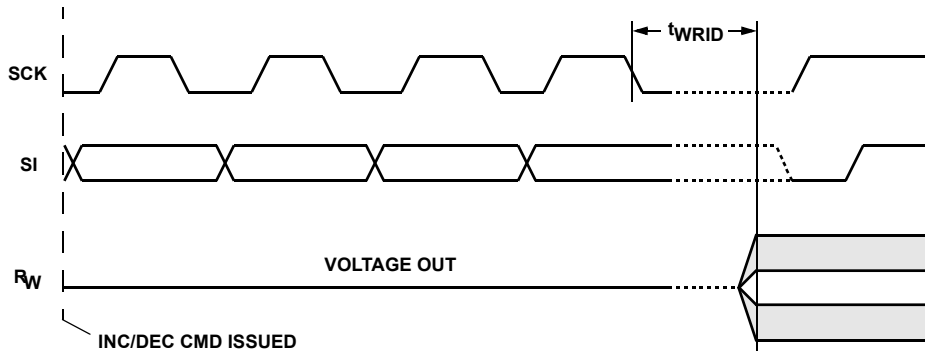


FIGURE 8. INCREMENT/DECREMENT TIMING SPEC

## Instruction Format

### Read Wiper Counter Register (WCR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | WCR<br>ADDRESSES |   |   |   | WIPER POSITION<br>(SENT BY X9251 ON SO) |   |   |   |   |   |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE |   |   |   |   |   |   |   |   |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|------------------|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 0 | 0 | 1 | 0                | 0 | 0 | 0 | W                                       | W | W | W | W | W | W | W |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | C                                       | C | C | C | C | C | C | C |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | R                                       | R | R | R | R | R | R | R |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | 7                                       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |   |   |   |   |   |   |   |   |

### Write Wiper Counter Register (WCR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | WCR<br>ADDRESSES |   |   |   | DATA BYTE<br>(SENT BY HOST ON SI) |   |   |   |   |   |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE |   |   |   |   |   |   |   |   |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|------------------|---|---|---|-----------------------------------|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 0 | 1 | 0 | 0                | 0 | 0 | 0 | W                                 | W | W | W | W | W | W | W |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | C                                 | C | C | C | C | C | C | C |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | R                                 | R | R | R | R | R | R | R |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                  |   |   |   | 7                                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |   |   |   |   |   |   |   |   |

### Read Data Register (DR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | DR AND WCR<br>ADDRESSES |    |    |    | DATA BYTE<br>(SENT BY X9271 ON SO) |   |   |   |   |   |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE |   |   |   |   |   |   |   |   |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-------------------------|----|----|----|------------------------------------|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 0 | 1 | 1 | RB                      | RA | P1 | P0 | D                                  | D | D | D | D | D | D | D |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                    |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                    |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                    |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |

### Write Data Register (DR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | DR AND WCR<br>ADDRESSES |    |    |    | DATA BYTE<br>(SENT BY HOST ON SI) |   |   |   |   |   |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE | HIGH-VOLTAGE<br>WRITE CYCLE |   |   |   |   |   |   |   |   |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-------------------------|----|----|----|-----------------------------------|---|---|---|---|---|---|---|--|-----------------------------|---|---|---|---|---|---|---|---|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 1 | 0 | 0 | RB                      | RA | P1 | P0 | D                                 | D | D | D | D | D | D | D |  |                             | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                   |   |   |   |   |   |   |   |  |                             |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                   |   |   |   |   |   |   |   |  |                             |   |   |   |   |   |   |   |   |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |    |    |                                   |   |   |   |   |   |   |   |  |                             |   |   |   |   |   |   |   |   |

### Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | DR<br>ADDRESSES |    |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE |  |  |  |  |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-----------------|----|---|---|--|--|--|--|--|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 0                     | 0 | 0 | 1 | RB              | RA | 0 | 0 |  |  |  |  |  |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                 |    |   |   |  |  |  |  |  |

### Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | DR<br>ADDRESSES |    |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE | HIGH-VOLTAGE<br>WRITE CYCLE |  |  |  |  |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-----------------|----|---|---|--|-----------------------------|--|--|--|--|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 0 | 0 | 0 | RB              | RA | 0 | 0 |  |                             |  |  |  |  |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                 |    |   |   |  |                             |  |  |  |  |

### Transfer Wiper Counter Register (WCR) to Data Register (DR)

| $\overline{\text{CS}}$<br>FALLING<br>EDGE | DEVICE TYPE<br>IDENTIFIER |   |   |   | DEVICE<br>ADDRESSES |   |    |    | INSTRUCTION<br>OPCODE |   |   |   | DR AND WCR<br>ADDRESSES |    |   |   | $\overline{\text{CS}}$<br>RISING<br>EDGE | HIGH-VOLTAGE<br>WRITE CYCLE |  |  |  |  |
|---|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-------------------------|----|---|---|--|-----------------------------|--|--|--|--|
|   | 0                         | 1 | 0 | 1 | 0                   | 0 | A1 | A0 | 1                     | 1 | 1 | 0 | RB                      | RA | 0 | 0 |  |                             |  |  |  |  |
|   |                           |   |   |   |                     |   |    |    |                       |   |   |   |                         |    |   |   |  |                             |  |  |  |  |

### Transfer Data Register (DR) to Wiper Counter Register (WCR)

| $\overline{\text{CS}}$ FALLING EDGE | DEVICE TYPE IDENTIFIER |   |   |   | DEVICE ADDRESSES |   |    |    | INSTRUCTION OPCODE |   |   |   | DR AND WCR ADDRESSES |    |   |   | $\overline{\text{CS}}$ RISING EDGE |
|-------------------------------------|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|----------------------|----|---|---|------------------------------------|
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 1                  | 1 | 0 | 1 | RB                   | RA | 0 | 0 |                                    |
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 1                  | 1 | 0 | 1 | RB                   | RA | 0 | 0 |                                    |

### Increment/Decrement Wiper Counter Register (WCR)

| $\overline{\text{CS}}$ FALLING EDGE | DEVICE TYPE IDENTIFIER |   |   |   | DEVICE ADDRESSES |   |    |    | INSTRUCTION OPCODE |   |   |   | WCR ADDRESSES |   |   |   | INCREMENT/DECREMENT (SENT BY MASTER ON SI) |     |   |   | $\overline{\text{CS}}$ RISING EDGE |   |     |     |     |
|-------------------------------------|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|---------------|---|---|---|--|-----|---|---|------------------------------------|---|-----|-----|-----|
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 0                  | 0 | 1 | 0 | X             | X | 0 | 0 | I/D  | I/D | . | . |                                    | . | .   | I/D | I/D |
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 0                  | 0 | 1 | 0 | X             | X | 0 | 0 | I/D  | I/D | . | . | .                                  | . | I/D | I/D |     |

### Read Status Register (SR)

| $\overline{\text{CS}}$ FALLING EDGE | DEVICE TYPE IDENTIFIER |   |   |   | DEVICE ADDRESSES |   |    |    | INSTRUCTION OPCODE |   |   |   | WCR ADDRESSES |   |   |   | DATA BYTE (SENT BY X9251 ON SO) |   |   |   |   |   |   |   | $\overline{\text{CS}}$ RISING EDGE |   |   |   |     |     |
|-------------------------------------|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|---------------|---|---|---|---------------------------------|---|---|---|---|---|---|---|------------------------------------|---|---|---|-----|-----|
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 0                  | 1 | 0 | 1 | 0             | 0 | 0 | 1 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 |                                    | 0 | 0 | 0 | 0   | WIP |
|                                     | 0                      | 1 | 0 | 1 | 0                | 0 | A1 | A0 | 0                  | 1 | 0 | 1 | 0             | 0 | 0 | 1 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | WIP |     |

NOTES:

5. "A1 ~ A0": stands for the device addresses sent by the master.
6. WPx refers to wiper position data in the Counter Register
7. "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
8. "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

## Absolute Maximum Ratings

|  |                 |
|--|-----------------|
| Temperature Under Bias   | -65°C to +135°C |
| Storage Temperature  | -65°C to +150°C |
| Voltage on SCK, CS, SI, SO, WP, HOLD, V <sub>CC</sub><br>with respect to V <sub>SS</sub> | -1V to +7V      |
| $\Delta V =  V_H - V_L $   | 5.5V            |
| Lead Temperature (Soldering, 10s)  | +300°C          |
| I <sub>W</sub> (10s)   | ±6mA            |
| Wiper Current  | ±3mA            |
| Power Rating (each pot)  | .50mW           |

## Recommended Operating Conditions

|  |                           |
|--|---------------------------|
| Commercial Temperature Range                       | 0°C to +70°C              |
| Industrial Temperature Range                       | -40°C to +85°C            |
| Supply Voltage (V <sub>CC</sub> ) Limits (Note 12) |                           |
| X9251  | .5V ±10%                  |
| X9251-2.7  | 2.7V to 5.5V              |
| Pb-Free Reflow Profile                             | see <a href="#">TB493</a> |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## Analog Characteristics

 Over the recommended operating conditions unless otherwise specified.

| SYMBOL   | PARAMETER   | TEST CONDITIONS   | MIN             | TYP      | MAX             | UNITS           |
|--|---|---|-----------------|----------|-----------------|-----------------|
| R <sub>TOTAL</sub>                             | End to End Resistance                               | U version   |                 | 50       |                 | kΩ              |
|  | End to End Resistance Tolerance                     |   |                 |          | ±20             | %               |
| R <sub>W</sub>                                 | Wiper Resistance                                    | $I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ at V <sub>CC</sub> = 3V       |                 |          | 300             | Ω               |
|  |   | $I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ at V <sub>CC</sub> = 5V       |                 |          | 220             | Ω               |
| V <sub>TERM</sub>                              | Voltage on any R <sub>H</sub> or R <sub>L</sub> Pin | V <sub>SS</sub> = 0V  | V <sub>SS</sub> |          | V <sub>CC</sub> | V               |
|  | Noise (Note 14)                                     | Ref: 1V   |                 | -120     |                 | dBV/√Hz         |
|  | Resolution  |   |                 | 0.4      |                 | %               |
|  | Absolute Linearity (Note 9)                         | R <sub>W(n)(actual)</sub> - R <sub>W(n)(expected)</sub> (Note 13) | -1              |          | +1              | MI<br>(Note 11) |
|  | Relative Linearity (Note 10)                        | R <sub>W(n+1)</sub> - [R <sub>W(n)</sub> + MI] (Note 13)          | -0.6            |          | +0.6            | MI<br>(Note 11) |
|  | Temperature Coefficient of R <sub>TOTAL</sub>       | (Note 14)   |                 | ±300     |                 | ppm/°C          |
|  | Ratiometric Temp. Coefficient                       | (Note 14)   |                 | ±20      |                 | ppm/°C          |
| C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub> | Potentiometer Capacitances                          | See macromodel on <a href="#">page 13</a> , (Note 14)             |                 | 10/10/25 |                 | pF              |

## DC Operating Characteristics

 Over the recommended operating conditions unless otherwise specified.

| SYMBOL           | PARAMETER  | TEST CONDITIONS  | MIN                   | TYP | MAX                   | UNITS |
|------------------|--|--|-----------------------|-----|-----------------------|-------|
| I <sub>CC1</sub> | V <sub>CC</sub> Supply Current (Active)            | f <sub>SCK</sub> = 2.5MHz, SO = Open, V <sub>CC</sub> = 6V<br>Other Inputs = V <sub>SS</sub> |                       |     | 400                   | μA    |
| I <sub>CC2</sub> | V <sub>CC</sub> Supply Current (Nonvolatile Write) | f <sub>SCK</sub> = 2.5MHz, SO = Open, V <sub>CC</sub> = 6V<br>Other Inputs = V <sub>SS</sub> |                       | 1   | 5                     | mA    |
| I <sub>SB</sub>  | V <sub>CC</sub> Current (Standby)                  | SCK = SI = V <sub>SS</sub> , Addr. = V <sub>SS</sub> ,<br>CS = V <sub>CC</sub> = 6V          |                       |     | 3                     | μA    |
| I <sub>LI</sub>  | Input Leakage Current                              | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>   |                       |     | 10                    | μA    |
| I <sub>LO</sub>  | Output Leakage Current                             | V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>  |                       |     | 10                    | μA    |
| V <sub>IH</sub>  | Input HIGH Voltage                                 |  | V <sub>CC</sub> × 0.7 |     |                       | V     |
| V <sub>IL</sub>  | Input LOW Voltage                                  |  |                       |     | V <sub>CC</sub> × 0.3 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                                 | I <sub>OL</sub> = 3mA  |                       |     | 0.4                   | V     |
| V <sub>OH</sub>  | Output HIGH Voltage                                | I <sub>OH</sub> = -1mA, V <sub>CC</sub> ≥ +3V  | V <sub>CC</sub> - 0.8 |     |                       | V     |
| V <sub>OH</sub>  | Output HIGH Voltage                                | I <sub>OH</sub> = -0.4mA, V <sub>CC</sub> ≤ +3V  | V <sub>CC</sub> - 0.4 |     |                       | V     |

## Endurance and Data Retention

| PARAMETER         | MIN     | UNITS                             |
|-------------------|---------|-----------------------------------|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention    | 100     | years                             |

## Capacitance

| SYMBOL                 | TEST  | TEST CONDITIONS | TYP | UNITS |
|------------------------|---|-----------------|-----|-------|
| $C_{IN/OUT}$ (Note 14) | Input/Output capacitance (SI)   | $V_{OUT} = 0V$  | 8   | pF    |
| $C_{OUT}$ (Note 14)    | Output capacitance (SO)   | $V_{OUT} = 0V$  | 8   | pF    |
| $C_{IN}$ (Note 14)     | Input capacitance (A0, A1, $\overline{CS}$ , $\overline{WP}$ , $\overline{HOLD}$ , and SCK) | $V_{IN} = 0V$   | 6   | pF    |

## Power-Up Timing

| SYMBOL                 | PARAMETER                                 | MIN | MAX | UNITS |
|------------------------|---|-----|-----|-------|
| $t_r V_{CC}$ (Note 14) | $V_{CC}$ Power-up Rate                    | 0.2 |     | V/ms  |
| $t_{PUR}$ (Note 15)    | Power-up to Initiation of Read Operation  |     | 1   | ms    |
| $t_{PUW}$ (Note 15)    | Power-up to Initiation of Write Operation |     | 50  | ms    |

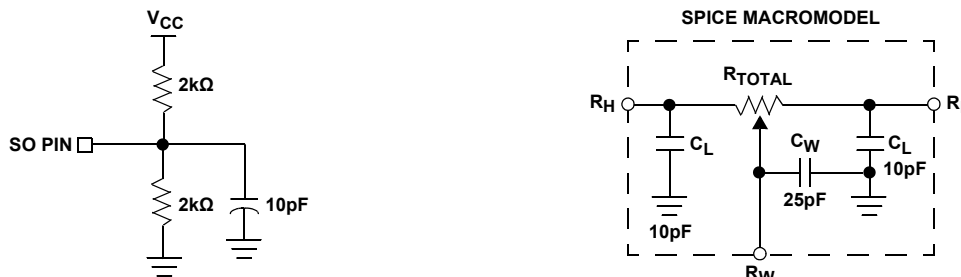
## AC Test Conditions

|                               |  |
|-------------------------------|--|
| Input Pulse Levels            | $V_{CC} \times 0.1$ to $V_{CC} \times 0.9$ |
| Input Rise and Fall Times     | 10ns                                       |
| Input and Output Timing Level | $V_{CC} \times 0.5$                        |

### NOTES:

- Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
- Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
- $MI = RTOT/255$  or  $(R_H - R_L)/255$ , single pot.
- During power up  $V_{CC} > V_H, V_L$ , and  $V_W$ .
- $n = 0, 1, 2, \dots, 255$ ;  $m = 0, 1, 2, \dots, 254$ .
- This parameter is not 100% tested
- $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time the (last) power supply ( $V_{CC}$ ) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

## Equivalent AC Load Circuit



**AC TIMING**

| SYMBOL                    | PARAMETER  | MIN | TYP | MAX | UNITS |
|---------------------------|--|-----|-----|-----|-------|
| f <sub>SCK</sub>          | SPI clock frequency  |     |     | 2   | MHz   |
| t <sub>CYC</sub>          | SPI Clock Cycle Time   | 500 |     |     | ns    |
| t <sub>WH</sub>           | SPI Clock High Time  | 200 |     |     | ns    |
| t <sub>WL</sub>           | SPI Clock Low Time   | 200 |     |     | ns    |
| t <sub>LEAD</sub>         | Lead Time  | 250 |     |     | ns    |
| t <sub>LAG</sub>          | Lag Time   | 250 |     |     | ns    |
| t <sub>SU</sub>           | SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ Input Setup Time                          | 50  |     |     | ns    |
| t <sub>H</sub>            | SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ Input Hold Time                           | 50  |     |     | ns    |
| t <sub>RI</sub>           | SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ Input Rise Time                           |     |     | 2   | μs    |
| t <sub>FI</sub>           | SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ Input Fall Time                           |     |     | 2   | μs    |
| t <sub>DIS</sub>          | SO Output Disable Time   | 0   |     | 250 | ns    |
| t <sub>V</sub>            | SO Output Valid Time   |     |     | 200 | ns    |
| t <sub>HO</sub>           | SO Output Hold Time  | 0   |     |     | ns    |
| t <sub>RO</sub> (Note 14) | SO Output Rise Time  |     |     | 100 | ns    |
| t <sub>FO</sub> (Note 14) | SO Output Fall Time  |     |     | 100 | ns    |
| t <sub>HOLD</sub>         | $\overline{\text{HOLD}}$ Time  | 400 |     |     | ns    |
| t <sub>HSU</sub>          | $\overline{\text{HOLD}}$ Setup Time  | 100 |     |     | ns    |
| t <sub>HH</sub>           | $\overline{\text{HOLD}}$ Hold Time   | 100 |     |     | ns    |
| t <sub>HZ</sub>           | $\overline{\text{HOLD}}$ Low to Output in High Z   |     |     | 100 | ns    |
| t <sub>LZ</sub>           | $\overline{\text{HOLD}}$ High to Output in Low Z   |     |     | 100 | ns    |
| T <sub>I</sub>            | Noise Suppression Time Constant at SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ Inputs |     | 10  |     | ns    |
| t <sub>CS</sub>           | $\overline{\text{CS}}$ Deselect Time   | 2   |     |     | μs    |
| t <sub>WPASU</sub>        | $\overline{\text{WP}}$ , A0 Setup Time   | 0   |     |     | ns    |
| t <sub>WPAH</sub>         | $\overline{\text{WP}}$ , A0 Hold Time  | 0   |     |     | ns    |

**High-Voltage Write Cycle Timing**

| SYMBOL          | PARAMETER  | TYP | MAX | UNITS |
|-----------------|--|-----|-----|-------|
| t <sub>WR</sub> | High-voltage write cycle time (store instructions) | 5   | 10  | ms    |

**XDCP Timing**

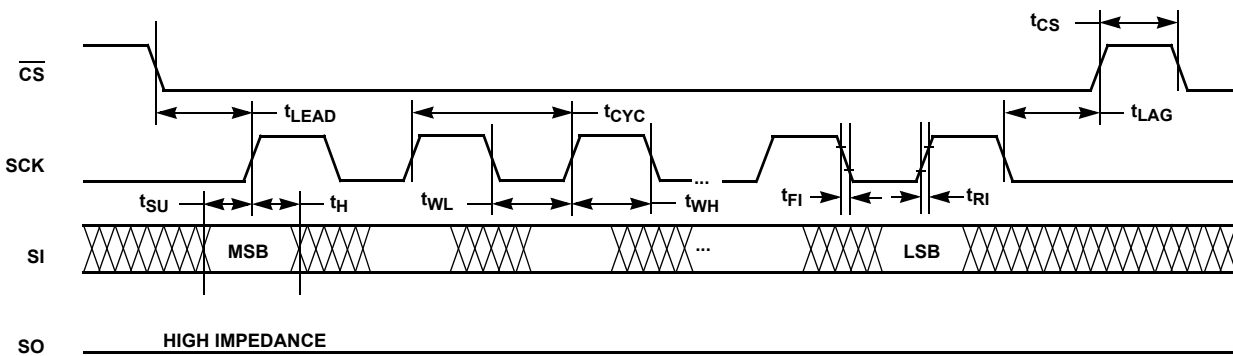
| SYMBOL                      | PARAMETER  | MIN | MAX | UNITS |
|-----------------------------|--|-----|-----|-------|
| t <sub>WRPO</sub> (Note 14) | Wiper response time after the third (last) power supply is stable    | 5   | 10  | μs    |
| t <sub>WRL</sub> (Note 14)  | Wiper response time after instruction issued (all load instructions) | 5   | 10  | μs    |

## Symbol Table

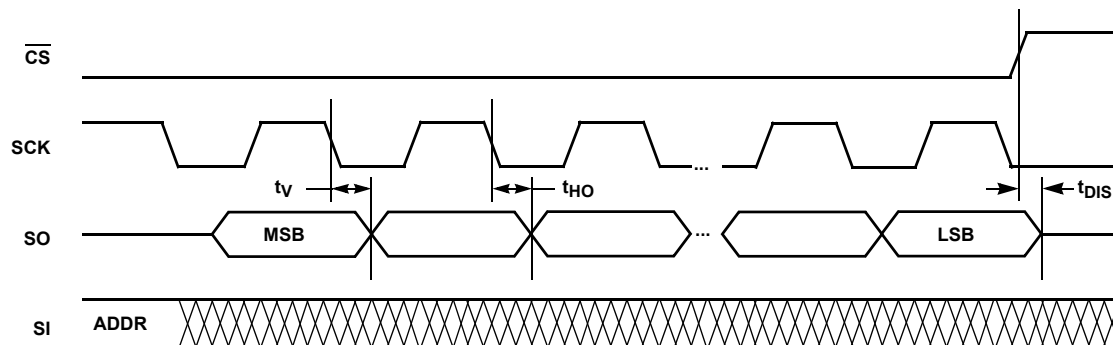
| WAVEFORM | INPUTS                      | OUTPUTS                       |
|----------|-----------------------------|-------------------------------|
|          | Must be steady              | Will be steady                |
|          | May change from Low to High | Will change from Low to High  |
|          | May change from High to Low | Will change from High to Low  |
|          | Don't Care: Changes Allowed | Changing: State Not Known     |
|          | N/A                         | Center Line is High Impedance |

## Timing Diagrams

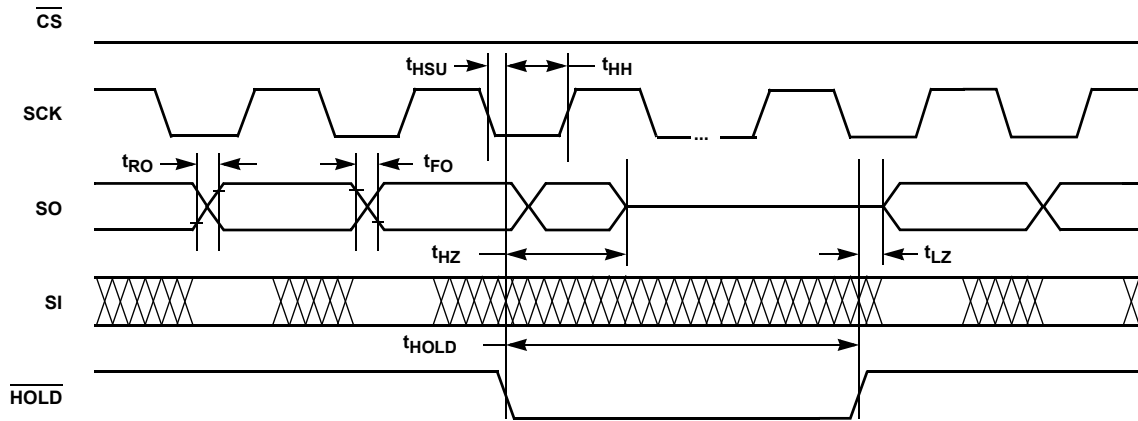
### Input Timing



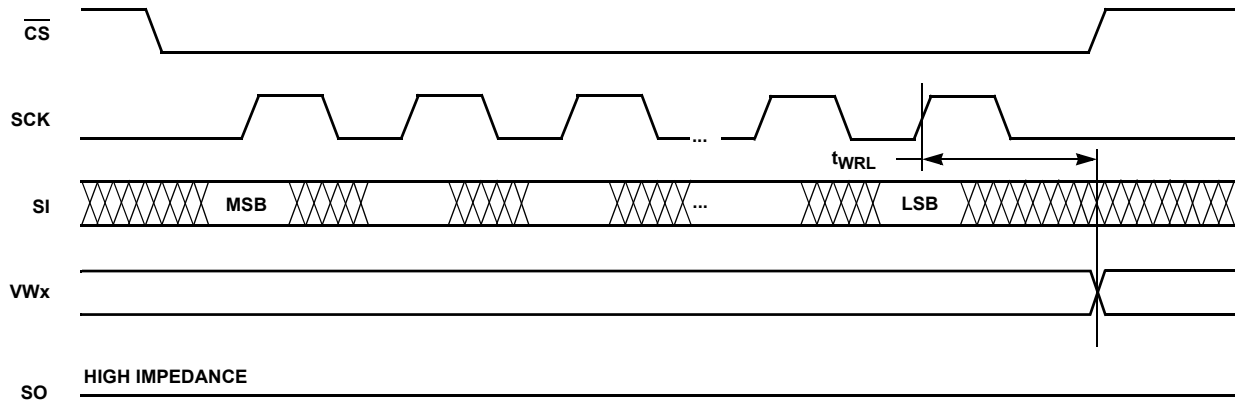
### Output Timing



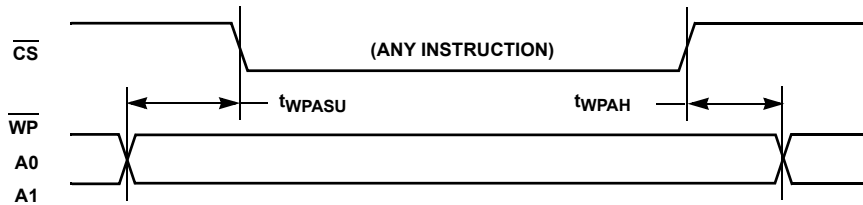
### Hold Timing



### XDCP Timing (for All Load Instructions)



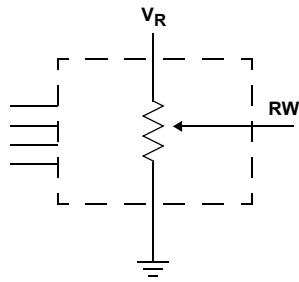
### Write Protect and Device Address Pins Timing



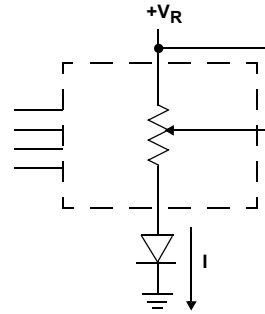


# Applications information

## Basic Configurations of Electronic Potentiometers



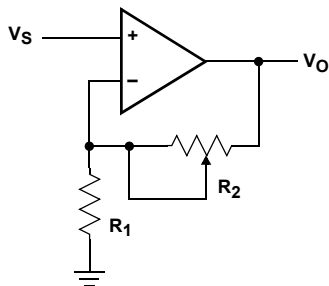
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

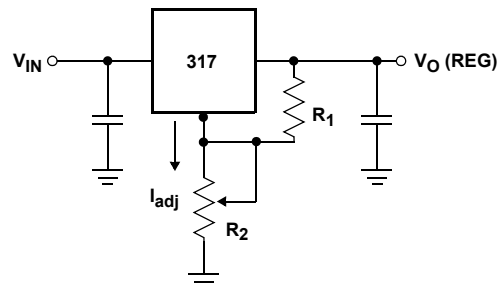
## Application Circuits

### NON INVERTING AMPLIFIER



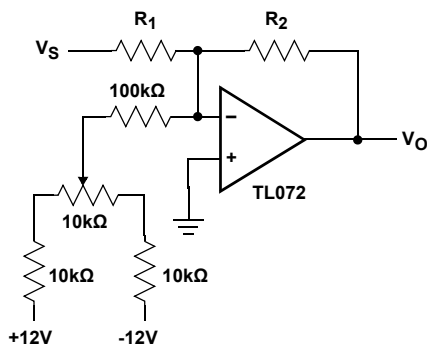
$$V_O = (1 + R_2/R_1)V_S$$

### VOLTAGE REGULATOR

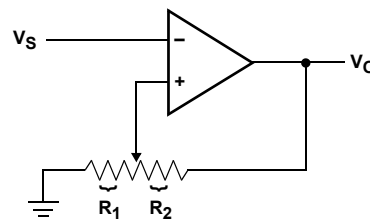


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

### OFFSET VOLTAGE ADJUSTMENT



### COMPARATOR WITH HYSTERESIS

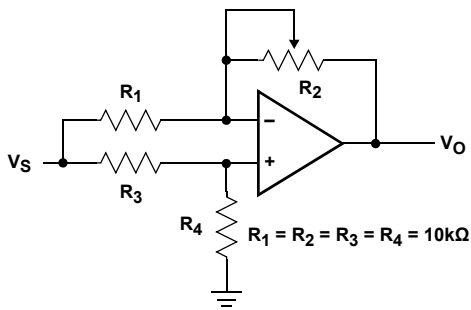


$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(\text{max})$$

$$R_{L} = \{R_1/(R_1 + R_2)\} V_O(\text{min})$$

**Application Circuits (continued)**

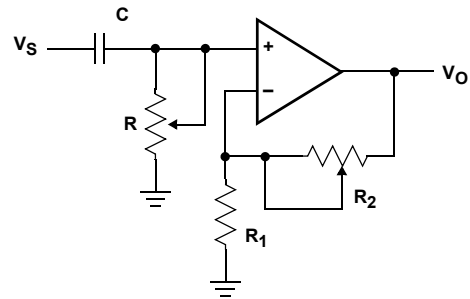
**ATTENUATOR**



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

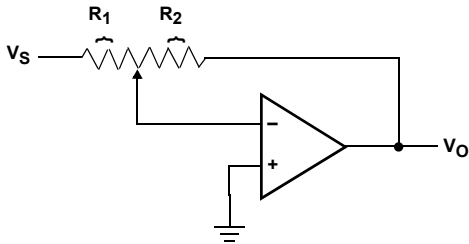
**FILTER**



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

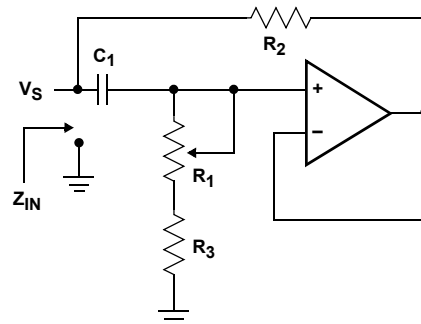
**INVERTING AMPLIFIER**



$$V_O = G V_S$$

$$G = -R_2/R_1$$

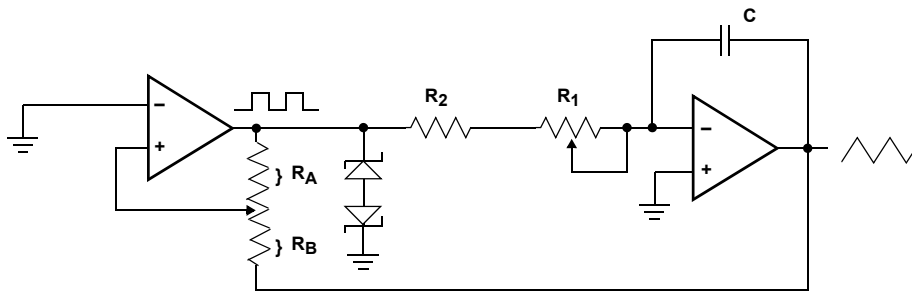
**EQUIVALENT L-R CIRCUIT**



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

**FUNCTION GENERATOR**



$$\text{FREQUENCY} \propto R_1, R_2, C$$

$$\text{AMPLITUDE} \propto R_A, R_B$$

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE             | REVISION | CHANGE   |
|------------------|----------|--|
| January 14, 2021 | FN8166.7 | Updated AC Timing table: the value of $T_1$ changed from 10ns (MAX) to 10ns (TYP).<br>Updated Ordering Information.<br>Removed about Intersil section.   |
| December 3, 2014 | FN8166.6 | Updated to Intersil new standards.<br>Updated Ordering Information Table on page 3, by removing obsoleted parts and 100k $\Omega$ referenced parts, adding Note 3 and changed TSSOP POD references from "MDP0044" to "M24.173".<br>Added Revision History and About Intersil verbiage.<br>Updated M24.3 POD to the latest revision.<br>-“Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing.<br>Added Land Pattern.”<br>Replaced MDP0044 POD with M24.173 POD to update to new format and only show 24 Ld version. |

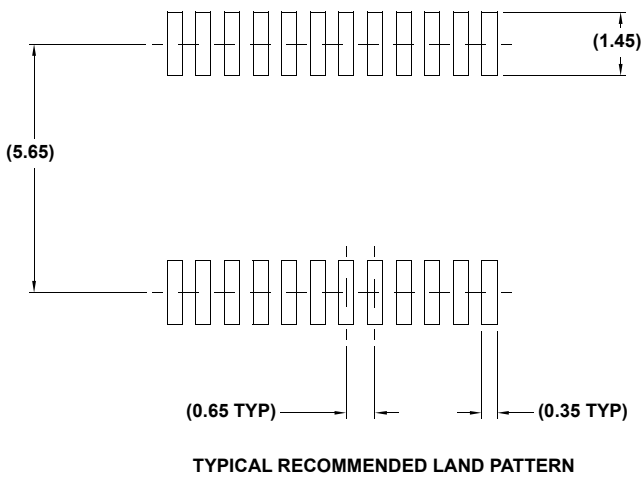
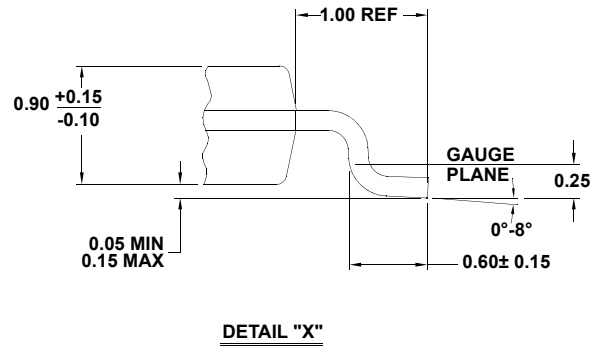
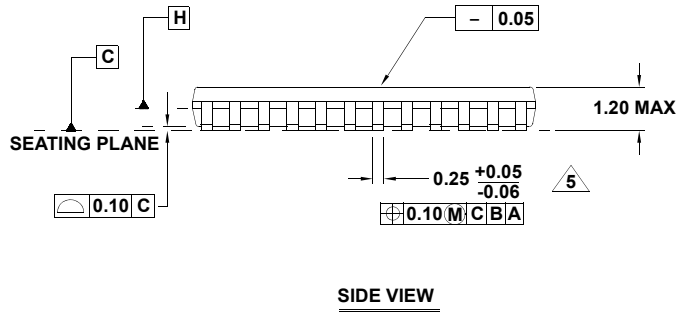
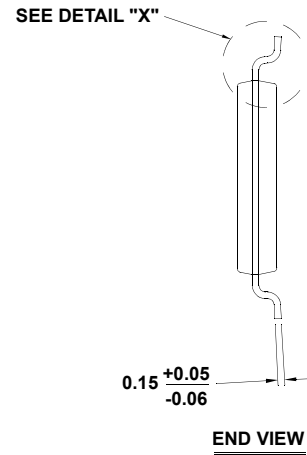
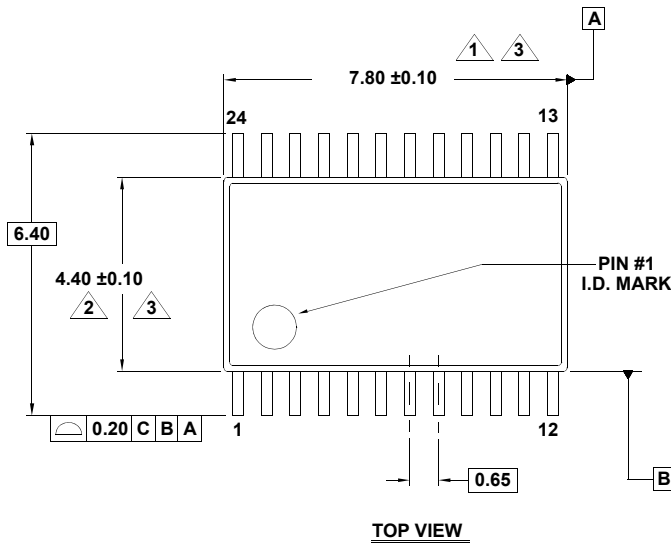
# Package Outline Drawing

For the most recent package outline drawing, see [M24.173](#).

## M24.173

24 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

Rev 1, 5/10



**NOTES:**

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.