

Summary

The Xilinx[®] Automotive (XA) Spartan[®]-3E family of FPGAs is specifically designed to meet the needs of high-volume, cost-sensitive automotive electronics applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, as shown in [Table 1](#).

Introduction

XA devices are available in both extended-temperature Q-Grade (–40°C to +125°C T_J) and I-Grade (–40°C to +100°C T_J) and are qualified to the industry recognized AEC-Q100 standard.

The XA Spartan-3E family builds on the success of the earlier XA Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These XA Spartan-3E FPGA enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, XA Spartan-3E FPGAs are ideally suited to a wide range of automotive applications, including infotainment, driver information, and driver assistance modules.

The XA Spartan-3E family is a superior alternative to mask programmed ASICs and ASSPs. FPGAs avoid the high initial mask set costs and lengthy development cycles, while also permitting design upgrades in the field with no hardware replacement necessary because of its inherent programmability, an impossibility with conventional ASICs and ASSPs with their inflexible hardware architecture.

Features

- Very low-cost, high-performance logic solution for high-volume automotive applications
- Proven advanced 90-nanometer process technology
- Multi-voltage, multi-standard SelectIO[™] interface pins
 - Up to 376 I/O pins or 156 differential signal pairs
 - LVCMOS, LVTTTL, HSTL, and SSTL single-ended signal standards
 - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
 - 622+ Mb/s data transfer rate per I/O
 - True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O

- Enhanced Double Data Rate (DDR) support
- DDR SDRAM support up to 266 Mb/s
- Abundant, flexible logic resources
 - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
 - Efficient wide multiplexers, wide logic
 - Fast look-ahead carry logic
 - Enhanced 18 x 18 multipliers with optional pipeline
 - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM[™] memory architecture
 - Up to 648 Kbits of fast block RAM
 - Up to 231 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
 - Clock skew elimination (delay locked loop)
 - Frequency synthesis, multiplication, division
 - High-resolution phase shifting
 - Wide frequency range (5 MHz to over 300 MHz)
- Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
 - Low-cost, space-saving SPI serial Flash PROM
 - x8 or x8/x16 parallel NOR Flash PROM
- Complete Xilinx [ISE](#)[®] and [WebPACK](#)[™] software support
- [MicroBlaze](#)[™] and [PicoBlaze](#)[™] embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI[™] technology support
- Low-cost QFP and BGA packaging options
 - Common footprints support easy density migration

Refer to Spartan-3E FPGA Family: Complete Data Sheet ([DS312](#)) for a full product description, AC and DC specifications, and package pinout descriptions. Any values shown specifically in this XA Spartan-3E Automotive FPGA Family data sheet override those shown in DS312.

For information regarding reliability qualification, refer to RPT081 (Xilinx Spartan-3E Family Automotive Qualification Report) and RPT012 (Spartan-3/3E UMC-12A 90 nm Qualification Report).

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specification over the $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ temperature range (Q-Grade)
- XA Spartan-3E devices are available in the -4 speed grade only.
- PCI-66 is not supported in the XA Spartan-3E FPGA product line.
- The readback feature is not supported in the XA Spartan-3E FPGA product line.
- XA Spartan-3E devices are available in Step 1 only.
- JTAG configuration frequency reduced from 30 MHz to 25 MHz.
- Platform Flash is not supported within the XA family.
- XA Spartan-3E devices are available in Pb-free packaging only.
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3E device must be power cycled prior to reconfiguration.

Table 1: Summary of XA Spartan-3E FPGA Attributes

| Device | System Gates | Equivalent Logic Cells | CLB Array (One CLB = Four Slices) | | | | Distributed RAM bits ⁽¹⁾ | Block RAM bits ⁽¹⁾ | Dedicated Multipliers | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|-----------|--------------|------------------------|--------------------------------------|---------|------------|--------------|-------------------------------------|-------------------------------|-----------------------|------|------------------|--------------------------------|
| | | | Rows | Columns | Total CLBs | Total Slices | | | | | | |
| XA3S100E | 100K | 2,160 | 22 | 16 | 240 | 960 | 15K | 72K | 4 | 2 | 108 | 40 |
| XA3S250E | 250K | 5,508 | 34 | 26 | 612 | 2,448 | 38K | 216K | 12 | 4 | 172 | 68 |
| XA3S500E | 500K | 10,476 | 46 | 34 | 1,164 | 4,656 | 73K | 360K | 20 | 4 | 190 | 77 |
| XA3S1200E | 1200K | 19,512 | 60 | 46 | 2,168 | 8,672 | 136K | 504K | 28 | 8 | 304 | 124 |
| XA3S1600E | 1600K | 33,192 | 76 | 58 | 3,688 | 14,752 | 231K | 648K | 36 | 8 | 376 | 156 |

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Architectural Overview

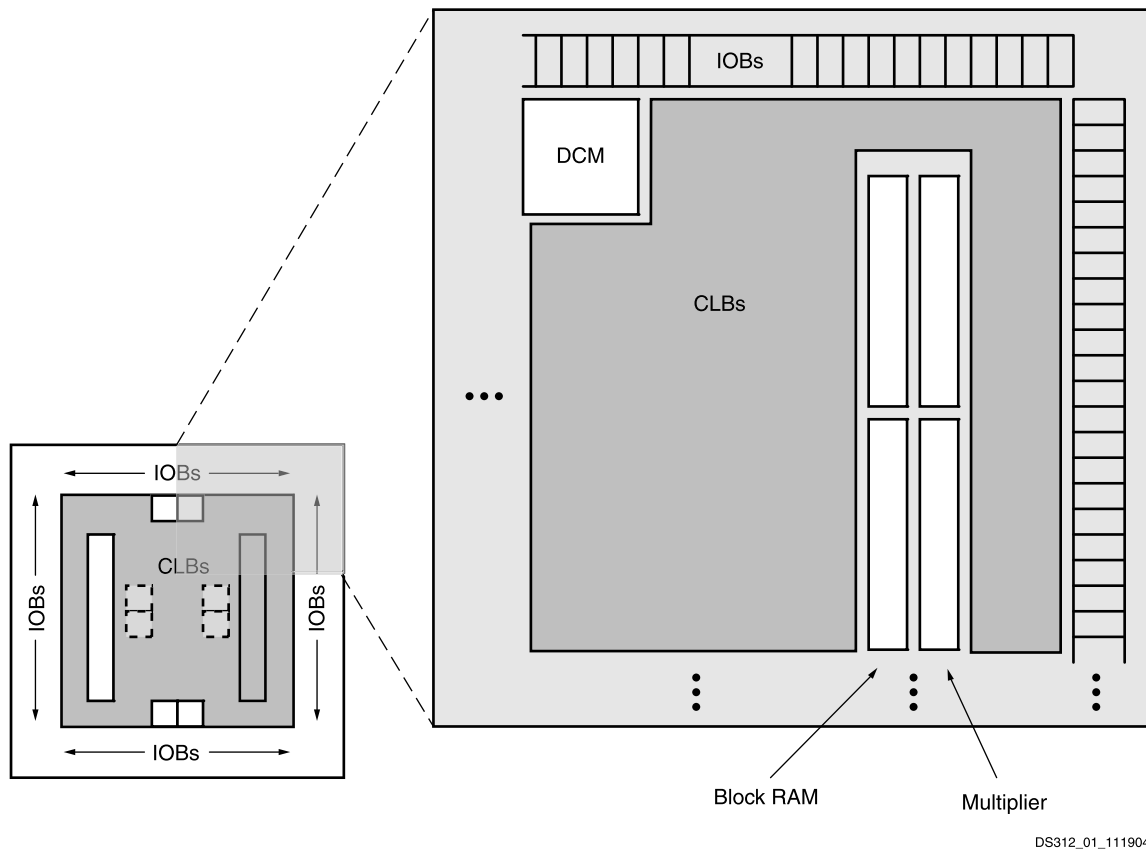
The XA Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.

- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XA3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XA3S100E has only one DCM at the top and bottom, while the XA3S1200E and XA3S1600E add two DCMs in the middle of the left and right sides.

The XA Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



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Notes:

1. The XA3S1200E and XA3S1600E have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XA3S100E has only one DCM at the top and one at the bottom.

Figure 1: XA Spartan-3E Family Architecture

Configuration

XA Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

I/O Capabilities

The XA Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 2](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

XA Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: Available User I/Os and Differential (Diff) I/O Pairs

| Package | VQG100 | | CPG132 | | TQG144 | | PQG208 | | FTG256 | | FGG400 | | FGG484 | |
|-----------|-------------------------|-------------------------|--------------------------|-------------------------|---------------------------|-------------------------|---------------------------|-------------------------|---------------------------|-------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| Size (mm) | 16 x 16 | | 8 x 8 | | 22 x 22 | | 28 x 28 | | 17 x 17 | | 21 x 21 | | 23 x 23 | |
| Device | User | Diff | User | Diff | User | Diff | User | Diff | User | Diff | User | Diff | User | Diff |
| XA3S100E | 66 <i>(7)</i> | 30 <i>(2)</i> | 83 <i>(11)</i> | 35 <i>(2)</i> | 108 <i>(28)</i> | 40 <i>(4)</i> | - | - | - | - | - | - | - | - |
| XA3S250E | 66 <i>(7)</i> | 30 <i>(2)</i> | 92 <i>(7)</i> | 41 <i>(2)</i> | 108 <i>(28)</i> | 40 <i>(4)</i> | 158 <i>(32)</i> | 65 <i>(5)</i> | 172 <i>(40)</i> | 68 <i>(8)</i> | - | - | - | - |
| XA3S500E | - | - | 92 <i>(7)</i> | 41 <i>(2)</i> | - | - | 158 <i>(32)</i> | 65 <i>(5)</i> | 190 <i>(41)</i> | 77 <i>(8)</i> | - | - | - | - |
| XA3S1200E | - | - | - | - | - | - | - | - | 190 <i>(40)</i> | 77 <i>(8)</i> | 304 <i>(72)</i> | 124 <i>(20)</i> | - | - |
| XA3S1600E | - | - | - | - | - | - | - | - | - | - | 304 <i>(72)</i> | 124 <i>(20)</i> | 376 <i>(82)</i> | 156 <i>(21)</i> |

Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of [DS312](#).
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *italics* indicates the number of input-only pins.

Package Marking

Figure 2 provides a top marking example for XA Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for XA Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CPG132). The markings for the BGA packages are nearly identical to those

for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for XA Spartan-3E FPGAs in the CPG132 package.

Note: No marking is shown for stepping.



Figure 2: XA Spartan-3E FPGA QFP Package Marking Example



Figure 3: XA Spartan-3E FPGA BGA Package Marking Example



Figure 4: XA Spartan-3E FPGA CPG132 Package Marking Example

Ordering Information

XA Spartan-3E FPGAs are available in Pb-free packaging options for all device/package combinations. All devices are in Pb-free packages only, with a “G” character to the ordering code. All devices are available in either I-Grade or

Q-Grade temperature ranges. Only the -4 speed grade is available for the XA Spartan-3E family. See [Table 2](#) for valid device/package combinations.

Pb-Free Packaging



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| Device | Speed Grade | Package Type / Number of Pins | Temperature Range (T_J) |
|-----------|-------------|---|--|
| XA3S100E | -4 Only | VQG100 100-pin Very Thin Quad Flat Pack (VQFP) | I I-Grade (-40°C to 100°C) |
| XA3S250E | | CPG132 132-ball Chip-Scale Package (CSP) | Q Q-Grade (-40°C to 125°C) |
| XA3S500E | | TQG144 144-pin Thin Quad Flat Pack (TQFP) | |
| XA3S1200E | | PQG208 208-pin Plastic Quad Flat Pack (PQFP) | |
| XA3S1600E | | FTG256 256-ball Fine-Pitch Thin Ball Grid Array (FTBGA) | |
| | | FGG400 400-ball Fine-Pitch Ball Grid Array (FBGA) | |
| | | FGG484 484-ball Fine-Pitch Ball Grid Array (FBGA) | |

Power Supply Specifications

Table 3: Supply Voltage Thresholds for Power-On Reset

| Symbol | Description | Min | Max | Units |
|--------------|---|-----|-----|-------|
| V_{CCINTT} | Threshold for the V_{CCINT} supply | 0.4 | 1.0 | V |
| V_{CCAUXT} | Threshold for the V_{CCAUX} supply | 0.8 | 2.0 | V |
| V_{CCO2T} | Threshold for the V_{CCO} Bank 2 supply | 0.4 | 1.0 | V |

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: Supply Voltage Ramp Rate

| Symbol | Description | Min | Max | Units |
|--------------|---|-----|-----|-------|
| V_{CCINTR} | Ramp rate from GND to valid V_{CCINT} supply level | 0.2 | 50 | ms |
| V_{CCAUXR} | Ramp rate from GND to valid V_{CCAUX} supply level | 0.2 | 50 | ms |
| V_{CCO2R} | Ramp rate from GND to valid V_{CCO} Bank 2 supply level | 0.2 | 50 | ms |

Notes:

- V_{CCINT} , V_{CCAUX} , and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
- To ensure successful power-on, V_{CCINT} , V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: Supply Voltage Levels Necessary for Preserving RAM Contents

| Symbol | Description | Min | Units |
|-------------|---|-----|-------|
| V_{DRINT} | V_{CCINT} level required to retain RAM data | 1.0 | V |
| V_{DRAUX} | V_{CCAUX} level required to retain RAM data | 2.0 | V |

Notes:

- RAM contents include configuration data.

DC Specifications

Table 6: General Recommended Operating Conditions

| Symbol | Description | | Min | Nominal | Max | Units |
|--------------------------|--|---|-------|---------|-------------------|-------|
| T_J | Junction temperature | I-Grade | -40 | 25 | 100 | °C |
| | | Q-Grade | -40 | 25 | 125 | °C |
| V_{CCINT} | Internal supply voltage | | 1.140 | 1.200 | 1.260 | V |
| $V_{CCO}^{(1)}$ | Output driver supply voltage | | 1.100 | - | 3.465 | V |
| V_{CCAUX} | Auxiliary supply voltage | | 2.375 | 2.500 | 2.625 | V |
| $\Delta V_{CCAUX}^{(2)}$ | Voltage variance on V_{CCAUX} when using a DCM | | - | - | 10 | mV/ms |
| $V_{IN}^{(3,4,5,6)}$ | Input voltage extremes to avoid turning on I/O protection diodes | I/O, Input-only, and Dual-Purpose pins ⁽³⁾ | -0.5 | - | $V_{CCO} + 0.5$ | V |
| | | Dedicated pins ⁽⁴⁾ | -0.5 | - | $V_{CCAUX} + 0.5$ | V |
| T_{IN} | Input signal transition time ⁽⁷⁾ | | - | - | 500 | ns |

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 9 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 11 lists that specific to the differential standards.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. See Absolute Maximum Ratings in DS312.
4. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
5. Input voltages outside the recommended range is permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. See Absolute Maximum Ratings in DS312.
6. See XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins."
7. Measured between 10% and 90% V_{CCO} . Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 7: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|-----------------|---|--|-------|-----|-------|------------|
| I_L | Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins | Driver is in a high-impedance state, $V_{IN} = 0V$ or V_{CCO} max, sample-tested | -10 | - | +10 | μA |
| $I_{RPU}^{(2)}$ | Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins | $V_{IN} = 0V, V_{CCO} = 3.3V$ | -0.36 | - | -1.24 | mA |
| | | $V_{IN} = 0V, V_{CCO} = 2.5V$ | -0.22 | - | -0.80 | mA |
| | | $V_{IN} = 0V, V_{CCO} = 1.8V$ | -0.10 | - | -0.42 | mA |
| | | $V_{IN} = 0V, V_{CCO} = 1.5V$ | -0.06 | - | -0.27 | mA |
| | | $V_{IN} = 0V, V_{CCO} = 1.2V$ | -0.04 | - | -0.22 | mA |
| $R_{PU}^{(2)}$ | Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2) | $V_{IN} = 0V, V_{CCO} = 3.0V$ to $3.465V$ | 2.4 | - | 10.8 | k Ω |
| | | $V_{IN} = 0V, V_{CCO} = 2.3V$ to $2.7V$ | 2.7 | - | 11.8 | k Ω |
| | | $V_{IN} = 0V, V_{CCO} = 1.7V$ to $1.9V$ | 4.3 | - | 20.2 | k Ω |
| | | $V_{IN} = 0V, V_{CCO} = 1.4V$ to $1.6V$ | 5.0 | - | 25.9 | k Ω |
| | | $V_{IN} = 0V, V_{CCO} = 1.14V$ to $1.26V$ | 5.5 | - | 32.0 | k Ω |

Table 7: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins (Continued)

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|-----------------|---|---|------|-----|------|------------|
| $I_{RPD}^{(2)}$ | Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins | $V_{IN} = V_{CCO}$ | 0.10 | – | 0.75 | mA |
| $R_{PD}^{(2)}$ | Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2) | $V_{IN} = V_{CCO} = 3.0V$ to 3.45V | 4.0 | – | 34.5 | k Ω |
| | | $V_{IN} = V_{CCO} = 2.3V$ to 2.7V | 3.0 | – | 27.0 | k Ω |
| | | $V_{IN} = V_{CCO} = 1.7V$ to 1.9V | 2.3 | – | 19.0 | k Ω |
| | | $V_{IN} = V_{CCO} = 1.4V$ to 1.6V | 1.8 | – | 16.0 | k Ω |
| | | $V_{IN} = V_{CCO} = 1.14V$ to 1.26V | 1.5 | – | 12.6 | k Ω |
| I_{REF} | V_{REF} current per pin | All V_{CCO} levels | –10 | – | +10 | μA |
| C_{IN} | Input capacitance | - | – | – | 10 | pF |
| R_{DT} | Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs. | $V_{OCM\ Min} \leq V_{ICM} \leq V_{OCM\ Max}$ $V_{OD\ Min} \leq V_{ID} \leq V_{OD\ Max}$ $V_{CCO} = 2.5V$ | – | 120 | – | Ω |

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPD}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Table 8: Quiescent Supply Current Characteristics

| Symbol | Description | Device | I-Grade Maximum | Q-Grade Maximum | Units |
|--------------|--------------------------------------|-----------|-----------------|-----------------|-------|
| I_{CCINTQ} | Quiescent V_{CCINT} supply current | XA3S100E | 36 | 58 | mA |
| | | XA3S250E | 104 | 158 | mA |
| | | XA3S500E | 145 | 300 | mA |
| | | XA3S1200E | 324 | 500 | mA |
| | | XA3S1600E | 457 | 750 | mA |
| I_{CCOQ} | Quiescent V_{CCO} supply current | XA3S100E | 1.5 | 2.0 | mA |
| | | XA3S250E | 1.5 | 3.0 | mA |
| | | XA3S500E | 1.5 | 3.0 | mA |
| | | XA3S1200E | 2.5 | 4.0 | mA |
| | | XA3S1600E | 2.5 | 4.0 | mA |

Table 8: Quiescent Supply Current Characteristics (Continued)

| Symbol | Description | Device | I-Grade Maximum | Q-Grade Maximum | Units |
|--------------|--------------------------------------|-----------|-----------------|-----------------|-------|
| I_{CCAUXQ} | Quiescent V_{CCAUX} supply current | XA3S100E | 13 | 22 | mA |
| | | XA3S250E | 26 | 43 | mA |
| | | XA3S500E | 34 | 63 | mA |
| | | XA3S1200E | 59 | 100 | mA |
| | | XA3S1600E | 86 | 150 | mA |

Notes:

1. The numbers in this table are based on the conditions set forth in [Table 6](#).
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at $V_{CCINT} = 1.2$ V, $V_{CCO} = 3.3$ V, and $V_{CCAUX} = 2.5$ V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with $V_{CCINT} = 1.26$ V, $V_{CCO} = 3.465$ V, and $V_{CCAUX} = 2.625$ V. The FPGA is programmed with a “blank” configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx XPower tools.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The [Spartan-3E XPower Estimator](#) provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

Single-Ended I/O Standards

Table 9: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

| IOSTANDARD Attribute | V _{CCO} for Drivers ⁽²⁾ | | | V _{REF} | | | V _{IL} | V _{IH} |
|----------------------------|---|---------|---------|--|---------|---------|--------------------------|--------------------------|
| | Min (V) | Nom (V) | Max (V) | Min (V) | Nom (V) | Max (V) | Max (V) | Min (V) |
| LVTTL | 3.0 | 3.3 | 3.465 | V _{REF} is not used for these I/O standards | | | 0.8 | 2.0 |
| LVC MOS33 ⁽⁴⁾ | 3.0 | 3.3 | 3.465 | | | | 0.8 | 2.0 |
| LVC MOS25 ^(4,5) | 2.3 | 2.5 | 2.7 | | | | 0.7 | 1.7 |
| LVC MOS18 | 1.65 | 1.8 | 1.95 | | | | 0.4 | 0.8 |
| LVC MOS15 | 1.4 | 1.5 | 1.6 | | | | 0.4 | 0.8 |
| LVC MOS12 | 1.1 | 1.2 | 1.3 | | | | 0.4 | 0.7 |
| PCI33_3 | 3.0 | 3.3 | 3.465 | | | | 0.3 * V _{CCO} | 0.5 * V _{CCO} |
| HSTL_I_18 | 1.7 | 1.8 | 1.9 | 0.8 | 0.9 | 1.1 | V _{REF} - 0.1 | V _{REF} + 0.1 |
| HSTL_III_18 | 1.7 | 1.8 | 1.9 | - | 1.1 | - | V _{REF} - 0.1 | V _{REF} + 0.1 |
| SSTL18_I | 1.7 | 1.8 | 1.9 | 0.833 | 0.900 | 0.969 | V _{REF} - 0.125 | V _{REF} + 0.125 |
| SSTL2_I | 2.3 | 2.5 | 2.7 | 1.15 | 1.25 | 1.35 | V _{REF} - 0.125 | V _{REF} + 0.125 |

Notes:

- Descriptions of the symbols used in this table are as follows:
V_{CCO} – the supply voltage for output drivers
V_{REF} – the reference voltage for setting the input switching threshold
V_{IL} – the input voltage that indicates a Low logic level
V_{IH} – the input voltage that indicates a High logic level
- The V_{CCO} rails supply only output drivers, not input circuits.
- For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72 in DS312.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVC MOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVC MOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see www.xilinx.com/pci.

Table 10: DC Characteristics of User I/Os Using Single-Ended Standards

| IOSTANDARD Attribute | Test Conditions | | | Logic Level Characteristics | |
|-------------------------|----------------------|----------------------|-------------------------|-----------------------------|------------------------|
| | I _{OL} (mA) | I _{OH} (mA) | V _{OL} Max (V) | V _{OH} Min (V) | |
| LVTTL ⁽³⁾ | 2 | 2 | -2 | 0.4 | 2.4 |
| | 4 | 4 | -4 | | |
| | 6 | 6 | -6 | | |
| | 8 | 8 | -8 | | |
| | 12 | 12 | -12 | | |
| | 16 | 16 | -16 | | |
| LVCMOS33 ⁽³⁾ | 2 | 2 | -2 | 0.4 | V _{CCO} - 0.4 |
| | 4 | 4 | -4 | | |
| | 6 | 6 | -6 | | |
| | 8 | 8 | -8 | | |
| | 12 | 12 | -12 | | |
| | 16 | 16 | -16 | | |
| LVCMOS25 ⁽³⁾ | 2 | 2 | -2 | 0.4 | V _{CCO} - 0.4 |
| | 4 | 4 | -4 | | |
| | 6 | 6 | -6 | | |
| | 8 | 8 | -8 | | |
| | 12 | 12 | -12 | | |
| LVCMOS18 ⁽³⁾ | 2 | 2 | -2 | 0.4 | V _{CCO} - 0.4 |
| | 4 | 4 | -4 | | |
| | 6 | 6 | -6 | | |
| | 8 | 8 | -8 | | |
| LVCMOS15 ⁽³⁾ | 2 | 2 | -2 | 0.4 | V _{CCO} - 0.4 |
| | 4 | 4 | -4 | | |
| | 6 | 6 | -6 | | |

Table 10: DC Characteristics of User I/Os Using Single-Ended Standards (Continued)

| IOSTANDARD Attribute | Test Conditions | | Logic Level Characteristics | | |
|--------------------------|----------------------|----------------------|-----------------------------|-------------------------|------------------------|
| | I _{OL} (mA) | I _{OH} (mA) | V _{OL} Max (V) | V _{OH} Min (V) | |
| LVC MOS12 ⁽³⁾ | 2 | 2 | -2 | 0.4 | V _{CCO} - 0.4 |
| PCI33_3 ⁽⁴⁾ | 1.5 | -0.5 | 10% V _{CCO} | 90% V _{CCO} | |
| HSTL_I_18 | 8 | -8 | 0.4 | V _{CCO} - 0.4 | |
| HSTL_III_18 | 24 | -8 | 0.4 | V _{CCO} - 0.4 | |
| SSTL18_I | 6.7 | -6.7 | V _{TT} - 0.475 | V _{TT} + 0.475 | |
| SSTL2_I | 8.1 | -8.1 | V _{TT} - 0.61 | V _{TT} + 0.61 | |

Notes:

- The numbers in this table are based on the conditions set forth in [Table 6](#) and [Table 9](#).
- Descriptions of the symbols used in this table are as follows:
 I_{OL} — the output current condition under which V_{OL} is tested
 I_{OH} — the output current condition under which V_{OH} is tested
 V_{OL} — the output voltage that indicates a Low logic level
 V_{OH} — the output voltage that indicates a High logic level
 V_{CCO} — the supply voltage for output drivers
 V_{TT} — the voltage applied to a resistor termination
- For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
- Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci.

Differential I/O Standards

Table 11: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

| IOSTANDARD Attribute | V _{CCO} for Drivers ⁽¹⁾ | | | V _{ID} | | | V _{ICM} | | |
|--------------------------|---|---------|---------|-----------------|----------|----------|------------------|---------|---------|
| | Min (V) | Nom (V) | Max (V) | Min (mV) | Nom (mV) | Max (mV) | Min (V) | Nom (V) | Max (V) |
| LVDS_25 | 2.375 | 2.50 | 2.625 | 100 | 350 | 600 | 0.30 | 1.25 | 2.20 |
| BLVDS_25 | 2.375 | 2.50 | 2.625 | 100 | 350 | 600 | 0.30 | 1.25 | 2.20 |
| MINI_LVDS_25 | 2.375 | 2.50 | 2.625 | 200 | - | 600 | 0.30 | - | 2.2 |
| LVPECL_25 ⁽²⁾ | Inputs Only | | | 100 | 800 | 1000 | 0.5 | 1.2 | 2.0 |
| RSDS_25 | 2.375 | 2.50 | 2.625 | 100 | 200 | - | 0.3 | 1.20 | 1.4 |
| DIFF_HSTL_I_18 | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.8 | - | 1.1 |
| DIFF_HSTL_III_18 | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.8 | - | 1.1 |
| DIFF_SSTL18_I | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.7 | - | 1.1 |
| DIFF_SSTL2_I | 2.3 | 2.5 | 2.7 | 100 | - | - | 1.0 | - | 1.5 |

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

Table 12: DC Characteristics of User I/Os Using Differential Signal Standards

| IOSTANDARD Attribute | V _{OD} | | | ΔV _{OD} | | V _{OCM} | | | ΔV _{OCM} | | V _{OH} | V _{OL} |
|----------------------|-----------------|----------|----------|------------------|----------|------------------|---------|---------|-------------------|----------|-------------------------|-------------------------|
| | Min (mV) | Typ (mV) | Max (mV) | Min (mV) | Max (mV) | Min (V) | Typ (V) | Max (V) | Min (mV) | Max (mV) | Min (V) | Max (V) |
| LVDS_25 | 250 | 350 | 450 | - | - | 1.125 | - | 1.375 | - | - | - | - |
| BLVDS_25 | 250 | 350 | 450 | - | - | - | 1.20 | - | - | - | - | - |
| MINI_LVDS_25 | 300 | - | 600 | - | 50 | 1.0 | - | 1.4 | - | 50 | - | - |
| RSDS_25 | 100 | - | 400 | - | - | 1.1 | - | 1.4 | - | - | - | - |
| DIFF_HSTL_I_18 | - | - | - | - | - | - | - | - | - | - | V _{CCO} - 0.4 | 0.4 |
| DIFF_HSTL_III_18 | - | - | - | - | - | - | - | - | - | - | V _{CCO} - 0.4 | 0.4 |
| DIFF_SSTL18_I | - | - | - | - | - | - | - | - | - | - | V _{TT} + 0.475 | V _{TT} - 0.475 |
| DIFF_SSTL2_I | - | - | - | - | - | - | - | - | - | - | V _{TT} + 0.61 | V _{TT} - 0.61 |

Notes:

1. The numbers in this table are based on the conditions set forth in [Table 6](#), and [Table 11](#).
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in [Figure 5](#) below.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25



Figure 5: External Termination Resistors for BLVDS Transmitter and BLVDS Receiver

Switching Characteristics

I/O Timing

Table 13: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

| Symbol | Description | Conditions | Device | -4 Speed Grade | Units |
|------------------------------|---|--|-----------|----------------|-------|
| | | | | Max | |
| Clock-to-Output Times | | | | | |
| $T_{ICKOFDCM}$ | When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used. | LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, with DCM ⁽³⁾ | XA3S100E | 2.79 | ns |
| | | | XA3S250E | 3.45 | ns |
| | | | XA3S500E | 3.46 | ns |
| | | | XA3S1200E | 3.46 | ns |
| | | | XA3S1600E | 3.45 | ns |
| T_{ICKOF} | When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used. | LVCMOS25 ⁽²⁾ , 12mA output drive, Fast slew rate, without DCM | XA3S100E | 5.92 | ns |
| | | | XA3S250E | 5.43 | ns |
| | | | XA3S500E | 5.51 | ns |
| | | | XA3S1200E | 5.94 | ns |
| | | | XA3S1600E | 6.05 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, add the appropriate Input adjustment from Table 17. If the latter is true, add the appropriate Output adjustment from Table 18.
3. DCM output jitter is included in all measurements.
4. For minimums, use the values reported by the Xilinx timing analyzer.

Table 14: Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)

| Symbol | Description | Conditions | IFD_DELAY_VALUE= | Device | -4 Speed Grade | Units | |
|--------------------|--|--|------------------|-----------|----------------|-------|----|
| | | | | | Min | | |
| Setup Times | | | | | | | |
| T _{PSDCM} | When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed. | LVCMOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0, with DCM ⁽⁴⁾ | 0 | XA3S100E | 2.98 | ns | |
| | | | | XA3S250E | 2.59 | ns | |
| | | | | XA3S500E | 2.59 | ns | |
| | | | | XA3S1200E | 2.58 | ns | |
| | | | | XA3S1600E | 2.59 | ns | |
| T _{PSFD} | When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed. | LVCMOS25 ⁽²⁾ , IFD_DELAY_VALUE = default software setting | 2 | XA3S100E | 3.58 | ns | |
| | | | | 3 | XA3S250E | 3.91 | ns |
| | | | | 2 | XA3S500E | 4.02 | ns |
| | | | | 5 | XA3S1200E | 5.52 | ns |
| | | | | 4 | XA3S1600E | 4.46 | ns |
| Hold Times | | | | | | | |
| T _{PHDCM} | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed. | LVCMOS25 ⁽³⁾ , IFD_DELAY_VALUE = 0, with DCM ⁽⁴⁾ | 0 | XA3S100E | -0.52 | ns | |
| | | | | XA3S250E | 0.14 | ns | |
| | | | | XA3S500E | 0.14 | ns | |
| | | | | XA3S1200E | 0.15 | ns | |
| | | | | XA3S1600E | 0.14 | ns | |
| T _{PHFD} | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed. | LVCMOS25 ⁽³⁾ , IFD_DELAY_VALUE = default software setting | 2 | XA3S100E | -0.24 | ns | |
| | | | | 3 | XA3S250E | -0.32 | ns |
| | | | | 2 | XA3S500E | -0.49 | ns |
| | | | | 5 | XA3S1200E | -0.63 | ns |
| | | | | 4 | XA3S1600E | -0.39 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 17. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 17. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 15: Setup and Hold Times for the IOB Input Path

| Symbol | Description | Conditions | IFD_DELAY_VALUE | Device | -4 Speed Grade | Units |
|------------------------------|---|---|-----------------|-----------|----------------------|-------|
| | | | | | Min | |
| Setup Times | | | | | | |
| T _{IOPICK} | Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed. | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0 | 0 | All | 2.12 | ns |
| T _{IOPICKD} | Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed. | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = default software setting | 2 | XA3S100E | 6.49 | ns |
| | | | 3 | XA3S250E | 6.85 | ns |
| | | | 2 | XA3S500E | 7.01 | ns |
| | | | 5 | XA3S1200E | 8.67 | ns |
| | | | 4 | XA3S1600E | 7.69 | ns |
| Hold Times | | | | | | |
| T _{IOICKP} | Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed. | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0 | 0 | All | -0.76 | ns |
| T _{IOICKPD} | Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed. | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = default software setting | 2 | XA3S100E | -3.93 | ns |
| | | | 3 | XA3S250E | -3.51 | ns |
| | | | 2 | XA3S500E | -3.74 | ns |
| | | | 5 | XA3S1200E | -4.30 | ns |
| | | | 4 | XA3S1600E | -4.14 | ns |
| Set/Reset Pulse Width | | | | | | |
| T _{RPW_IOB} | Minimum pulse width to SR control input on IOB | | | All | 1.80 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 19](#) and are based on the operating conditions set forth in [Table 6](#) and [Table 9](#).
2. This setup time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from [Table 17](#).
3. These hold times require adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from [Table 17](#). When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 16: Propagation Times for the IOB Input Path

| Symbol | Description | Conditions | IFD_DELAY_VALUE | Device | -4 Speed Grade | Units |
|--------------------------|---|--|-----------------|-----------|----------------|-------|
| | | | | | Max | |
| Propagation Times | | | | | | |
| T _{IOPLI} | The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0 | 0 | All | 2.25 | ns |
| T _{IOPLID} | The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed | LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = default software setting | 2 | XA3S100E | 5.97 | ns |
| | | | 3 | XA3S250E | 6.33 | ns |
| | | | 2 | XA3S500E | 6.49 | ns |
| | | | 5 | XA3S1200E | 8.15 | ns |
| | | | 4 | XA3S1600E | 7.16 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This propagation time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. When this is true, add the appropriate Input adjustment from Table 17.

Table 17: Input Timing Adjustments by IOSTANDARD

| Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | Units |
|---|--------------------------|-------|
| | -4 Speed Grade | |
| Single-Ended Standards | | |
| LVTTTL | 0.43 | ns |
| LVC MOS33 | 0.43 | ns |
| LVC MOS25 | 0 | ns |
| LVC MOS18 | 0.98 | ns |
| LVC MOS15 | 0.63 | ns |
| LVC MOS12 | 0.27 | ns |
| PCI33_3 | 0.42 | ns |
| HSTL_I_18 | 0.12 | ns |
| HSTL_III_18 | 0.17 | ns |
| SSTL18_I | 0.30 | ns |
| SSTL2_I | 0.15 | ns |

Table 17: Input Timing Adjustments by IOSTANDARD

| Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | Units |
|---|--------------------------|-------|
| | -4 Speed Grade | |
| Differential Standards | | |
| LVDS_25 | 0.49 | ns |
| BLVDS_25 | 0.39 | ns |
| MINI_LVDS_25 | 0.49 | ns |
| LVPECL_25 | 0.27 | ns |
| RSDS_25 | 0.49 | ns |
| DIFF_HSTL_I_18 | 0.49 | ns |
| DIFF_HSTL_III_18 | 0.49 | ns |
| DIFF_SSTL18_I | 0.30 | ns |
| DIFF_SSTL2_I | 0.32 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert input path times originally specified for the LVC MOS25 standard to times that correspond to other signal standards.

Table 18: Output Timing Adjustments for IOB

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below | Units | | |
|---|-------|-----------|--------------------------|-------|----|--|
| | | | -4 Speed Grade | | | |
| Single-Ended Standards | | | | | | |
| LVTTTL | Slow | 2 mA | 5.41 | ns | | |
| | | 4 mA | 2.41 | ns | | |
| | | 6 mA | 1.90 | ns | | |
| | | 8 mA | 0.67 | ns | | |
| | | 12 mA | 0.70 | ns | | |
| | | 16 mA | 0.43 | ns | | |
| | | 2 mA | 5.00 | ns | | |
| | Fast | 4 mA | 1.96 | ns | | |
| | | 6 mA | 1.45 | ns | | |
| | | 8 mA | 0.34 | ns | | |
| | | 12 mA | 0.30 | ns | | |
| | | 16 mA | 0.30 | ns | | |
| | | LVC MOS33 | | | | |
| | | Slow | 2 mA | 5.29 | ns | |
| 4 mA | 1.89 | | ns | | | |
| 6 mA | 1.04 | | ns | | | |
| 8 mA | 0.69 | | ns | | | |
| 12 mA | 0.42 | | ns | | | |
| 16 mA | 0.43 | | ns | | | |
| Fast | 2 mA | | 4.87 | ns | | |
| | 4 mA | | 1.52 | ns | | |
| | 6 mA | | 0.39 | ns | | |
| | 8 mA | | 0.34 | ns | | |
| | 12 mA | 0.30 | ns | | | |
| | 16 mA | 0.30 | ns | | | |
| LVC MOS25 | | | | | | |
| Slow | 2 mA | 4.21 | ns | | | |
| | 4 mA | 2.26 | ns | | | |
| | 6 mA | 1.52 | ns | | | |
| | 8 mA | 1.08 | ns | | | |
| | 12 mA | 0.68 | ns | | | |
| | Fast | 2 mA | 3.67 | ns | | |
| | | 4 mA | 1.72 | ns | | |
| | | 6 mA | 0.46 | ns | | |
| | | 8 mA | 0.21 | ns | | |
| | | 12 mA | 0 | ns | | |

Table 18: Output Timing Adjustments for IOB (Continued)

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | | | Add the Adjustment Below | Units |
|---|------|------|--------------------------|-------|
| | | | -4 Speed Grade | |
| LVC MOS18 | Slow | 2 mA | 5.24 | ns |
| | | 4 mA | 3.21 | ns |
| | | 6 mA | 2.49 | ns |
| | | 8 mA | 1.90 | ns |
| | Fast | 2 mA | 4.15 | ns |
| | | 4 mA | 2.13 | ns |
| | | 6 mA | 1.14 | ns |
| | | 8 mA | 0.75 | ns |
| LVC MOS15 | | | | |
| Slow | 2 mA | 4.68 | ns | |
| | 4 mA | 3.97 | ns | |
| | 6 mA | 3.11 | ns | |
| | Fast | 2 mA | 3.38 | ns |
| | | 4 mA | 2.70 | ns |
| | | 6 mA | 1.53 | ns |
| LVC MOS12 | | | | |
| Slow | 2 mA | 6.63 | ns | |
| Fast | 2 mA | 4.44 | ns | |
| HSTL_I_18 | | | 0.34 | ns |
| HSTL_III_18 | | | 0.55 | ns |
| PCI33_3 | | | 0.46 | ns |
| SSTL18_I | | | 0.25 | ns |
| SSTL2_I | | | -0.20 | ns |
| Differential Standards | | | | |
| LVDS_25 | | | -0.55 | ns |
| BLVDS_25 | | | 0.04 | ns |
| MINI_LVDS_25 | | | -0.56 | ns |
| LVPECL_25 | | | Input Only | ns |
| RSDS_25 | | | -0.48 | ns |
| DIFF_HSTL_I_18 | | | 0.42 | ns |
| DIFF_HSTL_III_18 | | | 0.55 | ns |
| DIFF_SSTL18_I | | | 0.40 | ns |
| DIFF_SSTL2_I | | | 0.44 | ns |

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVC MOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Table 19: Test Methods for Timing Measurement at I/Os

| Signal Standard (IOSTANDARD) | Inputs | | | Outputs | | Inputs and Outputs |
|---------------------------------|---------------|-------------------|-------------------|--------------------|-----------|-----------------------|
| | V_{REF} (V) | V_L (V) | V_H (V) | R_T (Ω) | V_T (V) | V_M (V) |
| Single-Ended | | | | | | |
| LVTTTL | - | 0 | 3.3 | 1M | 0 | 1.4 |
| LVCNOS33 | - | 0 | 3.3 | 1M | 0 | 1.65 |
| LVCNOS25 | - | 0 | 2.5 | 1M | 0 | 1.25 |
| LVCNOS18 | - | 0 | 1.8 | 1M | 0 | 0.9 |
| LVCNOS15 | - | 0 | 1.5 | 1M | 0 | 0.75 |
| LVCNOS12 | - | 0 | 1.2 | 1M | 0 | 0.6 |
| PCI33_3 | Rising | Note 3 | Note 3 | 25 | 0 | 0.94 |
| | Falling | | | 25 | 3.3 | 2.03 |
| HSTL_I_18 | 0.9 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 0.9 | V_{REF} |
| HSTL_III_18 | 1.1 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 1.8 | V_{REF} |
| SSTL18_I | 0.9 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 0.9 | V_{REF} |
| SSTL2_I | 1.25 | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | 50 | 1.25 | V_{REF} |
| Differential | | | | | | |
| LVDS_25 | - | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50 | 1.2 | V_{ICM} |
| BLVDS_25 | - | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 1M | 0 | V_{ICM} |
| MINI_LVDS_25 | - | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50 | 1.2 | V_{ICM} |
| LVPECL_25 | - | $V_{ICM} - 0.3$ | $V_{ICM} + 0.3$ | 1M | 0 | V_{ICM} |
| RSDS_25 | - | $V_{ICM} - 0.1$ | $V_{ICM} + 0.1$ | 50 | 1.2 | V_{ICM} |
| DIFF_HSTL_I_18 | - | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 0.9 | V_{ICM} |
| DIFF_HSTL_III_18 | - | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 1.8 | V_{ICM} |
| DIFF_SSTL18_I | - | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 0.9 | V_{ICM} |
| DIFF_SSTL2_I | - | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | 50 | 1.25 | V_{ICM} |

Notes:

- Descriptions of the relevant symbols are as follows:
 V_{REF} – The reference voltage for setting the input switching threshold
 V_{ICM} – The common mode input voltage
 V_M – Voltage of measurement point on signal transition
 V_L – Low-level test voltage at Input pin
 V_H – High-level test voltage at Input pin
 R_T – Effective termination resistance, which takes on a value of 1M Ω when no parallel termination is required
 V_T – Termination voltage
- The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
- According to the PCI specification.

Configurable Logic Block Timing

Table 20: CLB (SLICEM) Timing

| Symbol | Description | -4 Speed Grade | | Units |
|------------------------------|---|----------------|------|-------|
| | | Min | Max | |
| Clock-to-Output Times | | | | |
| T_{CKO} | When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output | - | 0.60 | ns |
| Setup Times | | | | |
| T_{AS} | Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB | 0.52 | - | ns |
| T_{DICK} | Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB | 1.81 | - | ns |
| Hold Times | | | | |
| T_{AH} | Time from the active transition at the CLK input to the point where data is last held at the F or G input | 0 | - | ns |
| T_{CKDI} | Time from the active transition at the CLK input to the point where data is last held at the BX or BY input | 0 | - | ns |
| Clock Timing | | | | |
| T_{CH} | The High pulse width of the CLB's CLK signal | 0.80 | - | ns |
| T_{CL} | The Low pulse width of the CLK signal | 0.80 | - | ns |
| F_{TOG} | Toggle frequency (for export control) | 0 | 572 | MHz |
| Propagation Times | | | | |
| T_{ILO} | The time it takes for data to travel from the CLB's F (G) input to the X (Y) output | - | 0.76 | ns |
| Set/Reset Pulse Width | | | | |
| T_{RPW_CLB} | The minimum allowable pulse width, High or Low, to the CLB's SR input | 1.80 | - | ns |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).

Table 21: CLB Distributed RAM Switching Characteristics

| Symbol | Description | -4 | | Units |
|------------------------------|---|------|------|-------|
| | | Min | Max | |
| Clock-to-Output Times | | | | |
| T_{SHCKO} | Time from the active edge at the CLK input to data appearing on the distributed RAM output | - | 2.35 | ns |
| Setup Times | | | | |
| T_{DS} | Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM | 0.46 | - | ns |
| T_{AS} | Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM | 0.52 | - | ns |
| T_{WS} | Setup time of the write enable input before the active transition at the CLK input of the distributed RAM | 0.40 | - | ns |
| Hold Times | | | | |
| T_{DH} | Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM | 0.15 | - | ns |
| T_{AH}, T_{WH} | Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM | 0 | - | ns |
| Clock Pulse Width | | | | |
| T_{WPH}, T_{WPL} | Minimum High or Low pulse width at CLK input | 1.01 | - | ns |

Table 22: CLB Shift Register Switching Characteristics

| Symbol | Description | -4 | | Units |
|------------------------------|--|------|------|-------|
| | | Min | Max | |
| Clock-to-Output Times | | | | |
| T_{REG} | Time from the active edge at the CLK input to data appearing on the shift register output | - | 4.16 | ns |
| Setup Times | | | | |
| T_{SRLDS} | Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register | 0.46 | - | ns |
| Hold Times | | | | |
| T_{SRLDH} | Hold time of the BX or BY data input after the active transition at the CLK input of the shift register | 0.16 | - | ns |
| Clock Pulse Width | | | | |
| T_{WPH}, T_{WPL} | Minimum High or Low pulse width at CLK input | 1.01 | - | ns |

Clock Buffer/Multiplexer Switching Characteristics

Table 23: Clock Distribution Switching Characteristics

| Description | Symbol | Maximum | Units |
|---|------------|----------------|-------|
| | | -4 Speed Grade | |
| Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay | T_{GIO} | 1.46 | ns |
| Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input | T_{GSI} | 0.63 | ns |
| Frequency of signals distributed on global buffers (all sides) | F_{BUFG} | 311 | MHz |

18 x 18 Embedded Multiplier Timing

Table 24: 18 x 18 Embedded Multiplier Timing

| Symbol | Description | -4 Speed Grade | | Units |
|----------------------------------|--|----------------|---------------------|-------|
| | | Min | Max | |
| Combinatorial Delay | | | | |
| T_{MULT} | Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused) | - | 4.88 ⁽¹⁾ | ns |
| Clock-to-Output Times | | | | |
| T_{MSCKP_P} | Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ⁽²⁾ | - | 1.10 | ns |
| T_{MSCKP_A} T_{MSCKP_B} | Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ⁽³⁾ | - | 4.97 | ns |
| Setup Times | | | | |
| T_{MSDCK_P} | Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽²⁾ | 3.98 | - | ns |
| T_{MSDCK_A} | Data setup time at the A input before the active transition at the CLK when using the AREG input register ⁽³⁾ | 0.23 | - | ns |
| T_{MSDCK_B} | Data setup time at the B input before the active transition at the CLK when using the BREG input register ⁽³⁾ | 0.39 | - | ns |
| Hold Times | | | | |
| T_{MSCKD_P} | Data hold time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽²⁾ | -0.97 | | |
| T_{MSCKD_A} | Data hold time at the A input before the active transition at the CLK when using the AREG input register ⁽³⁾ | 0.04 | | |
| T_{MSCKD_B} | Data hold time at the B input before the active transition at the CLK when using the BREG input register ⁽³⁾ | 0.05 | | |

Table 24: 18 x 18 Embedded Multiplier Timing (Continued)

| Symbol | Description | -4 Speed Grade | | Units |
|------------------------|---|----------------|-----|-------|
| | | Min | Max | |
| Clock Frequency | | | | |
| F_{MULT} | Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register ⁽¹⁾ | 0 | 240 | MHz |

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Block RAM Timing

Table 25: Block RAM Timing

| Symbol | Description | -4 Speed Grade | | Units |
|------------------------------|---|----------------|------|-------|
| | | Min | Max | |
| Clock-to-Output Times | | | | |
| T_{BCKO} | When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output | - | 2.82 | ns |
| Setup Times | | | | |
| T_{BACK} | Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM | 0.38 | - | ns |
| T_{BDCK} | Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM | 0.23 | - | ns |
| T_{BECK} | Setup time for the EN input before the active transition at the CLK input of the block RAM | 0.77 | - | ns |
| T_{BWCK} | Setup time for the WE input before the active transition at the CLK input of the block RAM | 1.26 | - | ns |
| Hold Times | | | | |
| T_{BCKA} | Hold time on the ADDR inputs after the active transition at the CLK input | 0.14 | - | ns |
| T_{BCKD} | Hold time on the DIN inputs after the active transition at the CLK input | 0.13 | - | ns |
| T_{BCKE} | Hold time on the EN input after the active transition at the CLK input | 0 | - | ns |
| T_{BCKW} | Hold time on the WE input after the active transition at the CLK input | 0 | - | ns |

Table 25: Block RAM Timing (Continued)

| Symbol | Description | -4 Speed Grade | | Units |
|------------------------|--|----------------|-----|-------|
| | | Min | Max | |
| Clock Timing | | | | |
| T_{BPWH} | High pulse width of the CLK signal | 1.59 | - | ns |
| T_{BPWL} | Low pulse width of the CLK signal | 1.59 | - | ns |
| Clock Frequency | | | | |
| F_{BRAM} | Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster. | 0 | 230 | MHz |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).

Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables ([Table 26](#) and [Table 27](#)) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables ([Table 28](#) through [Table 31](#)) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in [Table 26](#) and [Table 27](#).

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See [XAPP469](#), *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop

Table 26: Recommended Operating Conditions for the DLL

| Symbol | | Description | -4 Speed Grade | | Units |
|--|---|------------------------------------|------------------|--------------------|-------|
| | | | Min | Max | |
| Input Frequency Ranges | | | | | |
| F_{CLKIN} | CLKIN_FREQ_DLL | Frequency of the CLKIN clock input | 5 ⁽²⁾ | 240 ⁽³⁾ | MHz |
| Input Pulse Requirements | | | | | |
| CLKIN_PULSE | CLKIN pulse width as a percentage of the CLKIN period | $F_{\text{CLKIN}} \leq 150$ MHz | 40% | 60% | - |
| | | $F_{\text{CLKIN}} > 150$ MHz | 45% | 55% | - |
| Input Clock Jitter Tolerance and Delay Path Variation⁽⁴⁾ | | | | | |
| CLKIN_CYC_JITT_DLL_LF | Cycle-to-cycle jitter at the CLKIN input | $F_{\text{CLKIN}} \leq 150$ MHz | - | ±300 | ps |
| CLKIN_CYC_JITT_DLL_HF | | $F_{\text{CLKIN}} > 150$ MHz | - | ±150 | ps |
| CLKIN_PER_JITT_DLL | Period jitter at the CLKIN input | | - | ±1 | ns |
| CLKFB_DELAY_VAR_EXT | Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input | | - | ±1 | ns |

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See [Table 28](#).
3. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 27: Switching Characteristics for the DLL

| Symbol | | Description | -4 Speed Grade | | Units |
|--|--|--|----------------|-----------------------------|-------|
| | | | Min | Max | |
| Output Frequency Ranges | | | | | |
| CLKOUT_FREQ_CLK0 | | Frequency for the CLK0 and CLK180 outputs | 5 | 240 | MHz |
| CLKOUT_FREQ_CLK90 | | Frequency for the CLK90 and CLK270 outputs | 5 | 200 | MHz |
| CLKOUT_FREQ_2X | | Frequency for the CLK2X and CLK2X180 outputs | 10 | 311 | MHz |
| CLKOUT_FREQ_DV | | Frequency for the CLKDV output | 0.3125 | 160 | MHz |
| Output Clock Jitter^(2,3,4) | | | | | |
| CLKOUT_PER_JITT_0 | | Period jitter at the CLK0 output | - | ±100 | ps |
| CLKOUT_PER_JITT_90 | | Period jitter at the CLK90 output | - | ±150 | ps |
| CLKOUT_PER_JITT_180 | | Period jitter at the CLK180 output | - | ±150 | ps |
| CLKOUT_PER_JITT_270 | | Period jitter at the CLK270 output | - | ±150 | ps |
| CLKOUT_PER_JITT_2X | | Period jitter at the CLK2X and CLK2X180 outputs | - | ±[1% of CLKIN period + 150] | ps |
| CLKOUT_PER_JITT_DV1 | | Period jitter at the CLKDV output when performing integer division | - | ±150 | ps |
| CLKOUT_PER_JITT_DV2 | | Period jitter at the CLKDV output when performing non-integer division | - | ±[1% of CLKIN period + 200] | ps |

Table 27: Switching Characteristics for the DLL (Continued)

| Symbol | Description | -4 Speed Grade | | Units | |
|--------------------------------------|--|---|-----------------------------|-------|----|
| | | Min | Max | | |
| Duty Cycle⁽⁴⁾ | | | | | |
| CLKOUT_DUTY_CYCLE_DLL | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion | - | ±[1% of CLKIN period + 400] | ps | |
| Phase Alignment⁽⁴⁾ | | | | | |
| CLKIN_CLKFB_PHASE | Phase offset between the CLKIN and CLKFB inputs | - | ±200 | ps | |
| CLKOUT_PHASE_DLL | Phase offset between DLL outputs | CLK0 to CLK2X (not CLK2X180) | ±[1% of CLKIN period + 100] | ps | |
| | | All others | ±[1% of CLKIN period + 200] | ps | |
| Lock Time | | | | | |
| LOCK_DLL ⁽³⁾ | When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase | $5 \text{ MHz} \leq F_{\text{CLKIN}} \leq 15 \text{ MHz}$ | - | 5 | ms |
| | | $F_{\text{CLKIN}} > 15 \text{ MHz}$ | - | 600 | µs |
| Delay Lines | | | | | |
| DCM_DELAY_STEP | Finest delay resolution | 20 | 40 | ps | |

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 26.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. **Example:** The data sheet specifies a maximum jitter of “±[1% of CLKIN period + 150]”. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer

Table 28: Recommended Operating Conditions for the DFS

| Symbol | Description | -4 Speed Grade | | Units | |
|---|---|---|-------|--------------------|-----|
| | | Min | Max | | |
| Input Frequency Ranges⁽²⁾ | | | | | |
| F_{CLKIN} | CLKIN_FREQ_FX | Frequency for the CLKIN input | 0.200 | 333 ⁽⁴⁾ | MHz |
| Input Clock Jitter Tolerance⁽³⁾ | | | | | |
| CLKIN_CYC_JITT_FX_LF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency | $F_{\text{CLKFX}} \leq 150 \text{ MHz}$ | - | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | | $F_{\text{CLKFX}} > 150 \text{ MHz}$ | - | ±150 | ps |
| CLKIN_PER_JITT_FX | Period jitter at the CLKIN input | - | ±1 | ns | |

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 26.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 29: Switching Characteristics for the DFS

| Symbol | Description | Device | -4 Speed Grade | | Units | |
|--|---|--------|----------------|-----------------------------|-----------------------------|----|
| | | | Min | Max | | |
| Output Frequency Ranges | | | | | | |
| CLKOUT_FREQ_FX | Frequency for the CLKFX and CLKFX180 outputs | All | 5 | 311 | MHz | |
| Output Clock Jitter^(2,3) | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs | All | Typ | Max | | |
| | | | CLKIN ≤ 20 MHz | See Note 4 | | ps |
| | | | CLKIN > 20 MHz | ±[1% of CLKFX period + 100] | ±[1% of CLKFX period + 200] | ps |
| Duty Cycle^(5,6) | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion | All | - | ±[1% of CLKFX period + 400] | ps | |
| Phase Alignment⁽⁶⁾ | | | | | | |
| CLKOUT_PHASE_FX | Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used | All | - | ±200 | ps | |
| CLKOUT_PHASE_FX180 | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used | All | - | ±[1% of CLKFX period + 300] | ps | |
| Lock Time | | | | | | |
| LOCK_FX ⁽²⁾ | The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time. | All | - | 5 | ms | |
| | | | - | 450 | µs | |

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 6 and Table 28.
- For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI. **Example:** The data sheet specifies a maximum jitter of “±[1% of CLKFX period + 300]”. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.

Phase Shifter

Table 30: Recommended Operating Conditions for the PS in Variable Phase Mode

| Symbol | Description | -4 Speed Grade | | Units |
|-----------------------------------|---|----------------|-----|-------|
| | | Min | Max | |
| Operating Frequency Ranges | | | | |
| PSCLK_FREQ (FPSCLK) | Frequency for the PSCLK input | 1 | 167 | MHz |
| Input Pulse Requirements | | | | |
| PSCLK_PULSE | PSCLK pulse width as a percentage of the PSCLK period | 40% | 60% | - |

Table 31: Switching Characteristics for the PS in Variable Phase Mode

| Symbol | Description | | Units | |
|-----------------------------|--|--|--|-------|
| Phase Shifting Range | | | | |
| MAX_STEPS ⁽²⁾ | Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period. | CLKIN < 60 MHz | $\pm \lceil \text{INTEGER}(10 \bullet (T_{\text{CLKIN}} - 3 \text{ ns})) \rceil$ | steps |
| | | CLKIN \geq 60 MHz | $\pm \lceil \text{INTEGER}(15 \bullet (T_{\text{CLKIN}} - 3 \text{ ns})) \rceil$ | steps |
| FINE_SHIFT_RANGE_MIN | Minimum guaranteed delay for variable phase shifting | $\pm \lceil \text{MAX_STEPS} \bullet \text{DCM_DELAY_STEP_MIN} \rceil$ | | ns |
| FINE_SHIFT_RANGE_MAX | Maximum guaranteed delay for variable phase shifting | $\pm \lceil \text{MAX_STEPS} \bullet \text{DCM_DELAY_STEP_MAX} \rceil$ | | ns |

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 30.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 27.

Miscellaneous DCM Timing

Table 32: Miscellaneous DCM Timing

| Symbol | Description | Min | Max | Units |
|------------------------------------|--|-----|-----|--------------|
| DCM_RST_PW_MIN ⁽¹⁾ | Minimum duration of a RST pulse width | 3 | - | CLKIN cycles |
| DCM_RST_PW_MAX ⁽²⁾ | Maximum duration of a RST pulse width | N/A | N/A | seconds |
| | | N/A | N/A | seconds |
| DCM_CONFIG_LAG_TIME ⁽³⁾ | Maximum duration from V _{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL | N/A | N/A | minutes |
| | | N/A | N/A | minutes |

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specification. This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration and JTAG Timing

Table 33: Power-On Timing and the Beginning of Configuration

| Symbol | Description | Device | -4 Speed Grade | | Units |
|------------------|---|-----------|----------------|-----|---------|
| | | | Min | Max | |
| $T_{POR}^{(2)}$ | The time from the application of V_{CCINT} , V_{CCAUX} , and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin | XA3S100E | - | 5 | ms |
| | | XA3S250E | - | 5 | ms |
| | | XA3S500E | - | 5 | ms |
| | | XA3S1200E | - | 5 | ms |
| | | XA3S1600E | - | 7 | ms |
| T_{PROG} | The width of the low-going pulse on the PROG_B pin | All | 0.5 | - | μ s |
| $T_{PL}^{(2)}$ | The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin | XA3S100E | - | 0.5 | ms |
| | | XA3S250E | - | 0.5 | ms |
| | | XA3S500E | - | 1 | ms |
| | | XA3S1200E | - | 2 | ms |
| | | XA3S1600E | - | 2 | ms |
| T_{INIT} | Minimum Low pulse width on INIT_B output | All | 250 | - | ns |
| $T_{ICCK}^{(3)}$ | The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin | All | 0.5 | 4.0 | μ s |

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6. This means power must be applied to all V_{CCINT} , V_{CCO} , and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Configuration Clock (CCLK) Characteristics

Table 34: Master Mode CCLK Output Period by *ConfigRate* Option Setting

| Symbol | Description | <i>ConfigRate</i> Setting | Temperature Range | Minimum | Maximum | Units |
|---------------------|--|---|--------------------|---------|---------|-------|
| T _{CCLK1} | CCLK clock period by <i>ConfigRate</i> setting | 1 (power-on value and default value) | I-Grade Q-Grade | 485 | 1,250 | ns |
| T _{CCLK3} | | 3 | I-Grade Q-Grade | 242 | 625 | ns |
| T _{CCLK6} | | 6 | I-Grade Q-Grade | 121 | 313 | ns |
| T _{CCLK12} | | 12 | I-Grade Q-Grade | 60.6 | 157 | ns |
| T _{CCLK25} | | 25 | I-Grade Q-Grade | 30.3 | 78.2 | ns |
| T _{CCLK50} | | 50 | I-Grade Q-Grade | 15.1 | 39.1 | ns |

Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in [DS312](#), Module 2.

Table 35: Master Mode CCLK Output Frequency by *ConfigRate* Option Setting

| Symbol | Description | <i>ConfigRate</i> Setting | Temperature Range | Minimum | Maximum | Units |
|---------------------|--|---|--------------------|---------|---------|-------|
| F _{CCLK1} | Equivalent CCLK clock frequency by <i>ConfigRate</i> setting | 1 (power-on value and default value) | I-Grade Q-Grade | 0.8 | 2.1 | MHz |
| F _{CCLK3} | | 3 | I-Grade Q-Grade | 1.6 | 4.2 | MHz |
| F _{CCLK6} | | 6 | I-Grade Q-Grade | 3.2 | 8.3 | MHz |
| F _{CCLK12} | | 12 | I-Grade Q-Grade | 6.4 | 16.5 | MHz |
| F _{CCLK25} | | 25 | I-Grade Q-Grade | 12.8 | 33.0 | MHz |
| F _{CCLK50} | | 50 | I-Grade Q-Grade | 25.6 | 66.0 | MHz |

Table 36: Master Mode CCLK Output Minimum Low and High Time

| Symbol | Description | | <i>ConfigRate</i> Setting | | | | | | Units |
|--|--|--------------------|---------------------------|-----|----|------|------|-----|-------|
| | | | 1 | 3 | 6 | 12 | 25 | 50 | |
| T _{MCCL} , T _{MCCH} | Master mode CCLK minimum Low and High time | I-Grade Q-Grade | 235 | 117 | 58 | 29.3 | 14.5 | 7.3 | ns |

Table 37: Slave Mode CCLK Input Low and High Time

| Symbol | Description | Min | Max | Units |
|--|------------------------|-----|-----|-------|
| T _{SCCL} , T _{SCCH} | CCLK Low and High time | 5 | ∞ | ns |

Master Serial and Slave Serial Mode Timing

Table 38: Timing for the Master Serial and Slave Serial Configuration Modes

| Symbol | Description | Slave/ Master | -4 Speed Grade | | Units | |
|------------------------------|--|------------------|------------------------------|------|-------------------|-----|
| | | | Min | Max | | |
| Clock-to-Output Times | | | | | | |
| T_{CCO} | The time from the falling transition on the CCLK pin to data appearing at the DOUT pin | Both | 1.5 | 10.0 | ns | |
| Setup Times | | | | | | |
| T_{DCC} | The time from the setup of data at the DIN pin to the active edge of the CCLK pin | Both | 11.0 | - | ns | |
| Hold Times | | | | | | |
| T_{CCD} | The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin | Both | 0 | - | ns | |
| Clock Timing | | | | | | |
| T_{CCH} | High pulse width at the CCLK input pin | Master | See Table 36 | | | |
| | | Slave | See Table 37 | | | |
| T_{CCL} | Low pulse width at the CCLK input pin | Master | See Table 36 | | | |
| | | Slave | See Table 37 | | | |
| F_{CCSER} | Frequency of the clock signal at the CCLK input pin | Slave | No bitstream compression | 0 | 66 ⁽²⁾ | MHz |
| | | | With bitstream compression | 0 | 20 | MHz |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing

Table 39: Timing for the Slave Parallel Configuration Mode

| Symbol | Description | -4 Speed Grade | | Units | |
|------------------------------|--|----------------------------|---------------------------------------|-------|-----|
| | | Min | Max | | |
| Clock-to-Output Times | | | | | |
| T_{SMCKBY} | The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin | - | 12.0 | ns | |
| Setup Times | | | | | |
| T_{SMDCC} | The time from the setup of data at the D0-D7 pins to the active edge the CCLK pin | 11.0 | - | ns | |
| T_{SMCSCC} | Setup time on the CSI_B pin before the active edge of the CCLK pin | 10.0 | - | ns | |
| $T_{SMCCW}^{(2)}$ | Setup time on the RDWR_B pin before active edge of the CCLK pin | 23.0 | - | ns | |
| Hold Times | | | | | |
| T_{SMCCD} | The time from the active edge of the CCLK pin to the point when data is last held at the D0-D7 pins | 1.0 | - | ns | |
| T_{SMCCCS} | The time from the active edge of the CCLK pin to the point when a logic level is last held at the CSO_B pin | 0 | - | ns | |
| T_{SMWCC} | The time from the active edge of the CCLK pin to the point when a logic level is last held at the RDWR_B pin | 0 | - | ns | |
| Clock Timing | | | | | |
| T_{CCH} | The High pulse width at the CCLK input pin | | 5 | - | ns |
| T_{CCL} | The Low pulse width at the CCLK input pin | | 5 | - | ns |
| F_{CCPAR} | Frequency of the clock signal at the CCLK input pin | No bitstream compression | Not using the BUSY pin ⁽²⁾ | | MHz |
| | | | Using the BUSY pin | | |
| | | With bitstream compression | | 0 | 20 |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

Serial Peripheral Interface Configuration Timing

Table 40: Timing for SPI Configuration Mode

| Symbol | Description | Minimum | Maximum | Units |
|-------------|---|----------------|---------|-------|
| T_{CCLK1} | Initial CCLK clock period | (see Table 34) | | |
| T_{CCLKn} | CCLK clock period after FPGA loads ConfigRate setting | (see Table 34) | | |
| T_{MINIT} | Setup time on VS[2:0] and M[2:0] mode pins before the rising edge of INIT_B | 50 | - | ns |
| T_{INITM} | Hold time on VS[2:0] and M[2:0] mode pins after the rising edge of INIT_B | 0 | - | ns |
| T_{CCO} | MOSI output valid after CCLK edge | See Table 38 | | |
| T_{DCC} | Setup time on DIN data input before CCLK edge | See Table 38 | | |
| T_{CCD} | Hold time on DIN data input after CCLK edge | See Table 38 | | |

Table 41: Configuration Timing Requirements for Attached SPI Serial Flash

| Symbol | Description | Requirement | Units |
|----------------|--|--------------------------------------|-------|
| T_{CCS} | SPI serial Flash PROM chip-select time | $T_{CCS} \leq T_{MCCL1} - T_{CCO}$ | ns |
| T_{DSU} | SPI serial Flash PROM data input setup time | $T_{DSU} \leq T_{MCCL1} - T_{CCO}$ | ns |
| T_{DH} | SPI serial Flash PROM data input hold time | $T_{DH} \leq T_{MCCH1}$ | ns |
| T_V | SPI serial Flash PROM data clock-to-output time | $T_V \leq T_{MCCLn} - T_{DCC}$ | ns |
| f_C or f_R | Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used) | $f_C \geq \frac{1}{T_{CCLKn(\min)}}$ | MHz |

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface Configuration Timing

Table 42: Timing for BPI Configuration Mode

| Symbol | Description | Minimum | Maximum | Units | |
|----------------|--|------------------------------------|---------|-------|-----------------------|
| T_{CCLK1} | Initial CCLK clock period | (see Table 34) | | | |
| T_{CCLKn} | CCLK clock period after FPGA loads ConfigRate setting | (see Table 34) | | | |
| T_{MINIT} | Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B | 50 | - | ns | |
| T_{INITM} | Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B | 0 | - | ns | |
| $T_{INITADDR}$ | Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid | BPI-UP: (M[2:0]=<0:1:0>) | 5 | 5 | T_{CCLK1} cycles |
| | | BPI-DN: (M[2:0]=<0:1:1>) | 2 | 2 | |
| T_{CCO} | Address A[23:0] outputs valid after CCLK falling edge | See Table 38 | | | |
| T_{DCC} | Setup time on D[7:0] data inputs before CCLK rising edge | See Table 38 | | | |
| T_{CCD} | Hold time on D[7:0] data inputs after CCLK rising edge | See Table 38 | | | |

Table 43: Configuration Timing Requirements for Attached Parallel NOR Flash

| Symbol | Description | Requirement | Units |
|--|--|---|-------|
| T_{CE} (t_{ELQV}) | Parallel NOR Flash PROM chip-select time | $T_{CE} \leq T_{INITADDR}$ | ns |
| T_{OE} (t_{GLQV}) | Parallel NOR Flash PROM output-enable time | $T_{OE} \leq T_{INITADDR}$ | ns |
| T_{ACC} (t_{AVQV}) | Parallel NOR Flash PROM read access time | $T_{ACC} \leq 0.5T_{CCLKn(\min)} - T_{CCO} - T_{DCC} - PCB$ | ns |
| T_{BYTE} (t_{FLQV} , t_{FHQV}) | For x8/x16 PROMs only: BYTE# to output valid time ⁽³⁾ | $T_{BYTE} \leq T_{INITADDR}$ | ns |

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

IEEE 1149.1/1553 JTAG Test Access Port Timing

Table 44: Timing for the JTAG Test Access Port

| Symbol | Description | -4 Speed Grade | | Units |
|------------------------------|--|----------------|------|-------|
| | | Min | Max | |
| Clock-to-Output Times | | | | |
| T_{TCKTDO} | The time from the falling transition on the TCK pin to data appearing at the TDO pin | 1.0 | 11.0 | ns |
| Setup Times | | | | |
| T_{TDITCK} | The time from the setup of data at the TDI pin to the rising transition at the TCK pin | 7.0 | - | ns |
| T_{TMSTCK} | The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin | 7.0 | - | ns |
| Hold Times | | | | |
| T_{TCKTDI} | The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin | 0 | - | ns |
| T_{TCKTMS} | The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin | 0 | - | ns |
| Clock Timing | | | | |
| T_{CCH} | The High pulse width at the TCK pin | 5 | - | ns |
| T_{CCL} | The Low pulse width at the TCK pin | 5 | - | ns |
| F_{TCK} | Frequency of the TCK signal | - | 25 | MHz |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).

Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|---|
| 08/31/07 | 1.0 | Initial Xilinx release. |
| 01/20/09 | 1.1 | <ul style="list-style-type: none"> Updated "Key Feature Differences from Commercial XC Devices." Updated T_{ACC} requirement in Table 43. Updated description of T_{DCC} and T_{CCD} in Table 42. Removed Table 45: MultiBoot Trigger Timing. |
| 09/09/09 | 2.0 | <ul style="list-style-type: none"> Added package sizes to Table 2, page 4. Removed Genealogy Viewer Link from "Package Marking," page 5. Updated data and notes for Table 6, page 8. Updated test conditions for R_{PU} and maximum value for C_{IN} in Table 7, page 8. Updated notes for Table 8, page 9. Updated Max V_{CCO} for LVTTTL and LVCMOS33, removed PCIX data, updated V_{IL} Max for LVCMOS18, LVCMOS15, and LVCMOS12, updated V_{IH} Min for LVCMOS12, and added note 6 in Table 9, page 11. Removed PCIX data, revised note 2, and added note 4 in Table 10, page 12. Updated figure description of Figure 5, page 14. Added note 4 to Table 13, page 14. Removed PC166_3 and PCIX adjustment values from Table 17, page 17. Deleted Table 18 (duplicate of Table 17, page 17). Subsequent tables renumbered. Removed PCIX data Table 18, page 18. Removed PCIX data and removed V_{REF} values for DIFF_HSTL_I_18, DIFF_HSTL_III_18, DIFF_SSTL18_I, and DIFF_SSTL2_I from Table 19, page 19. Updated T_{DICK} minimum setup time in Table 20, page 20. Updated notes, references to notes, and revised the maximum clock-to-output times for T_{MSCKP_P} Table 24, page 22. Added "Spread Spectrum," page 24. Updated note 3 in Table 26, page 25. Added note 4 Table 28, page 26. Updated notes, references to notes, and CLKOUT_PER_JITT_FX data in Table 29, page 27. Updated MAX_STEPS data in Table 31, page 28. Updated ConfigRate Setting for T_{CCLK1} to indicate 1 is the default value in Table 34, page 30. Updated ConfigRate Setting for F_{CCLK1} to indicate 1 is the default value in Table 35, page 30. |

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