XA95144XL Automotive CPLD

DS600 (v1.1) April 3, 2007

Product Specification

Features

- AEC-Q100 device qualification and full PPAP support available in I-grade.
- Guaranteed to meet full electrical specifications over T_A = -40° C to +85° C (I-grade)
- 15.5 ns pin-to-pin logic delays
- System frequency up to 64.5 MHz
- 144 macrocells with 3,200 usable gates
- Available in the following package
  - 144-CSP (117 user I/O pins)
  - Pb-free package only
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS Fast FLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

WARNING: Programming temperature range of T_A = 0° C to +70° C

Description

The XA95144XL is a 3.3V CPLD targeted for high-performance, low-voltage automotive applications. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 15.5 ns. See Figure 2 for overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. Each macrocell in an XA9500XL automotive device must be configured for low-power mode (default mode for XA9500XL devices). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$I_{CC}(mA) = MC(0.052*PT + 0.272) + 0.04 * MC_{TOG} * MC * f$

where:

MC = # macrocells

PT = average number product terms per macrocell

f = maximum clock frequency

MC_{TOG} = average % of flip-flops toggling per clock (~12%)

This calculation was derived from laboratory measurements of an XA9500XL part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx application note **XAPP114, "Understanding XC9500XL CPLD Power."**

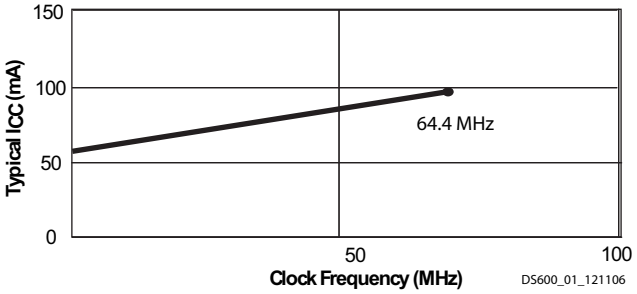


Figure 1: **Typical I_{CC} vs. Frequency for XA95144XL**

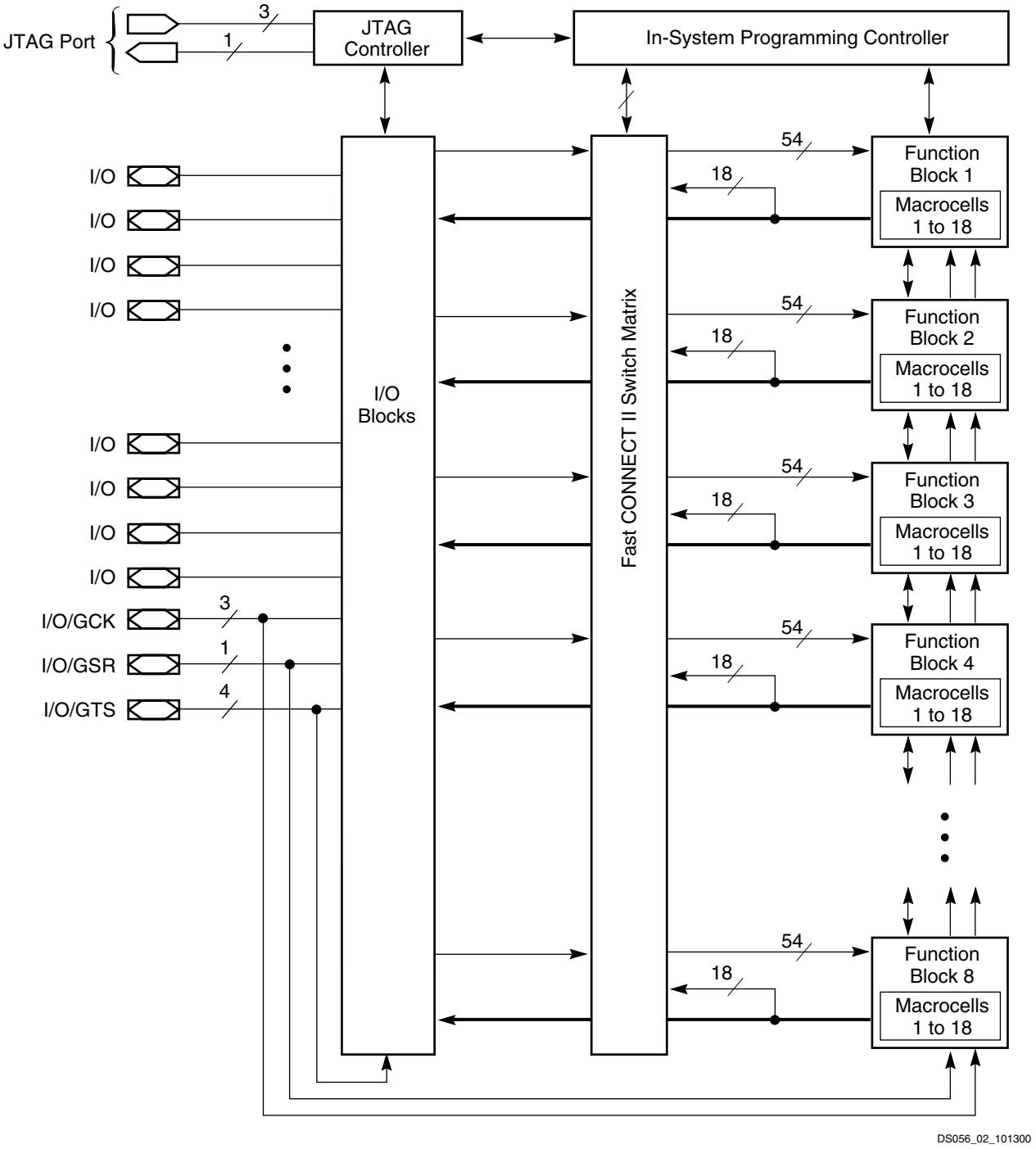


Figure 2: **XA95144XL Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings(1,3)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(2)	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output(2)	–0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)(4)	–65 to +150	°C
T_J	Junction temperature	+125	°C

Notes:

1. All automotive customers are required to set the Macrocell Power Setting to low, and set Logic Optimization to density.
2. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. External I/O voltage may not exceed V_{CCINT} by 4.0V.
3. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
4. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Recommended Operation Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient temperature	–40	+85	°C
V_{CCINT}	Supply voltage for internal logic and input buffers	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation	2.3	2.7	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance) @ T_A = 70°	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

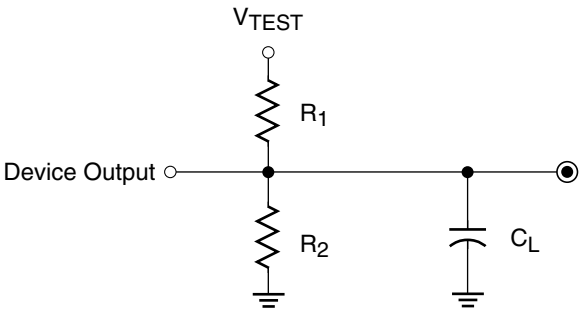
DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{CCIO} = Max; V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} Min < V_{IN} < 5.5V	-	±50	µA
C_{IN}	I/O capacitance	V_{IN} = GND; f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_{IN} = GND, No load; f = 1.0 MHz	45 (Typical)		mA

AC Characteristics

Symbol	Parameter	XA95144XL-15		Units
		Min	Max	
T_{PD}	I/O to output valid	-	15.5	ns
T_{SU}	I/O setup time before GCK	12.0	-	ns
T_{H}	I/O hold time after GCK	0	-	ns
T_{CO}	GCK to output valid	-	5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	64.5	MHz
T_{PSU}	I/O setup time before p-term clock input	7.6	-	ns
T_{PH}	I/O hold time after p-term clock input	0.0	-	ns
T_{PCO}	P-term clock output valid	-	10.2	ns
T_{OE}	GTS to output valid	-	7.0	ns
T_{OD}	GTS to output disable	-	7.0	ns
T_{POE}	Product term OE to output enabled	-	11.0	ns
T_{POD}	Product term OE to output disabled	-	11.0	ns
T_{AO}	GSR to output valid	-	14.5	ns
T_{PAO}	P-term S/R to output valid	-	15.3	ns
T_{WLH}	GCK pulse width (High or Low)	4.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	7.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	7.0	-	ns
T_{SUEC}	Clock enable setup	6.5	-	ns
T_{HEC}	Clock enable hold	0	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320 Ω	360 Ω	35 pF
	2.5V	2.5V	250 Ω	660 Ω	35 pF

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Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XA95144XL-15		Units
		Min	Max	
Buffer Delays				
T_{IN}	Input buffer delay	-	3.5	ns
T_{GCK}	GCK buffer delay	-	1.8	ns
T_{GSR}	GSR buffer delay	-	4.5	ns
T_{GTS}	GTS buffer delay	-	7.0	ns
T_{OUT}	Output buffer delay	-	3.0	ns
T_{EN}	Output buffer enable/disable delay	-	0	ns
Product Term Control Delays				
T_{PTCK}	Product term clock delay	-	2.7	ns
T_{PTSR}	Product term set/reset delay	-	1.8	ns
T_{PTTS}	Product term 3-state delay	-	7.5	ns
Internal Register and Combinatorial Delays				
T_{PDI}	Combinatorial logic propagation delay	-	1.7	ns
T_{SUI}	Register setup time	3.0	-	ns
T_{HI}	Register hold time	3.5	-	ns
T_{ECSU}	Register clock enable setup time	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.5	-	ns
T_{COI}	Register clock to output valid time	-	1.0	ns
T_{AOI}	Register async. S/R to output delay	-	7.0	ns
T_{RAI}	Register async. S/R recover before clock	10.0	-	ns
T_{LOGI}	Internal logic delay	-	7.3	ns
Feedback Delays				
T_F	Fast CONNECT II feedback delay	-	4.2	ns
Time Adders				
T_{PTA}	Incremental product term allocator delay	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	4.5	ns

XA95144XL I/O Pins

Function Block	Macrocell	CSG144	BScan Order
1	1	H3	429
1	2	F1	426
1	3	G2	423
1	4	J1	420
1	5	G3	417
1	6	G4	414
1	7	-	411
1	8	H1	408
1	9	H2	405
1	10	K3	402
1	11	H4	399
1	12	J2	396
1	13	-	393
1	14	J3	390
1	15	J4	387
1	16	M1	384
1	17(1)	K2(1)	381
1	18	-	378
2	1	C3	375
2	2(1)	A2(1)	372
2	3	-	369
2	4	C1	366
2	5(1)	B1(1)	363
2	6(1)	C2(1)	360
2	7	-	357
2	8(1)	D4(1)	354
2	9(1)	D3(1)	351
2	10	D2	348
2	11	E4	345
2	12	E3	342
2	13	E1	339
2	14	E2	336
2	15	F4	333
2	16	F3	330
2	17	F2	327
2	18	-	324
3	1	M3	321
3	2(1)	L1(1)	318
3	3	K4	315
3	4	N4	312
3	5	L2	309
3	6	L3	306
3	7	L5	303
3	8(1)	N2(1)	300
3	9	N3	297
3	10	N5	294
3	11	M4	291
3	12	K5	288
3	13	-	285
3	14	K6	282
3	15	L6	279
3	16	-	276
3	17	M6	273
3	18	-	270
4	1	C9	267
4	2	A7	264
4	3	A5	261
4	4	-	258
4	5	D7	255
4	6	A6	252
4	7	-	249
4	8	B6	246
4	9	C6	243
4	10	C5	240
4	11	D6	237
4	12	B5	234
4	13	A4	231
4	14	D5	228
4	15	B4	225
4	16	C4	222
4	17	A3	219
4	18	-	216

Notes:
1. Global control pin.

XA95144XL (Continued)

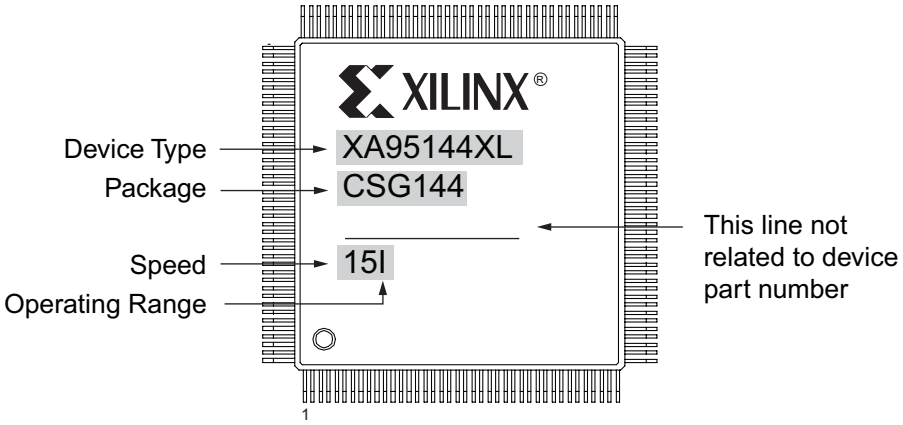
Function Block	Macrocell	CS144	BScan Order
5	1	-	213
5	2	N6	210
5	3	L8	207
5	4	-	204
5	5	M7	201
5	6	N7	198
5	7	M10	195
5	8	K7	192
5	9	N8	189
5	10	N11	186
5	11	M8	183
5	12	K8	180
5	13	L11	177
5	14	N9	174
5	15	K9	171
5	16	-	168
5	17	M11	165
5	18	-	162
6	1	-	159
6	2	C11	156
6	3	-	153
6	4	B11	150
6	5	A12	147
6	6	A11	144
6	7	-	141
6	8	D10	138
6	9	A10	135
6	10	B10	132
6	11	B9	129
6	12	A9	126
6	13	-	123
6	14	D8	120
6	15	A8	117
6	16	D9	114
6	17	B7	111
6	18	-	108

Function Block	Macrocell	CS144	BScan Order
7	1	-	105
7	2	N12	102
7	3	L12	99
7	4	-	96
7	5	M13	93
7	6	L13	90
7	7	K10	87
7	8	K11	84
7	9	K13	81
7	10	K12	78
7	11	J11	75
7	12	H10	72
7	13	J10	69
7	14	H11	66
7	15	H12	63
7	16	J12	60
7	17	H13	57
7	18	-	54
8	1	-	51
8	2	G11	48
8	3	F11	45
8	4	E13	42
8	5	G10	39
8	6	F13	36
8	7	-	33
8	8	F12	30
8	9	F10	27
8	10	D13	24
8	11	E12	21
8	12	E10	18
8	13	D11	15
8	14	D12	12
8	15	C13	9
8	16	B13	6
8	17	C12	3
8	18	-	0

XA95144XL Global, JTAG and Power Pins

Pin Type	CSG144
I/O/GCK1	K2
I/O/GCK2	L1
I/O/GCK3	N2
I/O/GTS1	D4
I/O/GTS2	D3
I/O/GTS3	B1
I/O/GTS4	C2
I/O/GSR	A2
TCK	L10
TDI	L9
TDO	C8
TMS	N10
V_{CCINT} 3.3V	B3, D1, J13, L4
V_{CCIO} 2.5V/3.3V	A1, A13, C7, L7, N1, N13
GND	B2, B8, B12, C10, E11, G1, G12, G13, K1, M2, M5, M9, M12
No Connects	–

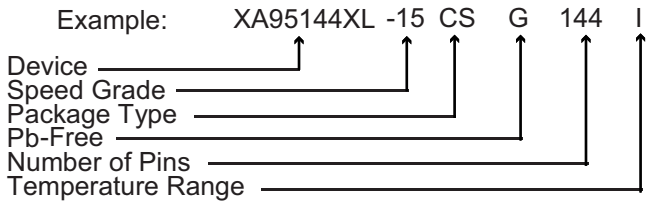
Device Part Marking and Ordering Combination Information.



Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XA95144XL-15CSG144I	15.5 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	I

Notes:
1. I-Grade: T_A = –40° to +85°C



XA9500XL Automotive Requirements and Recommendations

Requirements

The following requirements are for all automotive applications:

1. All automotive customers are required to keep the Macrocell Power selection set to low, and the Logic Optimization set to density when designing with ISE software. These are the default settings when XA9500XL devices are selected for design. These settings are found on the Process Properties page for Implement Design. See the ISE Online Help for details on these properties.
2. Use a monotonic, fast ramp power supply to power up XA9500XL . A V_{CC} ramp time of less than 1 ms is required.
3. Do not float I/O pins during device operation. Floating I/O pins can increase I_{CC} as input buffers will draw 1-2 mA per floating input. In addition, when I/O pins are floated, noise can propagate to the center of the CPLD. I/O pins should be appropriately terminated with keeper/bus-hold. Unused I/Os can also be configured as C_{GND} (programmable GND).
4. Do not drive I/O pins without V_{CC}/V_{CCIO} powered.
5. Sink current when driving LEDs. Because all Xilinx CPLDs have N-channel pull-down transistors on outputs, it is required that an LED anode is sourced through a resistor externally to V_{CC}. Consequently, this will give the brightest solution.
6. Avoid external pull-down resistors. Always use external pull-up resistors if external termination is required. This is because the XA9500XL Automotive CPLD, which includes some I/O driving circuits beyond the input and output buffers, may have contention with external pull-down resistors, and, consequently, the I/O will not switch as expected.
7. Do not drive I/Os pins above the V_{CCIO} assigned to its I/O bank.

a. The current flow can go into V_{CCIO} and affect a user voltage regulator.
b. It can also increase undesired leakage current associated with the device.
c. If done for too long, it can reduce the life of the device.

8. Do not rely on the I/O states before the CPLD configures.
9. Use a voltage regulator which can provide sufficient current during device power up. As a rule of thumb, the regulator needs to provide at least three times the peak current while powering up a CPLD in order to guarantee the CPLD can configure successfully.
10. Ensure external JTAG terminations for TMS, TCK, TDI, TDO comply with IEEE 1149.1. All Xilinx CPLDs have internal weak pull-ups of ~50 kΩ on TDI, TMS, and TCK.
11. Attach all CPLD V_{CC} and GND pins in order to have necessary power and ground supplies around the CPLD.
12. Decouple all V_{CC} and V_{CCIO} pins with capacitors of 0.01 µF and 0.1 µF closest to the pins for each V_{CC}/V_{CCIO}-GND pair.

Recommendations

The following recommendations are for all automotive applications.

1. Use strict synchronous design (only one clocking event) if possible. A synchronous system is more robust than an asynchronous one.
2. Include JTAG stakes on the PCB. JTAG stakes can be used to test the part on the PCB. They add benefit in reprogramming part on the PCB, inspecting chip internals with INTEST, identifying stuck pins, and inspecting programming patterns (if not secured).
3. XA9500XL Automotive CPLDs work with any power sequence, but it is preferable to power the V_{CCI} (internal V_{CC}) before the V_{CCIO} for the applications in which any glitches from device I/Os are unwanted.
4. Do not disregard report file warnings. Software identifies potential problems when compiling, so the report file is worth inspecting to see exactly how your design is mapped onto the logic.
5. Understand the Timing Report. This report file provides a speed summary along with warnings. Read the timing file (*.tim) carefully. Analyze key signal chains to determine limits to given clock(s) based on logic analysis.
6. Review Fitter Report equations. Equations can be shown in ABEL-like format, or can also be displayed in Verilog or VHDL formats. The Fitter Report also includes switch settings that are very informative of other device behaviors.
7. Let design software define pinouts if possible. Xilinx CPLD software works best when it selects the I/O pins and manages resources for users. It can spread signals around and improve pin-locking. If users must define pins, plan resources in advance.
8. Perform a post-fit simulation for all speeds to identify any possible problems (such as race conditions) that might occur when fast-speed silicon is used instead of slow-speed silicon.
9. Distribute SSOs (Simultaneously Switching Outputs) evenly around the CPLD to reduce switching noise.
10. Terminate high speed outputs to eliminate noise caused by very fast rising/falling edges.