

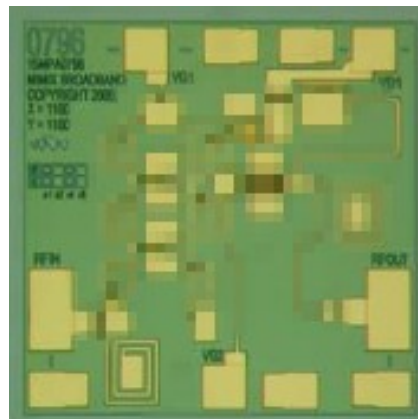
Features

- Excellent Transmit LO/Output Buffer Stage
- Compact Size
- 18.0 dB Small Signal Gain
- +20.0 dBm P1dB Compression Point
- 5.5 dB Noise Figure
- Variable Gain with Adjustable Bias
- 100% On-Wafer RF, DC & Output Power Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's two stage 10.0-21.0 GHz GaAs MMIC buffer amplifier has a small signal gain of 18.0 dB with a +20.0 dBm P1dB output compression point. The device also provides variable gain regulation with adjustable bias. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Microwave and Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 VDC
Supply Current (Id1)	180 mA
Gate Bias Voltage (Vg)	0 V
Input Power (Pin)	+20.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +85 °C
Channel Temperature (Tch)	175 °C

Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Ordering Information

Part Number	Package
XB1008-BD-000V	"V" - vacuum release gel paks
XB1008-BD-EV1	evaluation module

XB1008-BD



Buffer Amplifier
10.0-21.0 GHz

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Electrical Specifications: 10-21 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	15.0	-
Output Return Loss (S22)	dB	-	17.0	-
Small Signal Gain (S21)	dB	-	18.0	-
Gain Flatness (ΔS_{21})	dB	-	+/-2.0	-
Reverse Isolation (S12)	dB	-	35.0	-
Noise Figure (NF)	dB	-	5.5	-
Output Power for 1dB Compression Point (P1dB) ²	dBm	-	+20.0	-
Saturated Output Power (Psat)	dBm	-	+22.0	-
Drain Bias Voltage (Vd)	VDC	-	+4.0	+4.0
Gate Bias Voltage (Vg2)	VDC	-1.0	-0.23	-0.1
Supply Current (Id) (Vd=4.0 V, Vg2=-0.5 V Typical)	mA	-	100	130

2. Measured using constant current

XB1008-BD

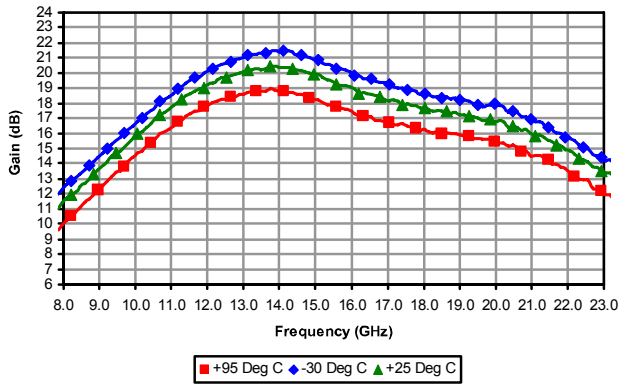


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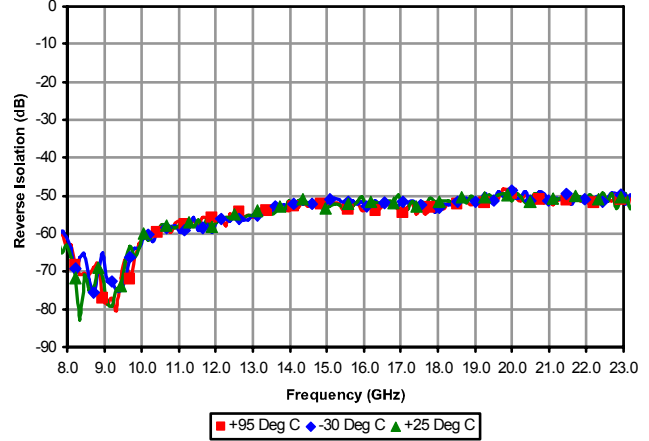
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Typical Performance Curves

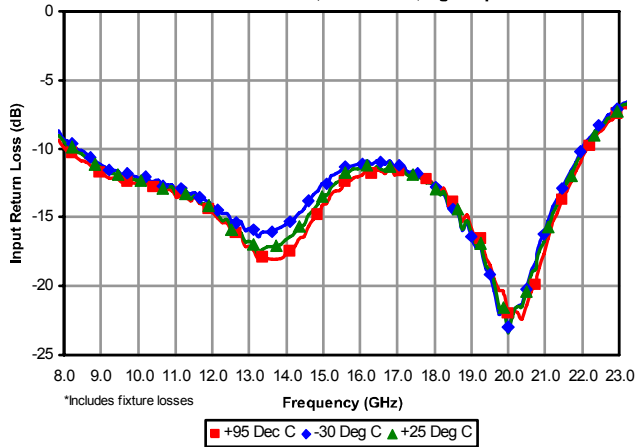
XB1008-BD Vd=4.0 V, Id=130 mA, Vg2=Open



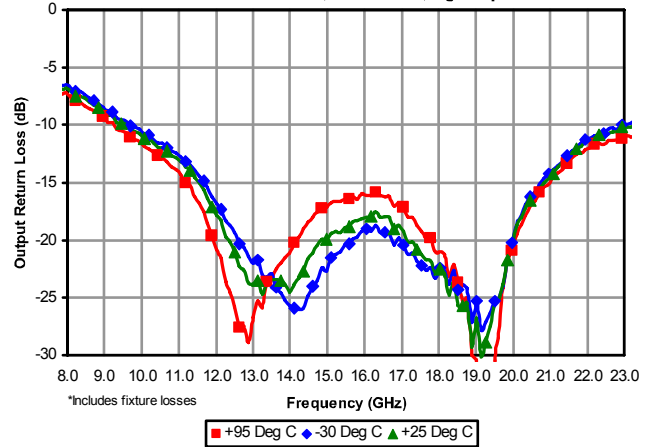
XB1008-BD Vd=4.0 V, Id=130 mA, Vg2=Open



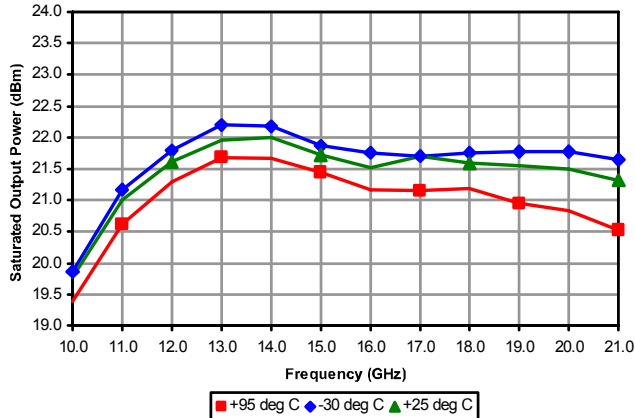
XB1008-BD Vd=4.0 V, Id=130 mA, Vg2=Open



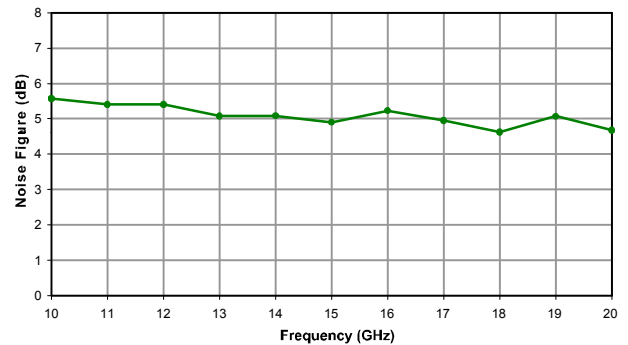
XB1008-BD Vd=4.0 V, Id=130 mA, Vg2=Open



XB1008-BD Vd=4.0 V, Id=130 mA, Vg2=Open
Pin=+10 dBm



XB1008-BD Vd=4V, Id=130mA, Vg1=Open



ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.
PRELIMINARY: Data Sheets contain information regarding a product M/A-COM Technology Solutions has under development. Performance is based on engineering tests. Specifications are typical. Mechanical outline has been fixed. Engineering samples and/or test data may be available. Commitment to produce in volume is not guaranteed.

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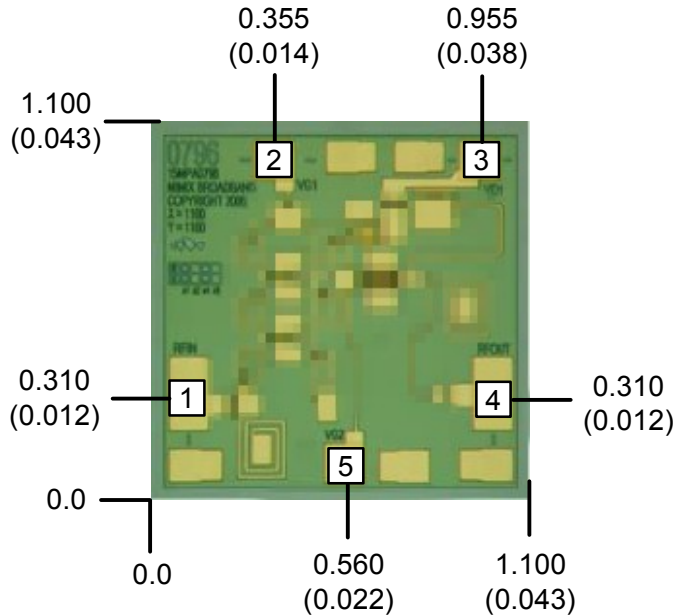
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Mechanical Drawing



(Note: Engineering designator is 15MPA0857)

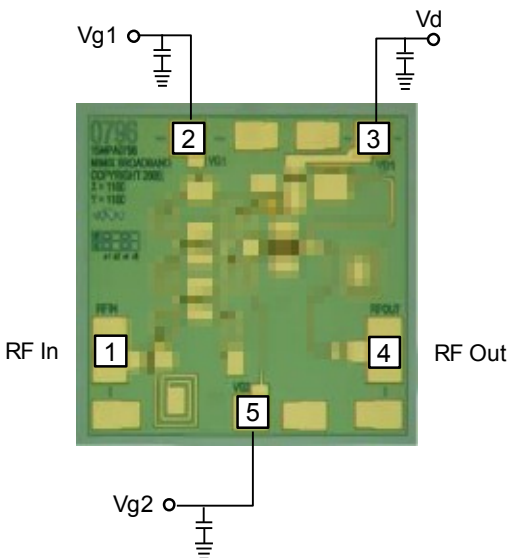
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
 Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
 All DC Bond Pads (except Vd3) are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads (and Vd3) are 0.100 x 0.200 (0.004 x 0.008)
 Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
 Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 0.75 mg.

Bond Pad #1 (RF In)
Bond Pad #2 (Vg1)

Bond Pad #3 (Vd)
Bond Pad #4 (RF Out)

Bond Pad #5 (Vg2)

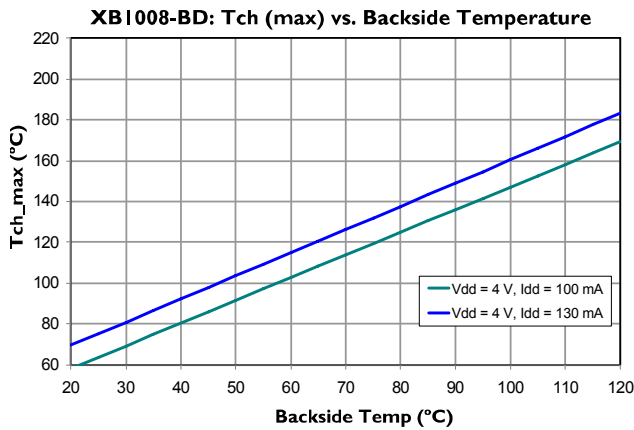
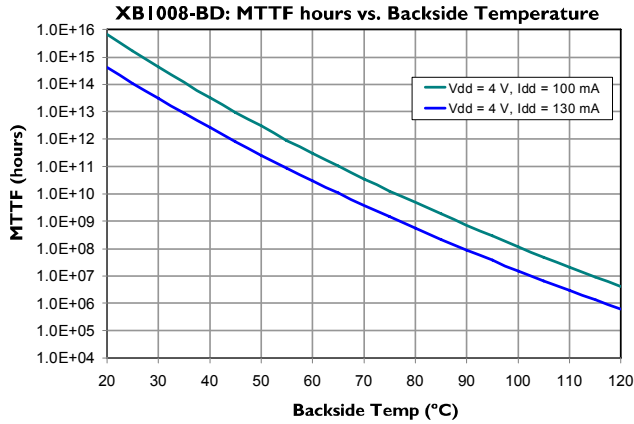
Bias Arrangement



Bypass Capacitors - See App Note [2]

MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.



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App Note [1] Biasing - The device provides variable gain with adjustable bias regulation. For optimum linearity performance, it is recommended to bias this device at $V_d=4V$ with $I_d=90\text{ mA}$ (V_{g2} at approximately $-0.5V$ and V_{g1} left open). It is also recommended to use active biasing to control the drain currents because this gives the most reproducible results over temperature or RF level variations. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is $-0.5V$. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - For Individual Stage Bias (Recommended for saturated applications) -- Each DC pad (V_d and $V_{g1,2}$) needs to have DC bypass capacitance ($\sim 100\text{-}200\text{ pF}$) as close to the device as possible. Additional DC bypass capacitance ($\sim 0.01\text{ }\mu\text{F}$) is also recommended.