Virtex-4 Family Overview

DS112 (v3.1) August 30, 2010 **Product Specification**

General Description

Combining Advanced Silicon Modular Block (ASMBL™) architecture with a wide variety of flexible features, the Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 FPGA hard-IP core blocks includes the PowerPC® processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks. The basic Virtex-4 FPGA building blocks are enhancements of those found in the popular Virtex, Virtex-E, Virtex-II, Virtex-II Pro, and Virtex-II Pro X product families, so previous-generation designs are upward compatible. Virtex-4 devices are produced on a state-of-the-art 90 nm copper process using 300 mm (12-inch) wafer technology.

Summary of Virtex-4 Family Features

- Three Families — LX/SX/FX
  - Virtex-4 LX: High-performance logic applications solution
  - Virtex-4 SX: High-performance solution for digital signal processing (DSP) applications
  - Virtex-4 FX: High-performance, full-featured solution for embedded platform applications
- Xesium™ Clock Technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ Slice
  - 18 x 18, two's complement, signed Multiplier
  - Optional pipeline stages
  - Built-in Accumulator (48-bit) and Adder/Subtracter
- Smart RAM Memory Hierarchy
  - Distributed RAM
  - Dual-port 18-Kbit RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
  - High-speed memory interface supports DDR and DDR-2 SDRAM, QDR-II, and RLDRAM-II.
- SelectIO™ Technology
  - 1.5V to 3.3V I/O operation
  - Built-in ChipSync™ source-synchronous technology
  - Digitally controlled impedance (DCI) active termination
  - Fine grained I/O banking (configuration in one bank)
- Flexible Logic Resources
- Secure Chip AES Bitstream Encryption
- 90 nm Copper CMOS Process
- 1.2V Core Voltage
- Flip-Chip Packaging including Pb-Free Package Choices
- RocketIO™ 622 Mb/s to 6.5 Gb/s Multi-Gigabit Transceiver (MGT) [*FX only*]
- IBM PowerPC RISC Processor Core [*FX only*]
  - PowerPC 405 (PPC405) Core
  - Auxiliary Processor Unit Interface (User Coprocessor)
- Multiple Tri-Mode Ethernet MACs [*FX only*]

Table 1: **Virtex-4 FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)(1)				XtremeDSP Slices(2)	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array(3) Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VLX15	64 x 24	13,824	6,144	96	32	48	864	4	0	N/A	N/A	N/A	9	320
XC4VLX25	96 x 28	24,192	10,752	168	48	72	1,296	8	4	N/A	N/A	N/A	11	448
XC4VLX40	128 x 36	41,472	18,432	288	64	96	1,728	8	4	N/A	N/A	N/A	13	640
XC4VLX60	128 x 52	59,904	26,624	416	64	160	2,880	8	4	N/A	N/A	N/A	13	640
XC4VLX80	160 x 56	80,640	35,840	560	80	200	3,600	12	8	N/A	N/A	N/A	15	768
XC4VLX100	192 x 64	110,592	49,152	768	96	240	4,320	12	8	N/A	N/A	N/A	17	960
XC4VLX160	192 x 88	152,064	67,584	1056	96	288	5,184	12	8	N/A	N/A	N/A	17	960
XC4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	N/A	N/A	N/A	17	960

Table 1: **Virtex-4 FPGA Family Members *(Continued)***

Device	Configurable Logic Blocks (CLBs)[1]				XtremeDSP Slices[2]	Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	RocketIO Transceiver Blocks	Total I/O Banks	Max User I/O
	Array[3] Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)							
XC4VSX25	64 x 40	23,040	10,240	160	128	128	2,304	4	0	N/A	N/A	N/A	9	320
XC4VSX35	96 x 40	34,560	15,360	240	192	192	3,456	8	4	N/A	N/A	N/A	11	448
XC4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	N/A	N/A	N/A	13	640
XC4VFX12	64 x 24	12,312	5,472	86	32	36	648	4	0	1	2	N/A	9	320
XC4VFX20	64 x 36	19,224	8,544	134	32	68	1,224	4	0	1	2	8	9	320
XC4VFX40	96 x 52	41,904	18,624	291	48	144	2,592	8	4	2	4	12	11	448
XC4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	16	13	576
XC4VFX100	160 x 68	94,896	42,176	659	160	376	6,768	12	8	2	4	20	15	768
XC4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	24	17	896

Notes:
1. One CLB = Four Slices = Maximum of 64 bits.
2. Each XtremeDSP slice contains one 18 x 18 multiplier, an adder, and an accumulator
3. Some of the row/column array is used by the processors in the FX devices.

System Blocks Common to All Virtex-4 Families

Xesium Clock Technology

- Up to twenty Digital Clock Manager (DCM) modules
  - Precision clock deskew and phase shift
  - Flexible frequency synthesis
  - Dual operating modes to ease performance trade-off decisions
  - Improved maximum input/output frequency
  - Improved phase shifting resolution
  - Reduced output jitter
  - Low-power operation
  - Enhanced phase detectors
  - Wide phase shift range
- Companion Phase-Matched Clock Divider (PMCD) blocks
- Differential clocking structure for optimized low-jitter clocking and precise duty cycle
- 32 Global Clock networks
- Regional I/O and Local clocks

Flexible Logic Resources

- Up to 40% speed improvement over previous generation devices
- Up to 200,000 logic cells including:
  - Up to 178,176 internal registers with clock enable (XC4VLX200)
  - Up to 178,176 look-up tables (LUTs)
  - Logic expanding multiplexers and I/O registers
- Cascadable variable shift registers or distributed memory capability

500 MHz XtremeDSP Slices

- Dedicated 18-bit x 18-bit multiplier, multiply-accumulator, or multiply-adder blocks
- Optional pipeline stages for enhanced performance
- Optional 48-bit accumulator for multiply accumulate (MACC) operation
- Integrated adder for complex-multiply or multiply-add operation
- Cascadeable Multiply or MACC
- Up to 100% speed improvement over previous generation devices.

500 MHz Integrated Block Memory

- Up to 10 Mb of integrated block memory
- Optional pipeline stages for higher performance
- Multi-rate FIFO support logic
  - Full and Empty Flag support
  - Fully programmable AF and AE Flags
  - Synchronous/ Asynchronous Operation
- Dual-port architecture
- Independent read and write port width selection (RAM only)
- 18 Kbit blocks (memory and parity/sideband memory support)
- Configurations from 16K x 1 to 512 x 36 (4K x 4 to 512 x 36 for FIFO operation)
- Byte-write capability (connection to PPC405, etc.)
- Dedicated cascade routing to form 32K x 1 memory without using FPGA routing
- Up to 100% speed improvement over previous generation devices.

SelectIO Technology

- Up to 960 user I/Os
- Wide selections of I/O standards from 1.5V to 3.3V
- Extremely high-performance
  - 600 Mb/s HSTL & SSTL (on all single-ended I/O)
  - 1 Gb/s LVDS (on all differential I/O pairs)
- True differential termination
- Selected low-capacitance I/Os for improved signal integrity
- Same edge capture at input and output I/Os
- Memory interface support for DDR and DDR-2 SDRAM, QDR-II, and RLDRAM-II.

ChipSync Technology

- Integrated with SelectIO technology to simplify source-synchronous interfaces
- Per-bit deskew capability built in all I/O blocks (variable input delay line)
- Dedicated I/O and regional clocking resources (pin and trees)
- Built in data serializer/deserializer logic in all I/O and clock dividers
- Memory/Networking/Telecommunication interfaces up to 1 Gb/s+ DDR

Digitally Controlled Impedance (DCI) Active I/O Termination

- Optional series or parallel termination
- Temperature compensation

Configuration

- 256-bit AES bitstream decryption provides intellectual property (IP) security
- Improved bitstream error detection/correction capability
- Fast SelectMAP configuration
- JTAG support
- Readback capability

90 nm Copper CMOS Process

1.2V Core Voltage

Flip-Chip Packaging

- Pb-Free packages available with production devices.

System Blocks Specific to the Virtex-4 FX Family

RocketIO Multi-Gigabit Transceiver (MGT)

- Full-duplex serial transceiver (MGT) capable of 622 Mb/s to 6.5 Gb/s baud rates
- 8B/10B, 64B/66B, user-defined FPGA logic, or no data encoding/decoding
- Channel bonding support
- CRC generation and checking
- Programmable TX pre-emphasis or pre-equalization
- Programmable RX continuous time equalization
- Programmable RX decision feedback equalization
- On-chip RX AC coupling
- RX signal detect and loss of signal indicator
- TX driver electrical idle mode
- User dynamic reconfiguration using secondary configuration bus

PowerPC 405 Processor RISC Core

- Embedded PowerPC 405 processor (PPC405) core
  - Up to 450 MHz operation
  - Five-stage data path pipeline
  - 16 KB instruction cache
  - 16 KB data cache
  - Enhanced instruction and data on-chip memory (OCM) controllers
  - Additional frequency ratio options between PPC405 and Processor Local Bus
- Auxiliary Processor Unit (APU) Interface for direct connection from PPC405 to coprocessors in fabric
  - APU can run at different clock rates
  - Supports autonomous instructions: no pipeline stalls
  - 32-bit instruction and 64-bit data
  - 4-cycle cache line transfer

Tri-Mode Ethernet Media Access Controller

- IEEE 802.3 compliant
- Operates at 10, 100, and 1,000 Mb/s
- Supports tri-mode auto-detect
- Receive address filter
- Fully monolithic 1000Base-X solution with RocketIO MGT
- Implements SGMII through RocketIO MGT to external PHY device
- Supports multiple PHY (MII, GMII, etc.) interfaces through an I/O resource
- Receive and transmit statistics available through separate interfaces
- Separate host and client interfaces
- Support for jumbo frames
- Flexible, user-configurable host interface

Architectural Description: Virtex-4 FPGA Array Overview

Virtex-4 devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. Virtex-4 devices implement the following functionality:

- I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by programmable I/O blocks (IOBs). The IOBs are enhanced for source-synchronous applications. Source-synchronous optimizations include per-bit deskew, data serializer/deserializer, clock dividers, and dedicated local clocking resources.
- Configurable Logic Blocks (CLBs), the basic logic elements for Xilinx FPGAs, provide combinatorial and synchronous logic as well as distributed memory and SRL16 shift register capability.
- Block RAM modules provide flexible 18Kbit true dual-port RAM, that are cascadable to form larger memory blocks. In addition, Virtex-4 FPGA block RAMs contain optional programmable FIFO logic for increased device utilization.
- Cascadable embedded XtremeDSP slices with 18-bit x 18-bit dedicated multipliers, integrated Adder, and 48-bit accumulator.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication/division, and coarse-/fine-grained clock phase shifting.

Additionally, FX devices support the following embedded system functionality:

- Integrated high-speed serial transceivers enable data rates up to 6.5 Gb/s per channel.
- Embedded IBM PowerPC 405 Processor RISC CPU (up to 450 MHz) with the auxiliary processor unit interface
- 10/100/1000 Ethernet media-access control (EMAC) cores.

The general routing matrix (GRM) provides an array of routing switches between each component. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-4 FPGA Features

This section briefly describes the features of the Virtex-4 family of FPGAs.

Input/Output (SelectIO) Blocks

IOBs are programmable and can be categorized as follows:

- Programmable single-ended or differential (LVDS) operation
- Input block with an optional single data rate (SDR) or double data rate (DDR) register
- Output block with an optional SDR or DDR register
- Bidirectional block
- Per-bit deskew circuitry
- Dedicated I/O and regional clocking resources
- Built in data serializer/deserializer

The IOB registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended standards:

- LVTTL
- LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI (33 and 66 MHz)
- PCI-X
- GTL and GTLP
- HSTL 1.5V and 1.8V (Class I, II, III, and IV)
- SSTL 1.8V and 2.5V (Class I and II)

The DCI I/O feature can be configured to provide on-chip termination for each single-ended I/O standard and some differential I/O standards.

The IOB elements also support the following differential signaling I/O standards:

- LVDS and Extended LVDS (2.5V only)
- BLVDS (Bus LVDS)
- ULVDS
- Hypertransport™
- Differential HSTL 1.5V and 1.8V (Class II)
- Differential SSTL 1.8V and 2.5V (Class II)

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Per-bit deskew circuitry allows for programmable signal delay internal to the FPGA. Per-bit deskew flexibly provides fine-grained increments of delay to carefully produce a

range of signal delays. This is especially useful for synchronizing signal edges in source synchronous interfaces.

General purpose I/O in select locations (four per bank) are designed to be “regional clock capable” I/O by adding special hardware connections for I/O in the same locality. These regional clock inputs are distributed within a limited region to minimize clock skew between IOBs. Regional I/O clocking supplements the global clocking resources.

Data serializer/deserializer capability is added to every I/O to support source synchronous interfaces. A serial-to-parallel converter with associated clock divider is included in the input path, and a parallel-to-serial converter in the output path.

An in-depth guide to the Virtex-4 FPGA IOB is discussed in the *Virtex-4 FPGA User Guide*.

Configurable Logic Blocks (CLBs)

A CLB resource is made up of four slices. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Fast carry look-ahead chain

The function generators F & G are configurable as 4-input look-up tables (LUTs). Two slices in a CLB can have their LUTs configured as 16-bit shift registers, or as 16-bit distributed RAM. In addition, the two storage elements are either edge-triggered D-type flip-flops or level sensitive latches. Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

The Virtex-4 FPGA CLBs are further discussed in the *Virtex-4 FPGA User Guide*.

Block RAM

The block RAM resources are 18 Kb true dual-port RAM blocks, programmable from 16K x 1 to 512 x 36, in various depth and width configurations. Each port is totally synchronous and independent, offering three “read-during-write” modes. Block RAM is cascadable to implement large embedded storage blocks. Additionally, back-end pipeline registers, clock control circuitry, built-in FIFO support, and byte write enable are new features supported in the Virtex-4 FPGA.

The block RAM feature in Virtex-4 devices is further discussed in the *Virtex-4 FPGA User Guide*.

XtremeDSP Slices

The XtremeDSP slices contain a dedicated 18 x 18-bit 2’s complement signed multiplier, adder logic, and a 48-bit accumulator. Each multiplier or accumulator can be used independently. These blocks are designed to implement extremely efficient and high-speed DSP applications.

The block DSP feature in Virtex-4 devices are further discussed in *XtremeDSP Design Considerations*.

Global Clocking

The DCM and global-clock multiplexer buffers provide a complete solution for designing high-speed clock networks.

Up to twenty DCM blocks are available. To generate deskewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90°, 180°, and 270° phase-shifted versions of the output clocks. Fine-grained phase shifting offers higher resolution phase adjustment with fraction of the clock period increments. Flexible frequency synthesis provides a clock output frequency equal to a fractional or integer multiple of the input clock frequency.

Virtex-4 devices have 32 global-clock MUX buffers. The clock tree is designed to be differential. Differential clocking helps reduce jitter and duty cycle distortion.

Routing Resources

All components in Virtex-4 devices use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance for high-speed designs.

Boundary-Scan

Boundary-Scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-4 devices, complying with IEEE standards 1149.1 and 1532.

Configuration

Virtex-4 devices are configured by loading the bitstream into internal configuration memory using one of the following modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE-1532)

Optional 256-bit AES decryption is supported on-chip (with software bitstream encryption) providing Intellectual Property security.

Virtex-4 FX Family

This section briefly describes blocks available only in FX devices.

RocketIO Multi-Gigabit Transceiver

8 – 24 Channels RocketIO Multi-Gigabit Serial Transceivers (MGTs) capable of running 622 Mb/s – 6.5 Gb/s

- Full Clock and Data Recovery
- 32-bit or 40-bit datapath support
- Optional 8B/10B, 64B/66B, or FPGA-based encode/decode
- Integrated FIFO/Elastic Buffer
- Support for Channel Bonding
- Embedded 32-bit CRC generation/checking
- Integrated Comma-detect or programmable A1/A2, A1A1/A2A2 detection
- Programmable pre-emphasis (AKA transmitter equalization)
- Programmable receiver equalization
- Embedded support for:
  - Out of Band (OOB) Signalling: Serial ATA
  - Beaconing and Electrical Idle: PCI-Express™
- On-chip bypassable AC coupling for receiver

One or Two PowerPC 405 Processor Cores

- 32-bit Harvard Architecture
- 5-Stage Execution Pipeline
- Integrated 16KB Level 1 Instruction Cache and 16KB Level 1 Data Cache
- Integrated Level 1 Cache Parity Generation and Checking
- CoreConnect™ Bus Architecture
- Efficient, high-performance on-chip memory (OCM) interface to block RAM
- PLB Synchronization Logic (Enables Non-Integer CPU-to-PLB Clock Ratios)
- Auxiliary Processor Unit (APU) Interface and Integrated APU Controller
  - Optimized FPGA-based Coprocessor connection
  - Automatic decode of PowerPC floating-point instructions — allows custom instructions (decode for up to eight instructions)
  - Extremely efficient microcontroller-style interfacing

Two or Four Tri-Mode (10/100/1000 Mb/s) Ethernet Media Access Control (MAC) Cores

- IEEE 802.3-2000 Compliant
- MII/GMII Interface or SGMII (when used with RocketIO Transceivers)
- Can Operate Independent of PowerPC processor
- Half- or Full-Duplex
- Supports Jumbo Frames
- 1000Base-X PCS/PMA: When used with RocketIO MGT can provide complete 1000Base-X implementation on-chip

Intellectual Property Cores

Xilinx offers IP cores for commonly used complex functions including DSP, bus interfaces, processors, and processor peripherals. Using Xilinx LogiCORE™ products and cores from third party AllianceCORE participants, customers can shorten development time, reduce design risk, and obtain superior performance for their designs. Additionally, our CORE Generator™ system allows customers to implement IP cores into Virtex-4 FPGAs with predictable and repeatable performance. It offers a simple user interface to generate parameter-based cores optimized for our FPGAs.

The System Generator for DSP tool allows system architects to quickly model and implement DSP functions using handcrafted IP, and features an interface to third-party system level DSP design tools. System Generator for DSP implements many of the high-performance DSP cores supporting Virtex-4 FPGAs including the Xilinx Forward Error Correction Solution with Interleaver/De-interleaver, Reed-Solomon encoder/decoders, and Viterbi decoders. These are ideal for creating highly-flexible, concatenated codecs to support the communications market.

Industry leading connectivity and networking IP cores include the electronics industry's first Advanced Switching product, leading-edge PCI Express, Serial RapidIO, Fibre Channel, and 10Gb Ethernet cores that include Virtex-4 FPGA RocketIO multi-gigabit serial interfaces. The Xilinx SPI-4.2 IP core utilizes the Virtex-4 FPGA embedded ChipSync technology to implement dynamic phase alignment for high-performance source-synchronous operation.

MicroBlaze™ processor 32-bit core provides the industry's fastest soft processing solution for building complex systems for the networking, telecommunication, data communication, embedded and consumer markets. The MicroBlaze processor features a RISC architecture with Harvard-style separate 32-bit instruction and data busses running at full speed to execute programs and access data from both on-chip and external memory. A standard set of peripherals are also CoreConnect™ enabled to offer MicroBlaze processor designers compatibility and reuse.

All IP cores for Virtex-4 FPGAs are found on the Xilinx IP Center Internet portal presenting the latest intellectual property cores and reference designs via Smart Search for faster access.

Application Notes and Reference Designs

Application notes and reference designs written specifically for the Virtex-4 family are available on the Xilinx web site at http://www.xilinx.com/support/documentation/virtex-4.htm.

Virtex-4 Device and Package Combinations and Maximum I/Os

Table 2: **Virtex-4 Device and Package Combinations and Maximum Available I/Os**

Package(1,2)	SF363 SFG363		FF668 FFG668		FF672 FFG672		FF676 FFG676		FF1148 FFG1148		FF1152 FFG1152		FF1513 FFG1513		FF1517 FFG1517	
Size	17 x 17		27 x 27		27 x 27		27 x 27		35 x 35		35 x 35		40 x 40		40 x 40	
Device	MGTs	I/O	MGTs	I/O	MGTs	I/O	MGTs	I/O	MGTs	I/O	MGTs	I/O	MGTs	I/O	MGTs	I/O
XC4VLX15	N/A	240	N/A	320			N/A	320								
XC4VLX25	N/A	240	N/A	448												
XC4VLX40			N/A	448					N/A	640						
XC4VLX60			N/A	448					N/A	640						
XC4VLX80									N/A	768						
XC4VLX100									N/A	768			N/A	960		
XC4VLX160									N/A	768			N/A	960		
XC4VLX200													N/A	960		
XC4VSX25			N/A	320												
XC4VSX35			N/A	448												
XC4VSX55									N/A	640						
XC4VFX12	N/A	240	N/A	320												
XC4VFX20					8	320										
XC4VFX40					12	352					12	448				
XC4VFX60					12	352					16	576				
XC4VFX100											20	576			20	768
XC4VFX140															24	768

Notes:
1. All packages are also available in Pb-Free versions (SFG/FFG).
2. Pinouts on all packages (except SF363/SFG363 and FF668/FFG668) are configured using the new, improved SparseChevron pin layout for superior signal integrity.

Virtex-4 FPGA Ordering Information

Virtex-4 FPGA ordering information shown in Figure 1 applies to all packages including Pb-Free.

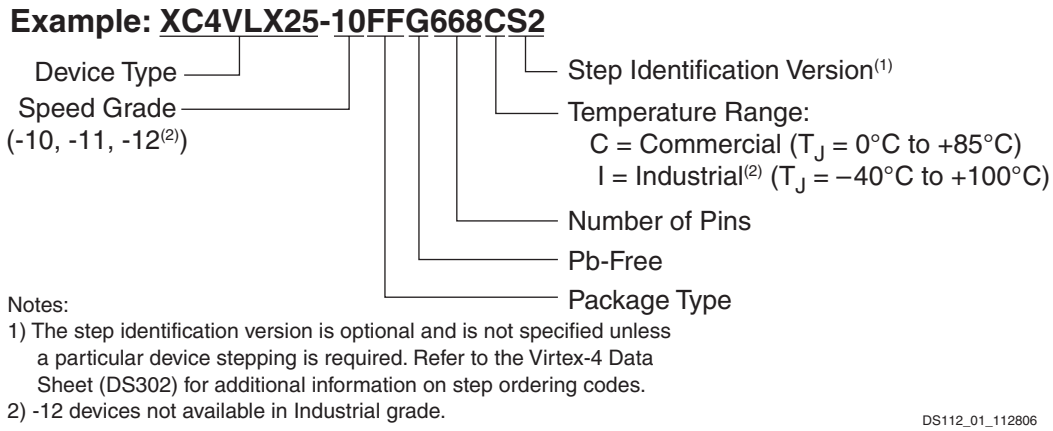

Figure 1: **Virtex-4 FPGA Ordering Information**

Virtex-4 Documentation

Complete and up-to-date documentation of the Virtex-4 family of FPGAs is available on the Xilinx web site. In addition to the most recent Virtex-4 Family Overview, the following files are also available for download:

Virtex-4 FPGA Data Sheet: DC and Switching Characteristics

This data sheet contains the DC and Switching Characteristic specifications for the Virtex-4 family.

Virtex-4 FPGA User Guide

This guide includes chapters on:

- Clocking Resources
- Digital Clock Manager (DCM)
- Phase-Matched Clock Dividers (PMCD)
- Block RAM and FIFO memory
- Configurable Logic Blocks (CLBs)
- SelectIO Resources
- SelectIO Logic Resources
- Advanced SelectIO Logic Resources

XtremeDSP for Virtex-4 FPGAs User Guide

This guide describes the DSP48 slice and includes reference designs for using DSP48 math functions and various FIR filters.

Virtex-4 FPGA Configuration Guide

This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, and reconfiguration techniques.

Virtex-4 FPGA Packaging and Pinout Specification

This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

Virtex-4 FPGA PCB Designer's Guide

This guide describes PCB guidelines for the Virtex-4 family. It covers SelectIO signaling, RocketIO signaling, power distribution systems, PCB breakout, and parts placement.

Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide

This guide describes the RocketIO Multi-Gigabit Transceivers available in the Virtex-4 FX family.

Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide

This guide describes the Embedded Tri-Mode Ethernet Media Access Controller available in the Virtex-4 FX family.

PowerPC 405 Processor Block Reference Guide

This guide is updated to include the PowerPC 405 processor block available in the Virtex-4 FX family.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/02/04	1.0	Initial Xilinx release. Printed Handbook version.
09/10/04	1.1	Typographical edits.
12/08/04	1.2	• Removed System Monitor and ADC references. • Edited Ethernet MAC section.
03/26/05	1.3	• Removed legacy CLB reference and typographical edits. • Edited serial transceiver sections. • In Table 2 added FFG Pb-Free packages.
06/17/05	1.4	Added note to Table 2 for SparseChevron pinouts.
02/10/06	1.5	• Removed FCRAM-II support. • Added note 3 to Table 1. • Revised the CLB numbers for XC4VFX40 devices in Table 1. • Added stepping to order information example in Figure 1.
10/10/06	1.6	• Changed maximum transceiver rate to 6.5 Gb/s. • Removed FF1760 package from Table 2.
01/23/07	2.0	Revision number jumped to 2.0 to correlate to data sheet (DS302) major revision. • Table 1: Corrected typo: XC4VFX40 number of slices = 18,624. • Table 2: Added column for FF676 package. Rewrote table footnotes.