XC6135 Series

ETR02041-004

Ultra-Low Power (44nA) Voltage Detector with Separated Sense Pin

■GENERAL DESCRIPTION

The XC6135 series is ultra-low power voltage detector with high accuracy detection, manufactured using CMOS process and laser trimming technologies.

Since the sense pin is separated from the power supply pin, it allows the IC to monitor the other power supply. The XC6135 can maintain the state of detection even when voltage of the monitored power supply drops to 0V. Sense Pin is also suited for detecting low voltages starting from 0.5V.

Ultra-small low height package USPQ-4B05 and standard packages SSOT-24 and SOT-25 which are ideally suited for small design of portable devices and high densely mounting applications.

UVLO circuit is implemented in order to suppress the floating of RESETB pin (undefined operation) when V_{IN} voltage is lower than the minimum operation voltage.

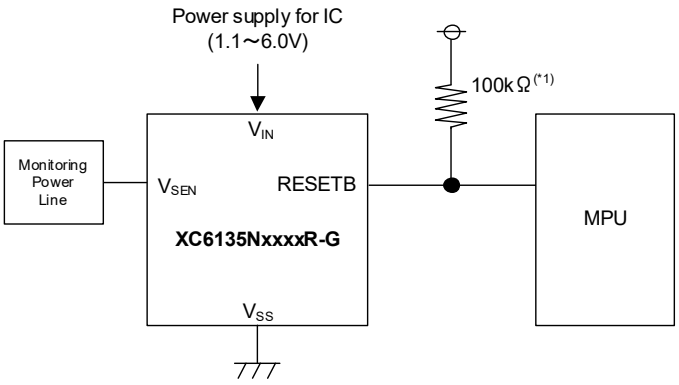
■APPLICATIONS

- Energy Harvesting
- Wearable devices
- Smart meter
- Microprocessor logic reset circuitry
- System battery life and charge voltage monitors
- Power-on reset circuits
- Power failure Detection

■ FEATURES

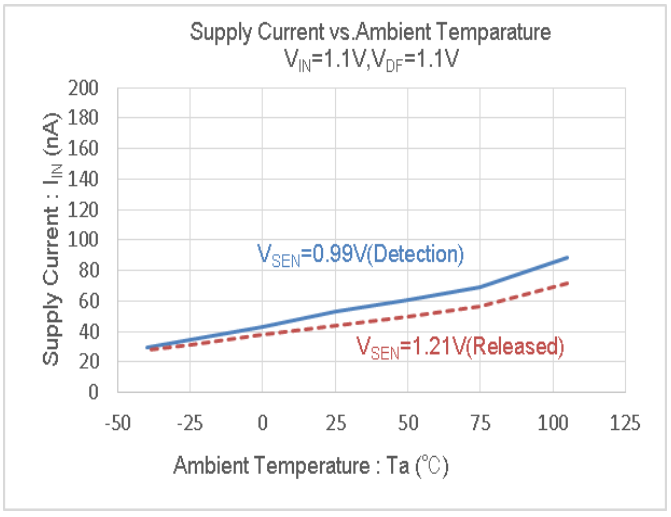
Ultra-Low Power	:53nA TYP.(@detection, V_{IN}=1.1V)
	:44nA TYP.(@released, V_{IN}=1.1V)
High Accuracy	:±10mV (0.5≦V_{DF}≦1.1V, Ta=25℃) ±0.8% (1.2≦V_{DF}≦3.0V, Ta=25℃) ±1.0% (3.1V≦V_{DF}≦5.0V, Ta=25℃)
	:±30mV (0.5≦V_{DF}≦1.1V, Ta=-40℃~ 105℃) ±2.5% (1.2≦V_{DF}≦3.0V, Ta=-40℃~ 105℃) ±2.7% (3.1V≦V_{DF}≦5.0V, Ta=-40℃~ 105℃)
Temperature Characteristics	:±50ppm/℃ (TYP.)
Hysteresis width	:TYPE:A/C V_{DF}×5.0% (TYP.) TYPE:B/D 2mV ~ 28mV (TYP.)
Detect voltage range	:0.5V ~ 5.0V (0.1Vstep)
Operating voltage range	:1.1V ~ 6.0V
Output type	:CMOS Nch open drain
Output logic	:RESETB (Active Low) RESET (Active High)
Undefined operation Protection (CMOS Output only)	:Output pin Voltage 0.38V (MAX: Ta=-40℃~ 105℃) @Power supply Input pin Voltage＜ Minimum operation Voltage
Packages	:USPQ-4B05, SSOT-24, SOT-25
Environment friendly	:EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION



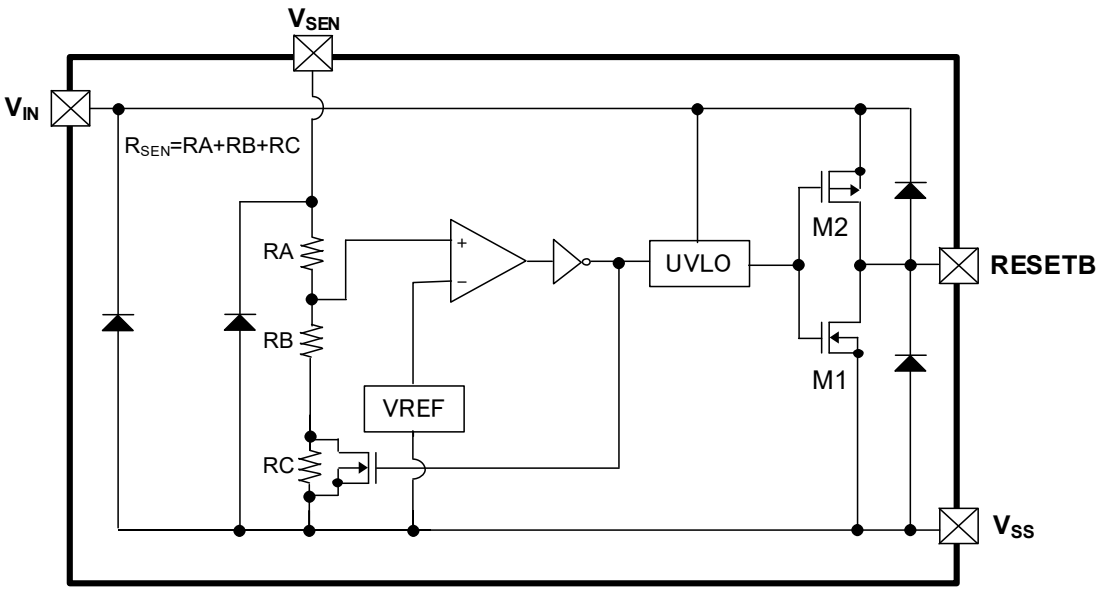
(*1) Unused for the CMOS output products

■TYPICAL PERFORMANCE CHARACTERISTICS



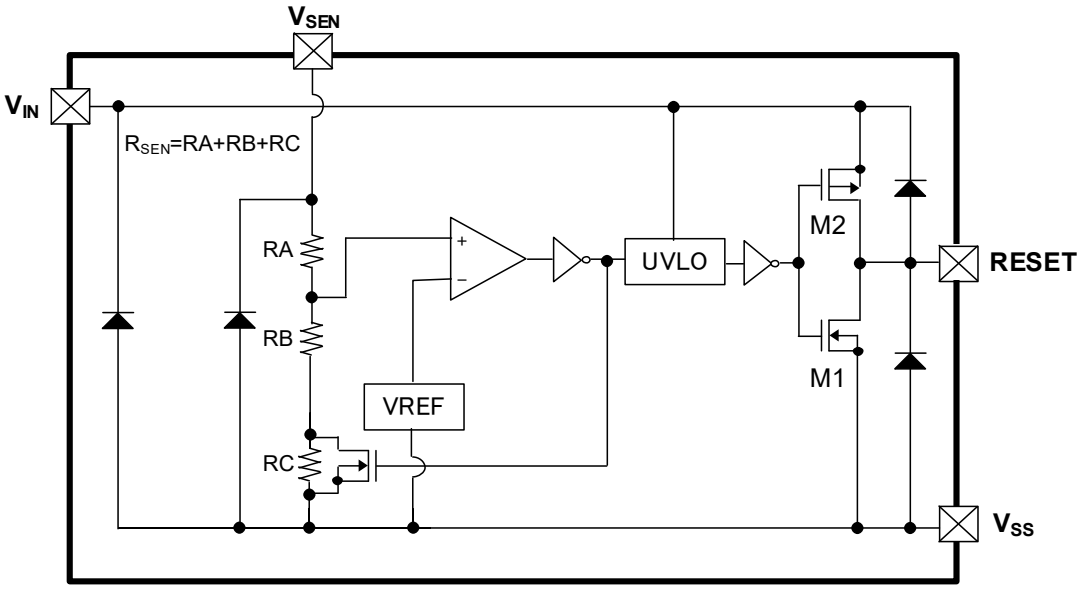
■BLOCK DIAGRAMS

(1) XC6135C Series A/B type (RESETB OUTPUT: CMOS output/Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

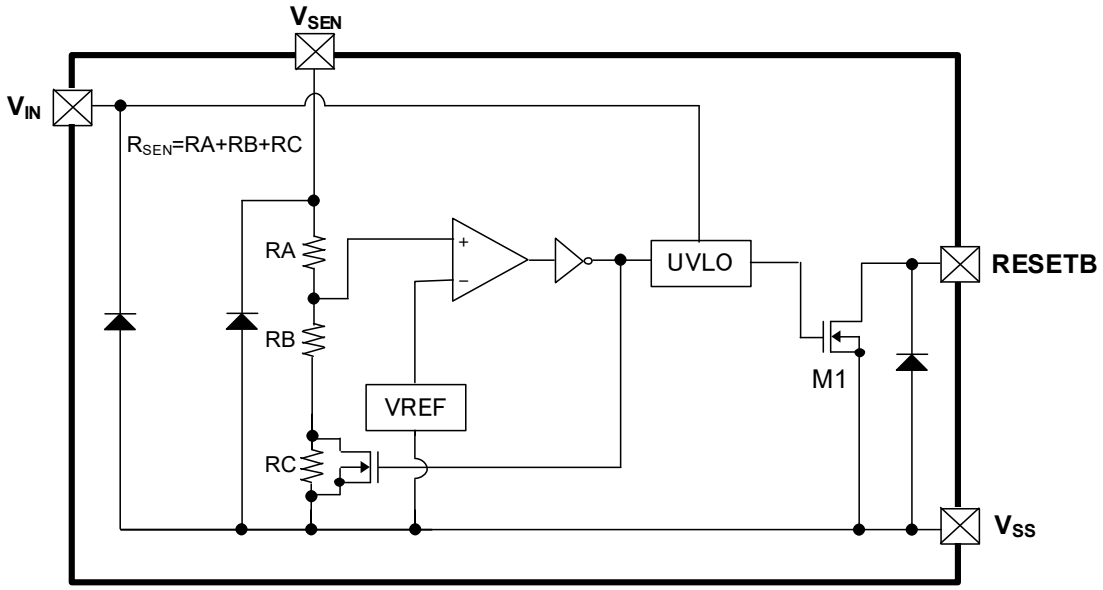
(2) XC6135C Series C/D type (RESETB OUTPUT: CMOS output/Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

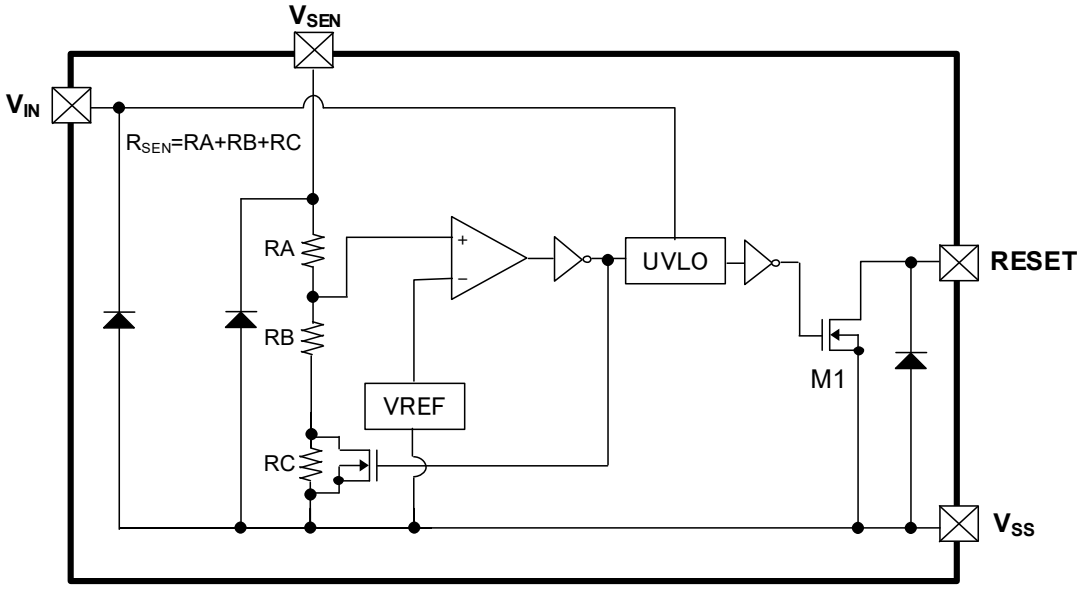
■BLOCK DIAGRAMS

(3) XC6135N Series A/B type（RESETB OUTPUT: Nch open drain output /Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

(4) XC6135N Series C/D type (RESETB OUTPUT: Nch open drain output /Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XC6135①②③④⑤⑥-⑦(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	Nch open drain output
②③	Detect Voltage	05 ~ 50	e.g. 5.0V → ②=5, ③=0
④	Type	A	Refer to Selection Guide
		B	
		C	
		D	
⑤⑥-⑦(*1)	Package (Order Unit)	9R-G	USPQ-4B05 (5,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)
		MR-G	SOT-25 (3,000pcs/Reel) (*2)

(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

(*2) SOT-25 uses Cu bonding wires.

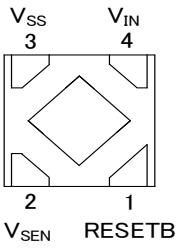
●Selection Guide

TYPE	RESETB/RESET OUTPUT	HYSTERESIS
A	Active Low	V_{DF}×5.0% (TYP)
B	↑	2mV ~ 28mV (TYP) (*1)
C	Active High	V_{DF}×5.0% (TYP)
D	↑	2mV ~ 28mV (TYP) (*1)

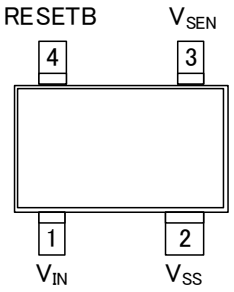
(*1) Refer to SPEC TABLE.

■PIN CONFIGURATION

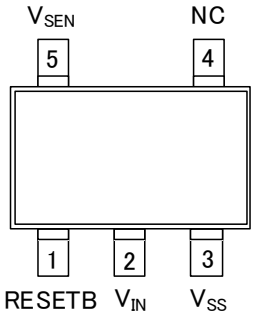
● Type: A/B



USPQ-4B05
(BOTTOM VIEW)

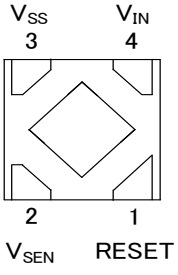


SSOT-24
(TOP VIEW)

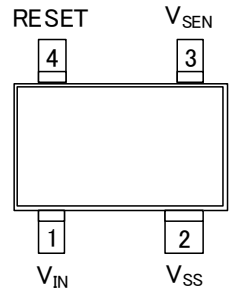


SOT-25
(TOP VIEW)

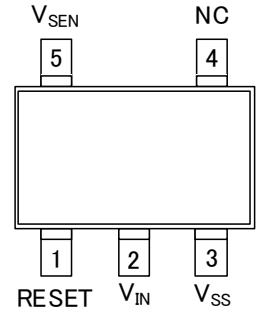
● Type: C/D



USPQ-4B05
(BOTTOM VIEW)



SSOT-24
(TOP VIEW)



SOT-25
(TOP VIEW)

*The dissipation pad for the USPQ-4B05 package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to V_{SS} (No. 3) pin.

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTION
USPQ-4B05	SSOT-24	SOT-25		
1	4	1	RESETB	Reset Output (Active Low) (*1)
			RESET	Reset Output (Active High) (*2)
2	3	5	V_{SEN}	Voltage Sense
3	2	3	V_{SS}	Ground
4	1	2	V_{IN}	Power Input
-	-	4	NC	No Connection

(*1) Type A,B (Refer to the ④ in Ordering Information table.)
(*2) Type C,D (Refer to the ④ in Ordering Information table.)

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL		RATINGS	UNITS
Input Voltage		V_{IN}		-0.3 ~ 7.0	V
V_{SEN} Pin Voltage		V_{SEN}		-0.3 ~ 7.0	V
Output Voltage	XC6135C(*2)	V_{RESETB}	V_{RESET}	V_{SS} - 0.3 ~ V_{IN} + 0.3 or 7.0 (*1)	V
	XC6135N(*3)			V_{SS} - 0.3 ~ 7.0	V
Output Current	XC6135C(*2)	I_{RBOUT}	I_{ROUT}	±50	mA
	XC6135N(*3)			50	
Power Dissipation (Ta=25℃)	USPQ-4B05	Pd		100	mW
				550 (40mm x 40mm Standard board) (*4)	
	SSOT-24			150	
				500 (40mm x 40mm Standard board) (*4)	
				680 (JESD51-7 board) (*4)	
	SOT-25			250	
				600 (40mm x 40mm Standard board) (*4)	
				760b(JESD51-7 board) (*4)	
Operating Ambient Temperature		Topr		-40 ~ 105	℃
Storage Temperature		Tstg		-55 ~ 125	℃

* All voltages are described based on the V_{SS}.
(*1) The maximum value should be either V_{IN}+0.3V or 7.0V in the lowest.
(*2) CMOS output
(*3) Nch open drain output
(*4) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦105℃(*4)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V_{IN}		1.1		6.0	1.1		6.0	V	①
MIN Voltage Holding the Detection(*3)	V_{INL}	V_{IN}=V_{SEN}	-	-	0.4	-	-	0.4	V	
Detect Voltage	V_{DF}	$V_{DF(T)}$(*1)=0.5V~1.1V	$V_{DF(T)}$ -10mV	$V_{DF(T)}$	$V_{DF(T)}$ +10mV	$V_{DF(T)}$ -30mV	$V_{DF(T)}$	$V_{DF(T)}$ +30mV	V	
		$V_{DF(T)}$(*1)=1.2V~3.0V	$V_{DF(T)}$ ×0.992	$V_{DF(T)}$	$V_{DF(T)}$ ×1.008	$V_{DF(T)}$ ×0.975	$V_{DF(T)}$	$V_{DF(T)}$ ×1.025	V	
		$V_{DF(T)}$(*1)=3.1V~5.0V	$V_{DF(T)}$ ×0.990	$V_{DF(T)}$	$V_{DF(T)}$ ×1.010	$V_{DF(T)}$ ×0.973	$V_{DF(T)}$	$V_{DF(T)}$ ×1.027	V	
Temperature Characteristics	ΔV_{DF}/ (ΔTopr・V_{DF})	-40℃≦Topr≦105℃	-	±50	-	-	±50	-	ppm/℃	
Hysteresis Width (TYPE: A/C)	V_{HYS}		V_{DF} ×0.032	V_{DF} ×0.05	V_{DF} ×0.068	V_{DF} ×0.03	V_{DF} ×0.05	V_{DF} ×0.07	V	
Hysteresis Width (TYPE: B/D)			-	E-1(*2)		-	E-2(*2)		V	
Supply Current1 (TYPE:A/B)CMOS output	I_{ss1}	V_{SEN}=V_{DF}×0.9 V_{IN}=1.1V	-	53	150	-	53	387	nA	②
Supply Current1 (TYPE:C/D)CMOS output								242		
Supply Current1 (TYPE:A/B/C/D) Nch open drain output								252		
Supply Current1 (TYPE:A/B)CMOS output		V_{SEN}=V_{DF}×0.9 V_{IN}=6.0V	-	59	167	-	59	442		
Supply Current1 (TYPE:C/D)CMOS output								252		
Supply Current1 (TYPE:A/B/C/D) Nch open drain output								262		
Supply Current2 (TYPE:A/B)CMOS output	I_{ss2}	V_{SEN}=V_{DF}×1.1 V_{IN}=1.1V	-	44	134	-	44	230	nA	
Supply Current2 (TYPE:C/D)CMOS output								372		
Supply Current2 (TYPE:A/B/C/D) Nch open drain output								232		
Supply Current2 (TYPE:A/B)CMOS output		V_{SEN}=V_{DF}×1.1 V_{IN}=6.0V	-	48	142	-	48	242		
Supply Current2 (TYPE:C/D)CMOS output								422		
Supply Current2 (TYPE:A/B/C/D)Nch open drain output								242		
SENSE Resistance	R_{SEN}	V_{IN}=6.0V, V_{SEN}=1.0V	E-3(*2)		-	E-4(*2)		MΩ		③

(*1) $V_{DF(T)}$: Nominal detect voltage

(*2) Refer to SPEC TABLE

(*3) For XC6135C (CMOS output) only. V_{IN} value where RESETB <0.05V or RESET> V_{IN}-0.05V.

(*4) The ambient temperature range (-40℃≦Ta≦105℃) is a design value.

■ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦105℃(*9)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Peak of Undefined Operation(*5) (TYPE:A/B)	V_{UNO}	V_{IN}=V_{SEN}, V_{IN}<0.4V	-	0.1	0.38	-	0.1	0.38	V	④
UVLO Release Voltage	V_{UVLOR}	V_{IN}=0V→1.1 V V_{SEN}=V_{DF}×1.1	-	0.82	1.05	-	0.82	1.07	V	⑤
UVLO Detect Voltage	V_{UVLOD}	V_{IN}=1.1V→0 V V_{SEN}=V_{DF}×1.1	0.57	0.79	-	0.55	0.79	-		
UVLO Release Delay Time(*6)	t_{UVLOR}	V_{IN}=0V→1.1V V_{SEN}=V_{DF}×1.1	-	157	290	-	157	425	μs	⑥
Release Delay Time(*7)	t_{DR0}	V_{IN}=6.0V V_{SEN}=V_{DF}×0.9→ V_{DF}×1.1	-	44	200	-	44	224	μs	⑦
Detect Delay Time(*8)	t_{DF0}	V_{IN}=6.0V V_{SEN}=V_{DF}×1.1→ V_{DF}×0.9	-	40	170	-	40	184		

(*5) For XC6135C (CMOS output) only.

(*6) RESETB product: Time from when the V_{IN} pin voltage reaches the UVLO release voltage until the reset output pin reaches V_{IN}×90%.
RESET product: Time from when the V_{IN} pin voltage reaches the UVLO release voltage until the reset output pin reaches V_{IN}×10%.

(*7) RESETB product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches 5.4V (V_{IN}×90%).
RESET product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches 0.6V (V_{IN}×10%)
Release voltage (V_{DR}) =Detect voltage (V_{DF}) + Hysteresis width (V_{HYS}).

(*8) RESETB product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches 0.6V (V_{IN}×10%).
RESET product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches 5.4V (V_{IN}×90%).

(*9) The ambient temperature range (-40℃≦Ta≦105℃) is a design Value.

■ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25℃			-40℃≦Ta≦105℃(*12)			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
RESETB Output Current	I_{RBOUTN}	$V_{SEN}=V_{DF}\times0.9$ Nch. $V_{RESETB}=0.3V$							mA	⑧
		V_{IN}=1.1V	0.3	1.4	-	0.2	1.4	-		
		V_{IN}=2.0V	4.1	6.2	-	3.1	6.2	-		
		V_{IN}=3.0V	8.1	10.8	-	4.3	10.8	-		
		V_{IN}=4.0V	11.2	14.3	-	6.2	14.3	-		
		V_{IN}=5.0V	13.7	17.1	-	7.3	17.1	-		
		V_{IN}=6.0V	15.7	19.3	-	8.1	19.3	-		
	I_{RBOUTP}(*10)	$V_{SEN}=V_{DF}\times1.1$ Pch. $V_{RESETB}=V_{IN}-0.3V$								
		V_{IN}=1.0V	-	-0.7	-0.2	-	-0.7	-0.15		
		V_{IN}=3.0V	-	-3.2	-1.4	-	-3.2	-1.3		
		V_{IN}=6.0V	-	-5.1	-2.9	-	-5.1	-2.6		
RESET Output Current	I_{ROUTN}	$V_{SEN}=V_{DF}\times1.1$ Nch. $V_{RESETB}=0.3V$								
		V_{IN}=1.1V	0.3	1.4	-	0.2	1.4	-		
		V_{IN}=2.0V	4.1	6.2	-	3.1	6.2	-		
		V_{IN}=3.0V	8.1	10.8	-	4.3	10.8			
		V_{IN}=4.0V	11.2	14.3	-	6.2	14.3			
		V_{IN}=5.0V	13.7	17.1	-	7.3	17.1	-		
		V_{IN}=6.0V	15.7	19.3	-	8.1	19.3	-		
	I_{ROUTP}(*10)	$V_{SEN}=V_{DF}\times0.9$ Pch. $V_{RESET}=V_{IN}-0.3V$								
		V_{IN}=1.1V	-	-0.7	-0.2	-	-0.7	-0.15		
		V_{IN}=3.0V(*8)	-	-3.2	-1.4	-	-3.2	-1.3		
		V_{IN}=6.0V,	-	-5.1	-2.9	-	-5.1	-2.6		
RESETB Output Leakage Current	I_{LEAKN}(*11)	V_{IN}=6.0V,V_{SEN}=6.0V Nch. V_{RESETB}=6.0V	-	0.01	0.1	-	0.01	0.3	μA	
	I_{LEAKP}	V_{IN}=6.0V,V_{SEN}=0V Pch. V_{RESETB}=0V	-	-0.01	-	-	-0.01	-		
RESET Output Leakage Current	I_{LEAKN}(*11)	V_{IN}=6.0V,V_{SEN}=0V Nch. V_{RESET}=6.0V	-	0.01	0.1	-	0.01	0.3		
	I_{LEAKP}	V_{IN}=6.0V,V_{SEN}=6.0V Pch. V_{RESET}=0V	-	-0.01	-	-	-0.01	-		

(*10) For XC6135C (CMOS output) only.

(*11) Max. value is for XC6135N (Nch open drain).

(*12) The ambient temperature range (-40℃≦Ta≦105℃) is a design Value.

■ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

NOMINAL DETECT VOLTAGE(V)	E-1		E-2		E-3		E-4	
	Ta=25℃		-40℃≦Ta≦105℃		Ta=25℃		-40℃≦Ta≦105℃	
	Hysteresis Width (mV)				SENSE Resistance (MΩ)			
$V_{DF(T)}$	TYP.	MAX.	TYP.	MAX.	MIN	TYP.	MIN	TYP.
0.5	1	2.0	1	2.2	4.0	23	3.1	23
0.6	1	2.4	1	2.7	3.6	27	3.0	27
0.7	1	2.8	1	3.1	2.8	31	2.7	31
0.8	1	3.2	1	3.5	2.5	35	2.4	35
0.9	1	3.6	1	4.0	2.9	38	2.8	38
1.0	2	4.0	2	4.4	4.0	39	3.9	39
1.1	2	4.4	2	4.9	14	39	11	39
1.2	2	4.8	2	5.3	15	40	12	40
1.3	2	5.2	2	5.7	16	42	13	42
1.4	2	5.6	2	6.2	17	41	13	41
1.5	2	6.0	2	6.6	16	41	13	41
1.6	2	6.4	2	7.1	16	41	13	41
1.7	3	6.8	3	7.5	16	40	13	40
1.8	3	7.2	3	8.0	16	39	12	39
1.9	3	7.9	3	8.7	16	39	12	39
2.0	3	8.6	3	9.5	16	38	12	38
2.1	4	9.4	4	10	16	37	12	37
2.2	4	10	4	11	16	37	12	37
2.3	5	11	5	12	16	36	12	36
2.4	5	12	5	13	15	36	12	36
2.5	6	13	6	14	15	36	12	36
2.6	6	14	6	15	15	35	12	35
2.7	7	15	7	16	15	35	12	35
2.8	8	16	8	17	15	35	12	35
2.9	8	17	8	18	15	35	12	35
3.0	9	18	9	19	15	34	11	34
3.1	9	19	9	20	15	34	11	34
3.2	10	20	10	21	15	34	11	34
3.3	11	21	11	23	15	34	11	34
3.4	12	22	12	24	15	33	11	33
3.5	12	23	12	25	15	33	11	33
3.6	13	25	13	26	15	33	11	33
3.7	14	26	14	28	15	33	11	33
3.8	15	27	15	29	15	33	11	33
3.9	16	29	16	30	15	33	11	33
4.0	17	30	17	32	15	33	11	33
4.1	18	32	18	33	15	32	11	32
4.2	19	33	19	35	15	32	11	32
4.3	20	35	20	36	15	32	11	32

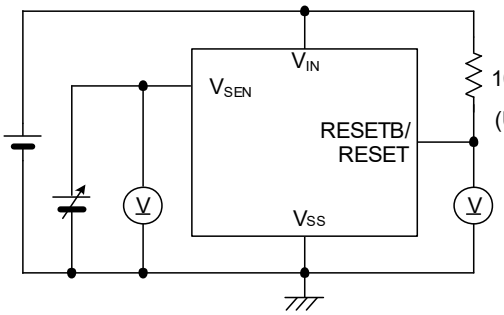
■ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

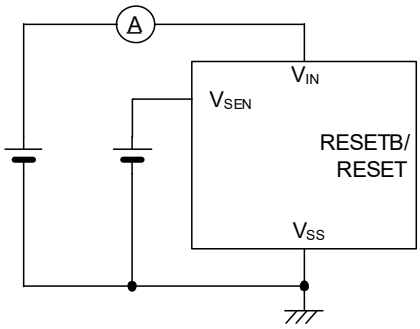
NOMINAL DETECT VOLTAGE(V)	E-1 Ta=25℃ Hysteresis Width (mV)		E-2 -40℃≦Ta≦105℃ Hysteresis Width (mV)		E-3 Ta=25℃ SENSE Resistance (MΩ)		E-4 -40℃≦Ta≦105℃ SENSE Resistance (MΩ)	
$V_{DF(T)}$	TYP.	MAX.	TYP.	MAX.	MIN	TYP.	MIN	TYP.
4.4	21	36	21	38	15	32	11	32
4.5	22	38	22	40	15	32	11	32
4.6	23	39	23	41	15	32	11	32
4.7	24	41	24	43	15	32	11	32
4.8	25	43	25	45	15	32	11	32
4.9	26	44	26	46	14	32	11	32
5.0	28	46	28	48	14	32	11	32

■TEST CIRCUITS

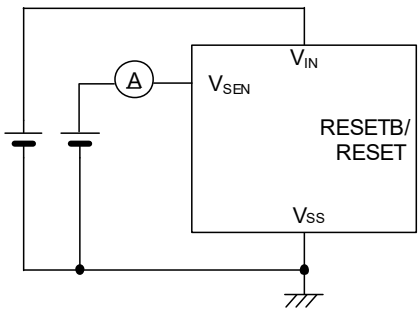
CIRCUIT①



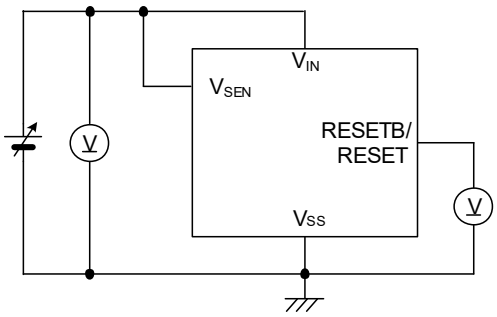
CIRCUIT②



CIRCUIT③



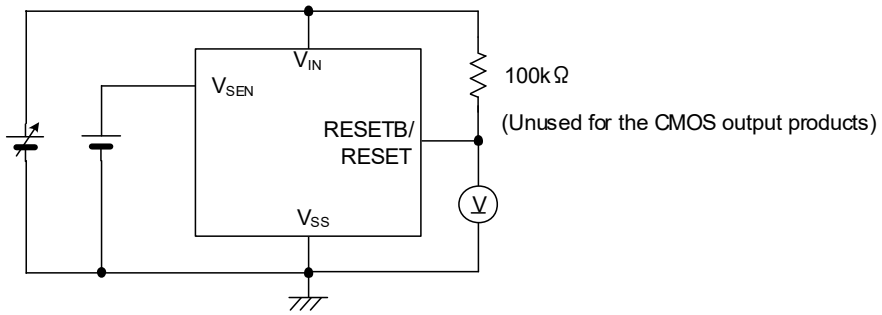
CIRCUIT④



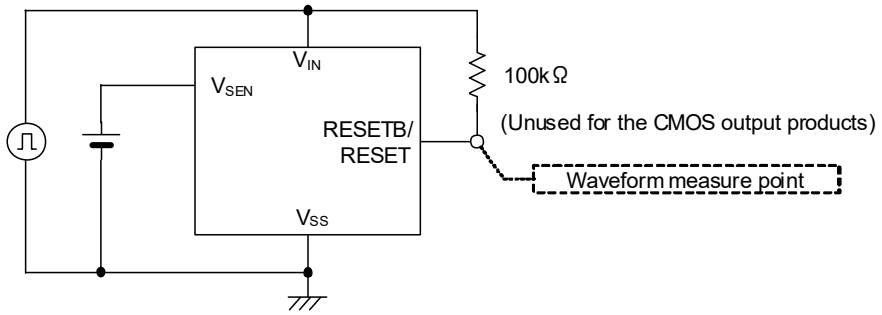
*“RESETB” is A/B type, and “RESET” is C/D type.

■TEST CIRCUITS

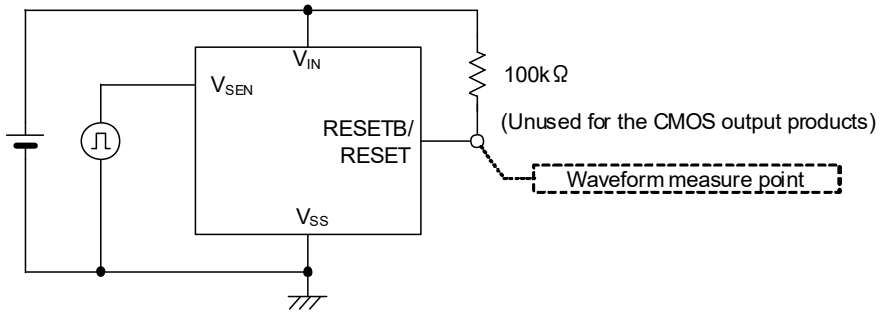
CIRCUIT⑤



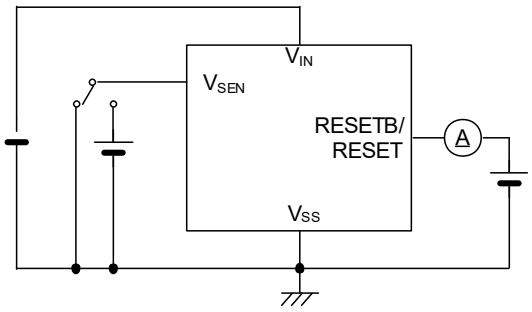
CIRCUIT⑥



CIRCUIT⑦



CIRCUIT⑧



*“RESETB” is A/B type, and “RESET” is C/D type.

■ OPERATIONAL DESCRIPTION (V_{IN} and V_{SEN} are separated)

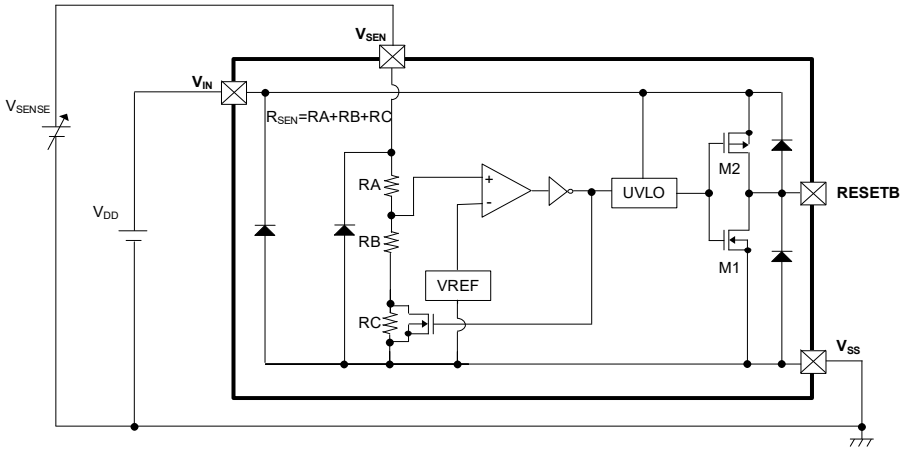


Fig. 1: Typical block diagram (CMOS output/Active Low product)

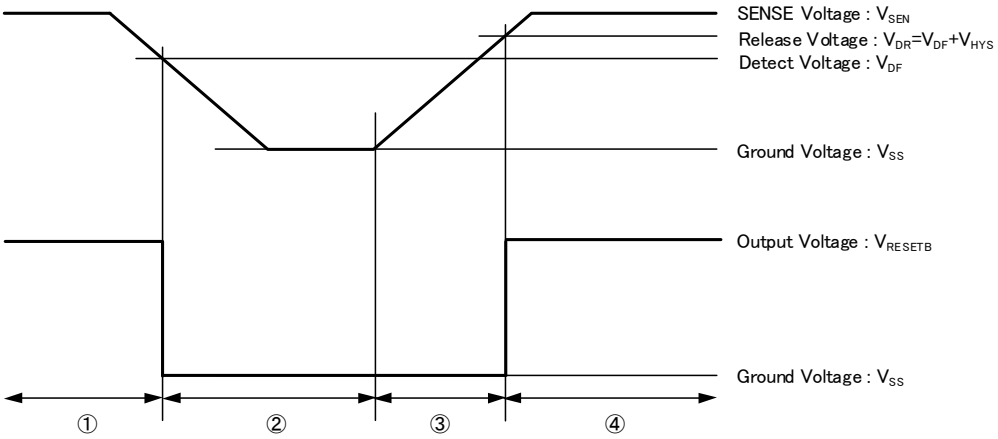


Fig. 2: Timing chart of Fig. 1 (V_{DD}=6.0V)

The circuit operation in the above representative circuit example will be explained using the timing chart.

(1) Assume that the V_{SEN} pin voltage in the initial state is higher than the release voltage (V_{DR}), and V_{SEN} gradually decreases. In a state where a voltage higher than the detection voltage (V_{DF}) is applied to the V_{SEN} pin voltage, the input voltage (V_{IN}) is output to the RESETB pin (released state).
* In the case of N-ch open drain output products, the RESETB pin goes into a high impedance state. When the output is pulled up, the pull-up voltage is output to the RESETB pin.

(2) When the V_{SEN} pin voltage drops below the detection voltage (V_{DF}), the ground potential (V_{SS}) is output to the RESETB pin (detection state).

(3) The RESETB pin keeps the ground potential until the V_{SEN} pin voltage goes up to release voltage (V_{DR}).

(4) When the V_{SEN} pin voltage becomes equal to or higher than the release voltage (V_{DR}), the input voltage (V_{IN}) is output to the RESETB pin.
* In the case of N-ch open drain output products, the RESETB pin goes into a high-impedance state in the same way as in 1), and if the output is pulled up, the pull-up voltage is output to the RESETB pin.

* The difference between the release voltage (V_{DR}) and the detect voltage (V_{DF}) is the hysteresis width (V_{HYS}).

Note: In the above explanation, the operation time of the circuit is omitted for simplicity of explanation.
For Active High products, please reverse the output logic of RESETB pin voltage.

■ OPERATIONAL DESCRIPTION (V_{IN} and V_{SEN} are connected)

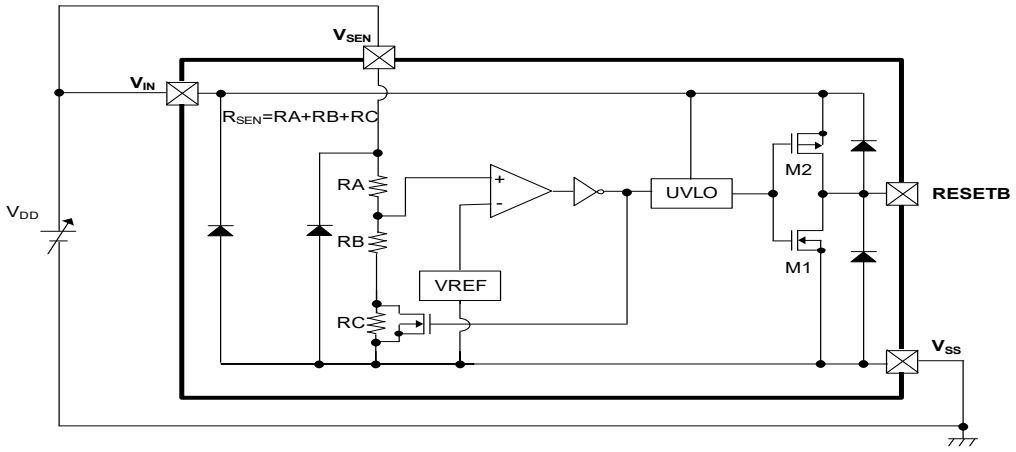


Fig. 3: Typical block diagram (CMOS output/Active Low product)

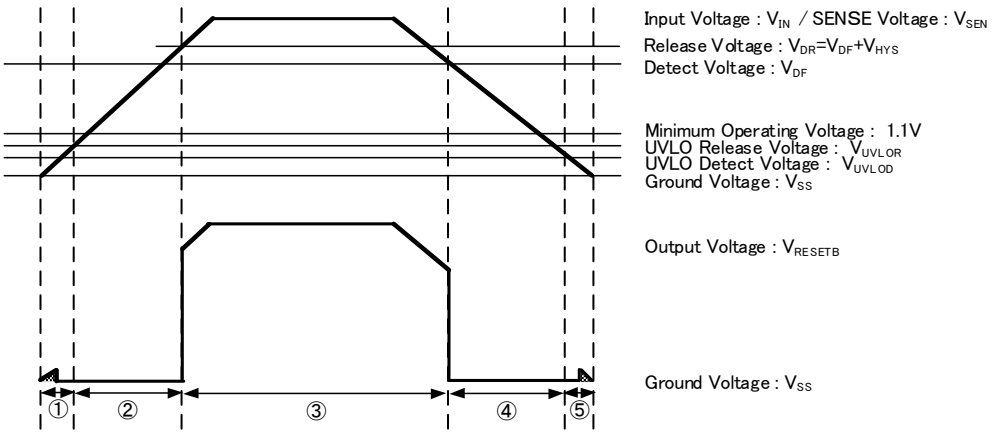


Fig. 4: Timing chart of Fig. 3

The circuit operation in the above representative circuit example will be explained using the timing chart.

(1) As for the voltage detectors, when the input voltage is under the minimum operation voltage, an unstable voltage will be output to the RESETB pin. However, the XC6136C series (CMOS output product) incorporates an under-voltage lockout (UVLO) circuit which can minimize the floating of the RESETB terminal caused by a voltage lower than the minimum operation voltage at V_{IN}. Please refer to the specifications of the undefined operation on the P.7 of the electrical characteristics.
* Pull-up voltage may be output to the RESETB terminal when the output terminal is pulled up with an N-ch open drain output product.

(2) The RESETB pin keeps the ground potential (release state) until the V_{SEN} pin voltage goes up to the release voltage (V_{DR}), even exceeding the UVLO release voltage.

(3) When the V_{SEN} pin voltage becomes equal to or higher than the release voltage (V_{DR}), the input voltage (V_{IN}) is output to the RESETB pin.
* Pull-up voltage may be output to the RESETB terminal when the output terminal is pulled up with an N-ch open drain output product.

(4) When the input voltage (V_{IN}) drops below the detection voltage (V_{DF}), the ground potential (V_{SS}) is output to the RESETB pin (detection state).* N-ch open drain output products are also the same.

(5) In the case that the input voltage is under the minimum operation voltage, same as ①, with the built-in UVLO circuit, the floating of the RESETB terminal can be minimized.

* The difference between the release voltage (V_{DR}) and the detect voltage (V_{DF}) is the hysteresis width (V_{HYS}).
Note: In the above explanation, the operation time of the circuit is omitted for simplicity of explanation.
For Active High products, please reverse the output logic of RESETB pin voltage.

■NOTES ON USE

(1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

(2) The power input pin voltage may fall due to the flow through current during IC operation and the resistance component between the power supply and the power input pin.
In the case of CMOS output, a drop in the power input pin voltage may occur in the same way due to the output current. When this happens, if the power input pin voltage drops below the minimum operating voltage, a malfunction may occur.

(3) Note that large, sharp changes of the power input pin voltage may lead to malfunction.

(4) Since the power supply noise may cause malfunction, please fully evaluate with an actual system. As necessary, please take measures such as inserting a capacitor between V_{IN} and V_{SS}.

(5) When an N-ch open drain output is used, the V_{RESETB} voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.

At detection:
$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{ON})$
V_{pull} : Voltage after pull-up
R_{ON}(*1) : ON resistance of N-ch driver M1 (calculated from V_{RESETB}/I_{RBOUTN} based on electrical characteristics)

Example: When V_{IN}=2.0V(*2), R_{ON} = 0.3V / (4.1×10^{-3} A) ≒ 73.2Ω (MAX.)
If it is desired to make V_{RESETB} at detection 0.1V or less when V_{pull} is 3.0V,
$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{ON} = \{ (3V / 0.1V) - 1 \} \times 73.2Ω$ ≒ 2.1kΩ

Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.1kΩ or higher.
(*1) Note that R_{ON} becomes larger as V_{IN} becomes smaller.
(*2) For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

At release:
$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{off})$
V_{pull} : Voltage after pull-up
R_{off} : Resistance when N-ch driver M1 is OFF (calculated from V_{RESETB}/I_{LEAKN} based on electrical characteristics)

Example: When V_{pull} is 6.0V, R_{off} = 6V / (0.1×10^{-6} A) = 60MΩ (MIN.).
If it is desired to make V_{RESETB} 5.99V or higher,
$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{off} = \{ (6V / 5.99V) - 1 \} \times 60 \times 10^{6}Ω$ ≒ 100kΩ

Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100kΩ or less.The above V_{RESETB} voltage is an example calculation of Active Low products.
To calculate the V_{RESET} voltage (Active High product), calculate by inverting the logic at detection and release.

(6) As for the products of detect voltage 0.5V~1.0V, in the case that the V_{SEN} voltage is over than 1.0V, a current will flow at the inner diode which will cause R_{SEN}(SENSE Resistance) drops lower than the standard value, consequently ,the current flowing at V_{SEN} increases. (Shown as following chart).

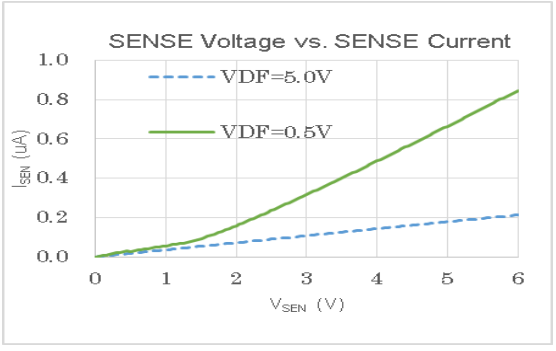
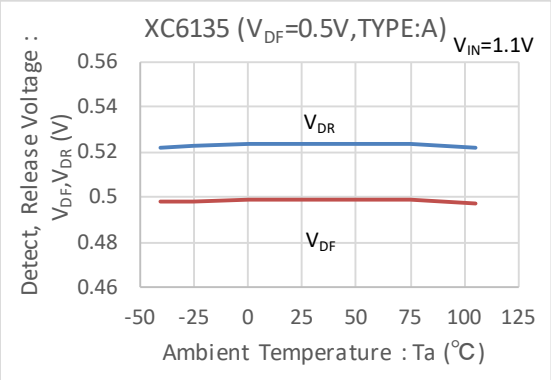


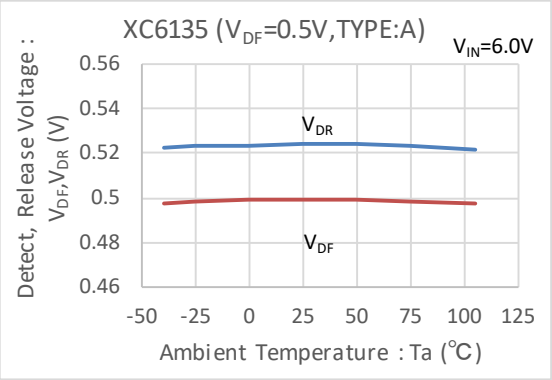
Fig.5 : I_{SEN} Current Comparison between V_{DF}=0.5V and V_{DF}=5.0V

(7) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

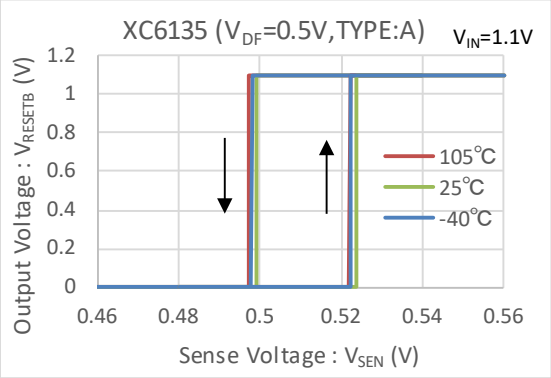
■TYPICAL PERFORMANCE CHARACTERISTICS

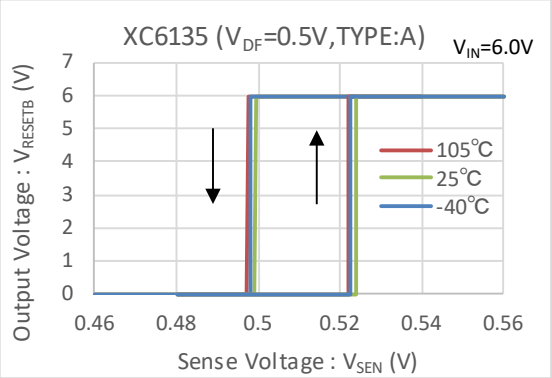
(1)Detect, Release Voltage vs. Ambient Temperature



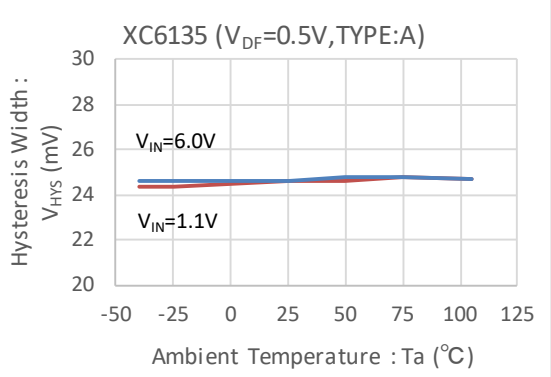


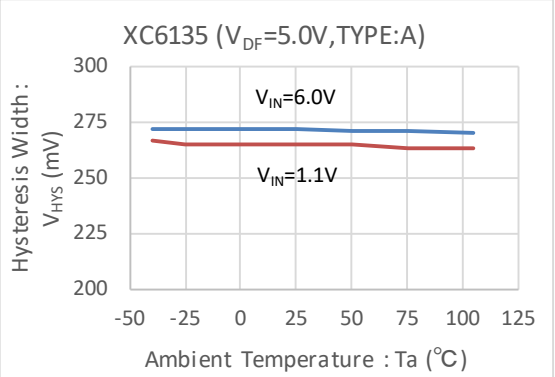
(2)Output Voltage vs. Sense Voltage

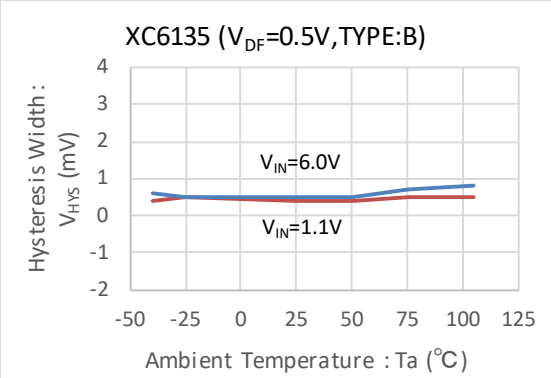


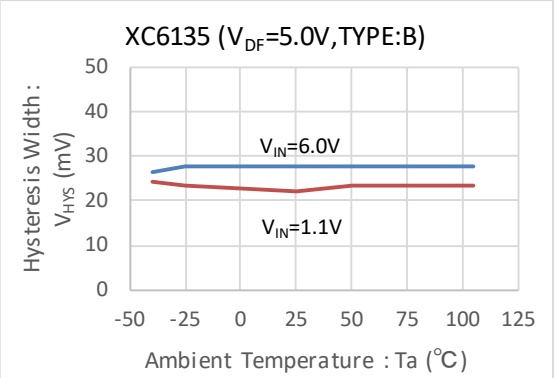


(3)Hysteresis Width vs. Ambient Temperature



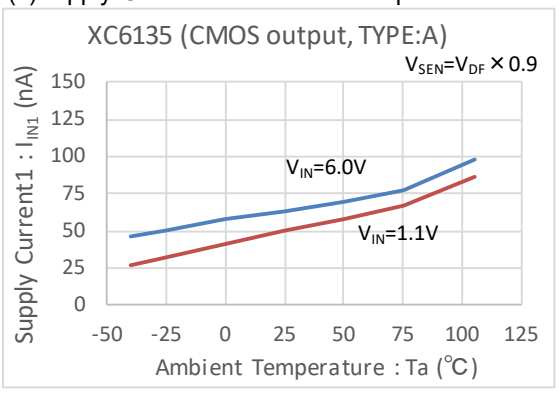


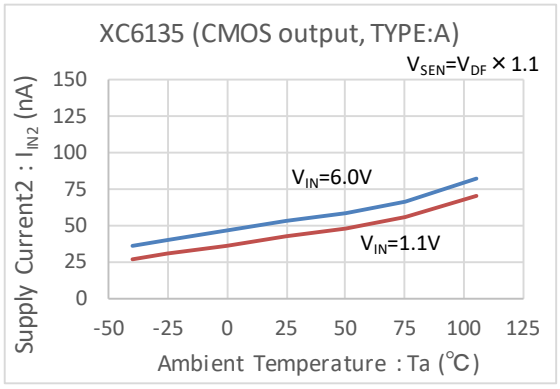




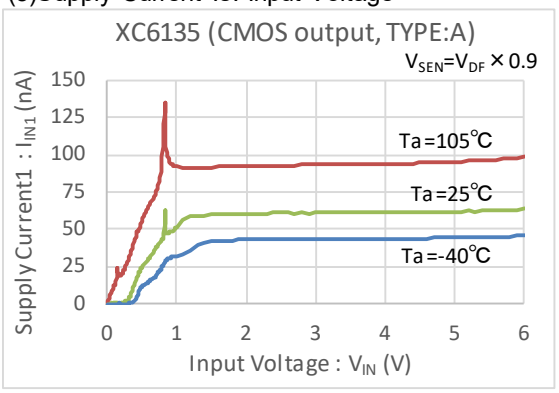
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

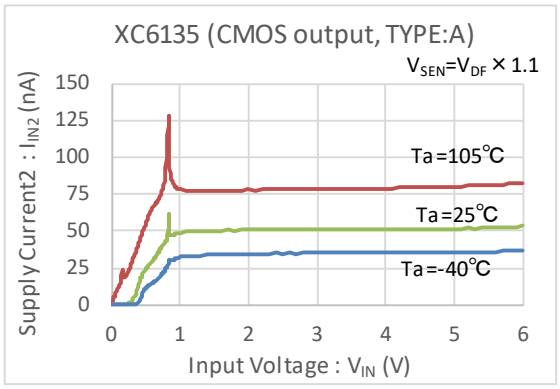
(4)Supply Current vs. Ambient Temperature



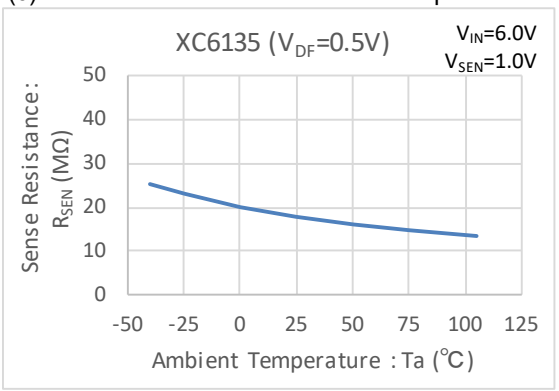


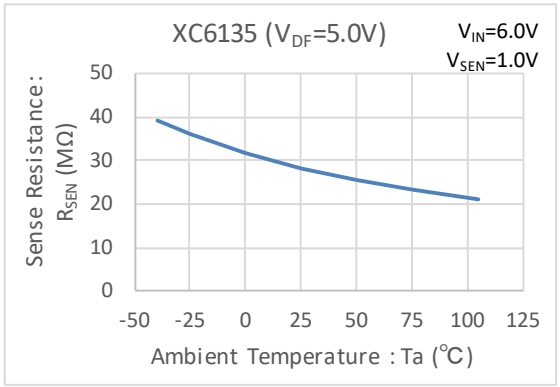
(5)Supply Current vs. Input Voltage



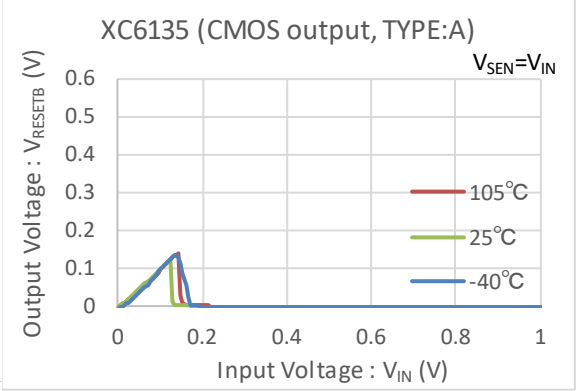


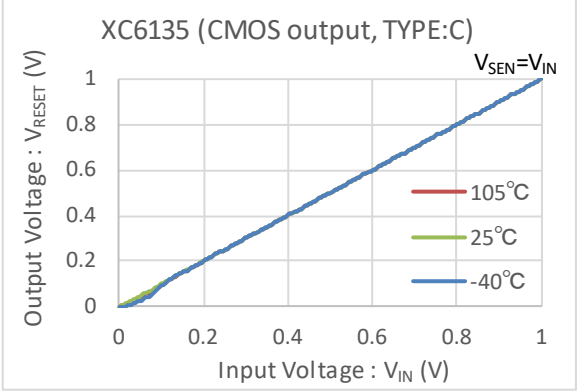
(6)Sense Resistance vs. Ambient Temperature





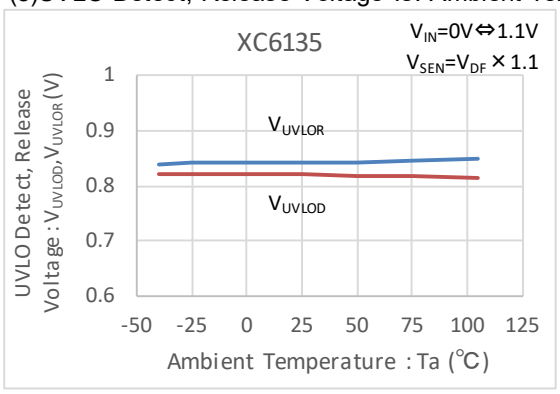
(7)Output Voltage vs. Input Voltage (VIN<Operating Voltage)



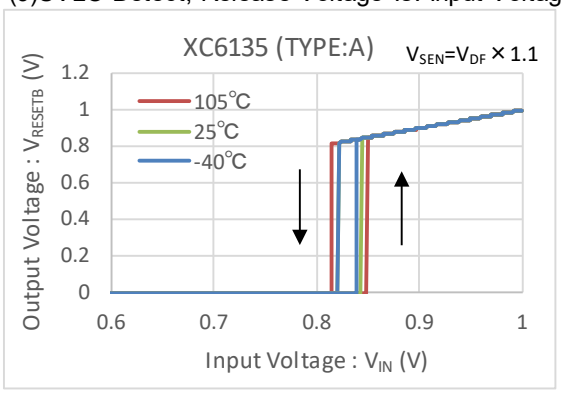


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

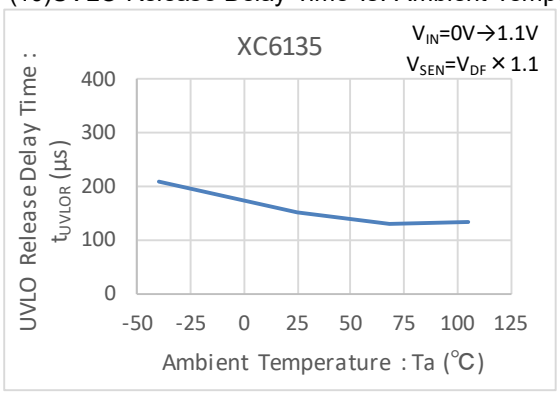
(8)UVLO Detect, Release Voltage vs. Ambient Temperature



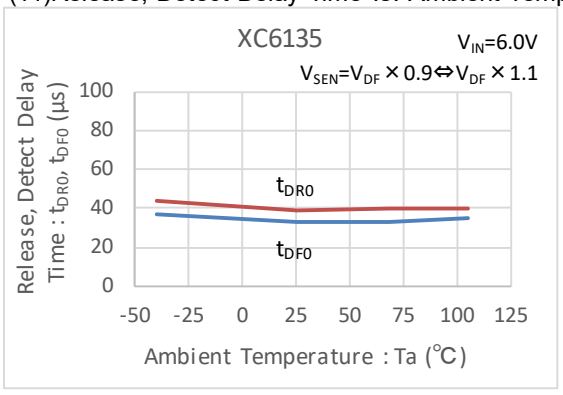
(9)UVLO Detect, Release Voltage vs. Input Voltage



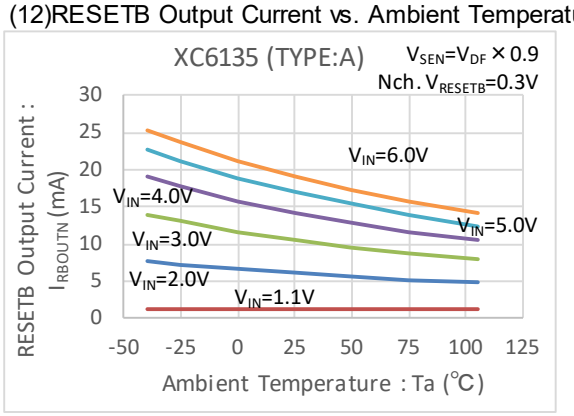
(10)UVLO Release Delay Time vs. Ambient Temperature

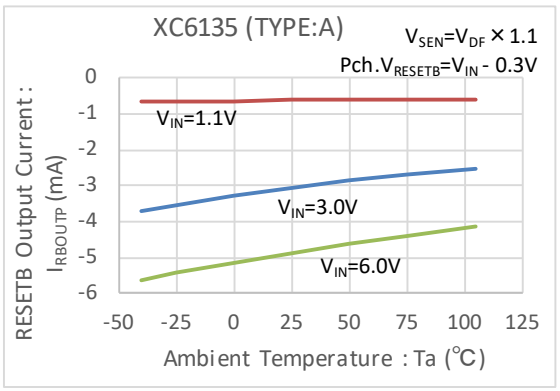


(11)Release, Detect Delay Time vs. Ambient Temperature

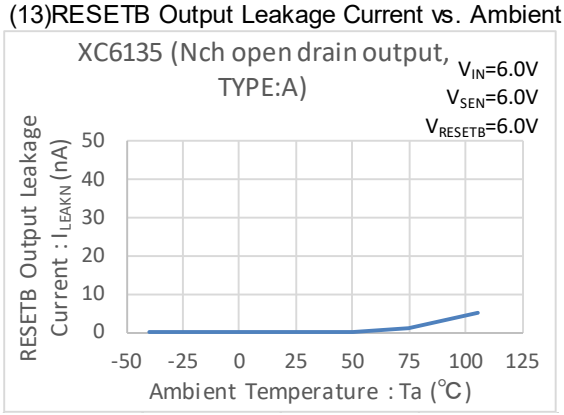


(12)RESETB Output Current vs. Ambient Temperature





(13)RESETB Output Leakage Current vs. Ambient Temperature



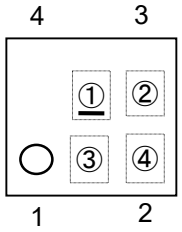
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

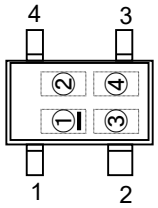
PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SSOT-24	SSOT-24 PKG	Standard Board	SSOT-24 Power Dissipation
		JESD51-7 Board	
SOT-25	SOT-25 PKG	Standard Board	SOT-25 Power Dissipation
		JESD51-7 Board	
USPQ-4B05	USPQ-4B05 PKG	Standard Board	USPQ-4B05 Power Dissipation

■MARKING RULE

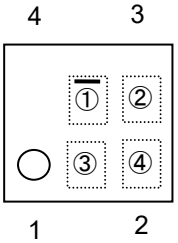
USPQ-4B05 (with underline mark ①)



SSOT-24 (with underline mark①)



USPQ-4B05 (with overline mark①)



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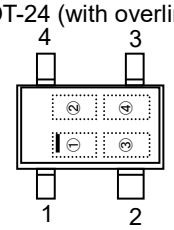
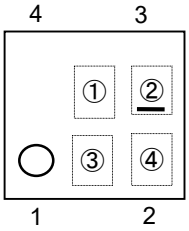
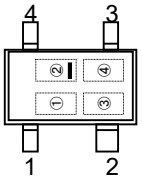


USPQ-4B05 (with underline mark②)



SSOT-24 (with underline mark②)



① represents products series

MARK	Registration order	PRODUCT SERIES
$\underline{X}$ (with underline)	1	XC6135******-G
$\overline{1}$ (with overline)	2	
$\overline{3}$ (with overline)	3	
$\overline{5}$ (with overline)	4	
A	5	
B	6	
C	7	

*Mark ① is a common symbol and Mark ② is assigned a sequential number.
(The sequential numbers of Mark② are numbered stating from "0".)

② represents internal sequential number

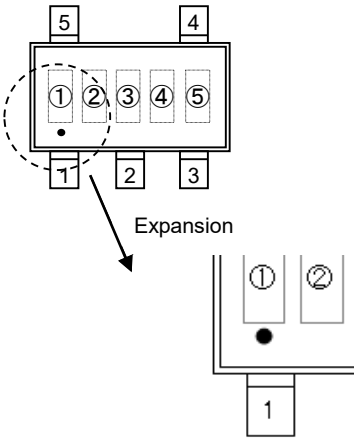
MARK①	MARK ①Line	MARK ②Line
$\underline{X}$	with underline	-
$\overline{1}$	with overline	-
$\overline{3}$	with overline	-
$\overline{5}$	with overline	-
A	-	with underline
B	-	with underline
C	-	with underline

sequential number 0～9、A～Z repeated.(G, I, J, O, Q, W excluded)

③,④ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～A9, AA～Z9 repeated.
(G, I, J, O, Q, W excluded)

■ MARKING RULE

SOT-25 (under dot)



① represents products series

MARK	PRODUCT SERIES
X	XC6135******-G

※Mark ① gets a serial number with a common symbol.
※Under dot

②③ represents internal sequential number

sequential number 01～09、10～99、A0～A9、B0～B9･･･Z0～Z9、AA～AZ、BA～BZ･･･ZA～ZZ repeated.
(G, I, J, O, Q, W excluded)

④⑤ represents production lot number
01～09、0A～0Z、11･･･9Z、A1～A9、AA･･･Z9、ZA～ZZ repeated
(G, I, J, O, Q, W excluded)
* No character inversion used.
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