

XC6136 Series

ETR02042-004

Ultra-Low Power (88nA) Voltage Detector

■ GENERAL DESCRIPTION

The XC6136 series is ultra-low power voltage detector with high accuracy detection, manufactured using CMOS process and laser trimming technologies.

The device is available in both CMOS and N-channel open drain output configurations. Also detect logic is available in both RESETB (Active Low) and RESET (Active High).

Ultra-small low height package USPQ-4B05 and standard packages SSOT-24 and SOT-25 which are ideally suited for small design of portable devices and high densely mounting applications.

UVLO circuit is implemented in order to suppress the floating of RESETB pin (undefined operation) when V_{IN} voltage is lower than the minimum operating voltage.

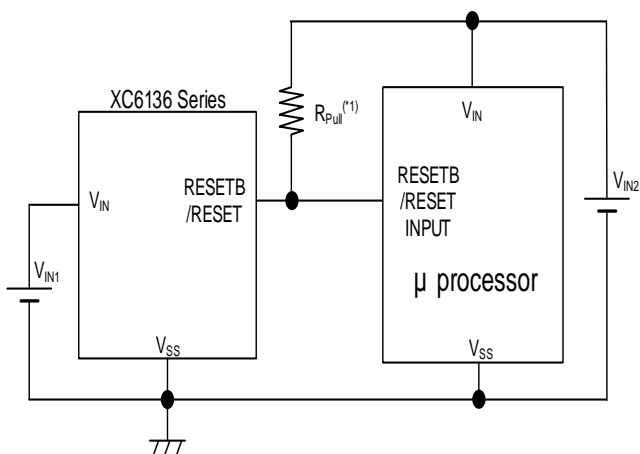
■ APPLICATIONS

- Energy Harvesting
- Wearable devices
- Smart meter
- Microprocessor logic reset circuitry
- System battery life and charge voltage monitors
- Power-on reset circuits
- Power failure Detection

■ FEATURES

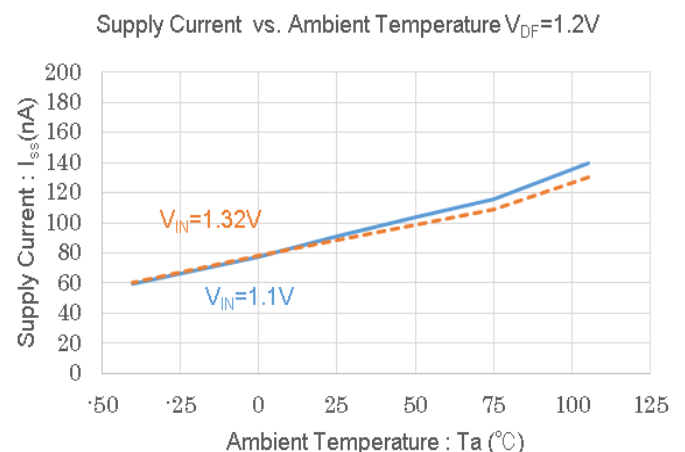
| | |
|---|--|
| Ultra-Low Power | : 91nA TYP.(@detect, $V_{DF}=1.2V$, $V_{IN}=1.1V$) : 88nA TYP.(@release, $V_{DF}=1.2V$, $V_{IN}=1.32V$) |
| High Accuracy | : $\pm 0.8\%$ ($V_{DF} \leq 3.0V$, $T_a=25^\circ C$) : $\pm 1.0\%$ ($3.1V \leq V_{DF}$, $T_a=25^\circ C$) : $\pm 2.5\%$ ($V_{DF} \leq 3.0V$, $T_a=-40^\circ C \sim 105^\circ C$) : $\pm 2.7\%$ ($3.1V \leq V_{DF}$, $T_a=-40^\circ C \sim 105^\circ C$) |
| Temperature Characteristics | : $\pm 50ppm/^\circ C$ (TYP.) |
| Hysteresis width | : TYPE:A/C $V_{DF} \times 5.0\%$ (TYP.) : TYPE:B/D 2mV ~ 28mV (TYP.) |
| Detect voltage range | : 1.2V ~ 5.0V (0.1Vstep) |
| Operating voltage range | : 1.1V ~ 6.0V |
| Output type | : CMOS : Nch open drain |
| Output logic | : RESETB (Active Low) : RESET (Active High) |
| Undefined operation Protection (CMOS Output only) | : Output pin Voltage 0.38V (MAX: $T_a=-40^\circ C \sim 105^\circ C$) @Power supply Input pin Voltage < operating voltage (MIN.) |
| Packages | : USPQ-4B05, SSOT-24, SOT-25 |
| Environment friendly | : EU RoHS Compliant, Pb Free |

■ TYPICAL APPLICATION CIRCUIT



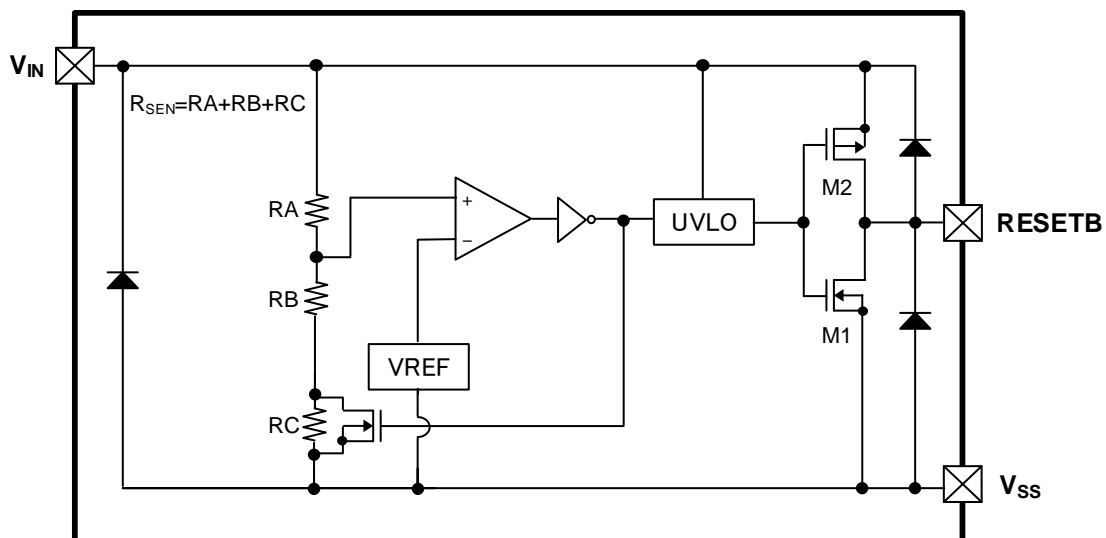
(*) Unused for the CMOS output products

■ TYPICAL PERFORMANCE CHARACTERISTICS



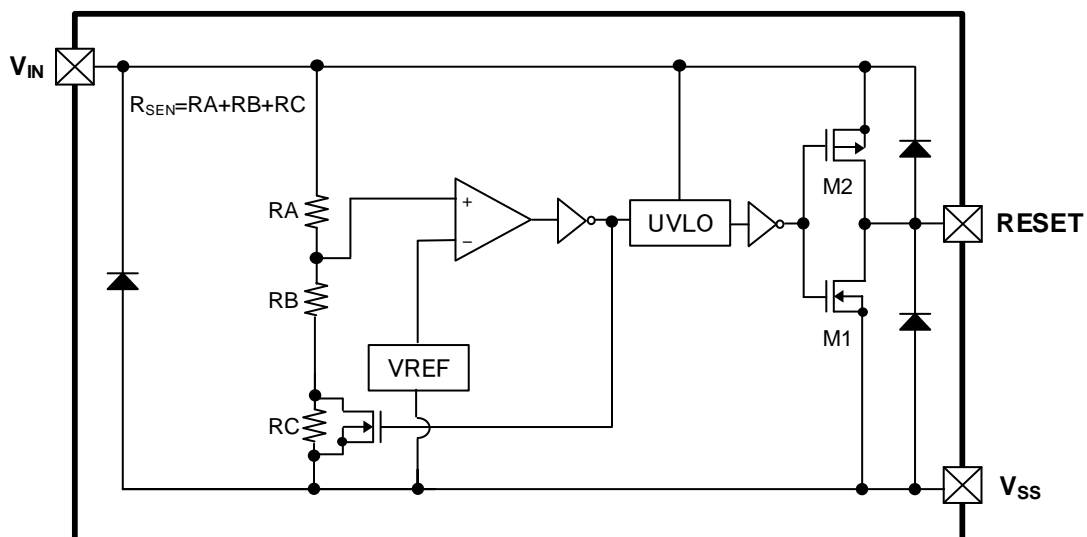
■ BLOCK DIAGRAMS

(1) XC6136C Series A/B type (RESETB OUTPUT:CMOS output/Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

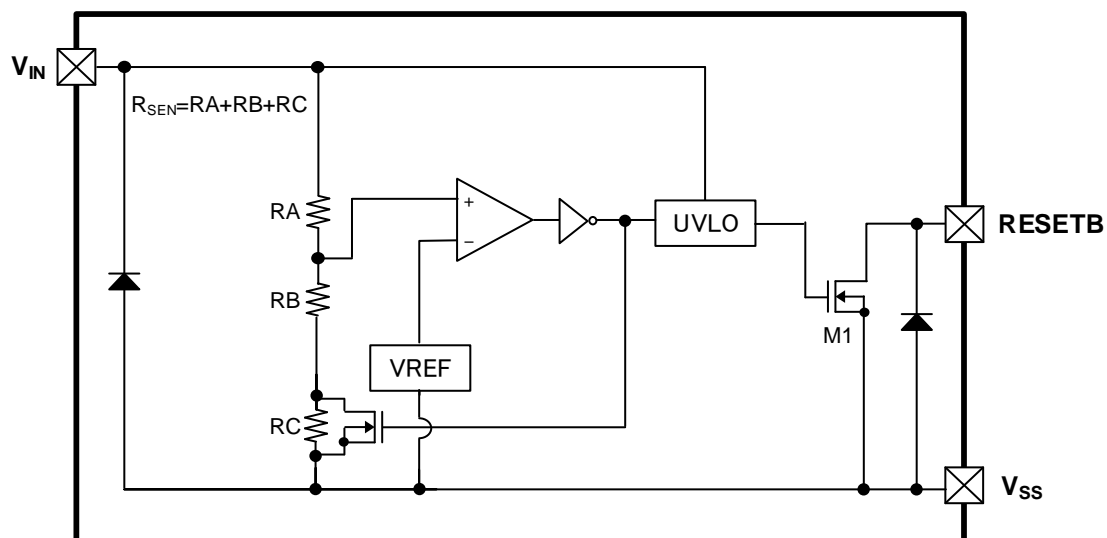
(2) XC6136C Series C/D type (RESET OUTPUT:CMOS output /Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

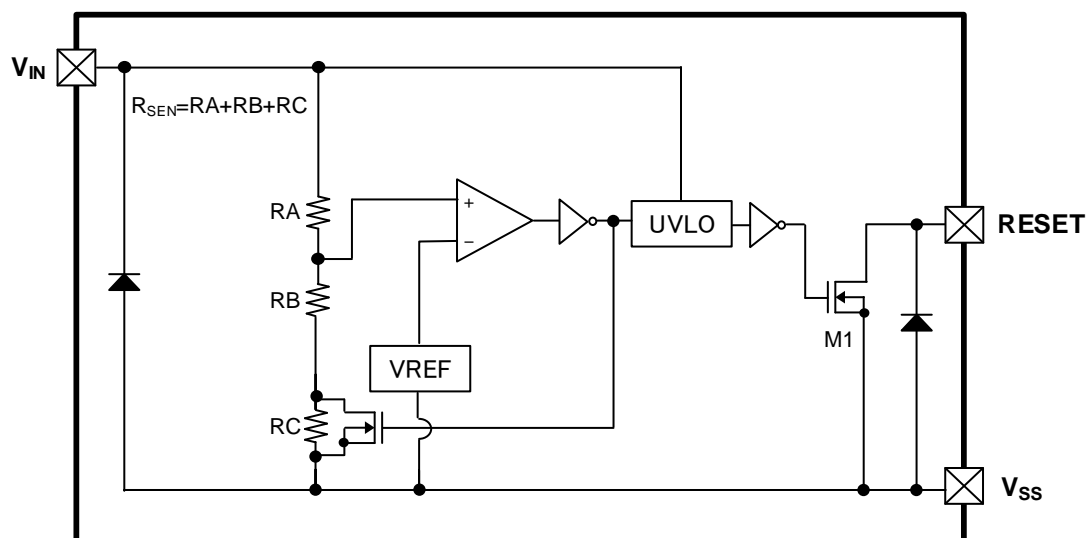
■ BLOCK DIAGRAMS

(3) XC6136N Series A/B type (RESETB OUTPUT: Nch open drain output /Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

(4) XC6136N Series C/D type (RESET OUTPUT: Nch open drain output /Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

PRODUCT CLASSIFICATION

Ordering Information

XC6136①②③④⑤⑥-⑦^(*)

| DESIGNATOR | ITEM | SYMBOL | DESCRIPTION |
|---------------------|----------------------|---------|---------------------------------------|
| ① | Output Configuration | C | CMOS output |
| | | N | Nch open drain output |
| ②③ | Detect Voltage | 12 ~ 50 | e.g. 1.2V → ②=1, ③=2 |
| ④ | Type | A | Refer to Selection Guide |
| | | B | |
| | | C | |
| | | D | |
| ⑤⑥-⑦ ^(*) | PKG | 9R-G | USPQ-4B05 (5,000pcs/Reel) |
| | | NR-G | SSOT-24 (3,000pcs/Reel) |
| | | MR-G | SOT-25 (3,000pcs/Reel) ⁽²⁾ |

^(*) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

⁽²⁾ SOT-25 uses Cu bonding wires.

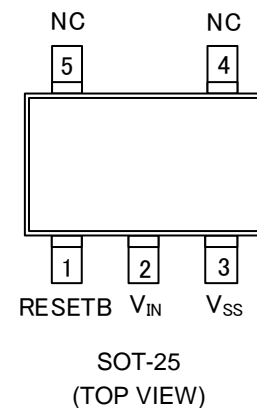
Selection Guide

| TYPE | RESETB/RESET OUTPUT | HYSTERESIS |
|------|---------------------|---------------------------------|
| A | Active Low | $V_{DF} \times 5.0\%$ (TYP) |
| B | ↑ | 2mV ~ 28mV (TYP) ^(*) |
| C | Active High | $V_{DF} \times 5.0\%$ (TYP) |
| D | ↑ | 2mV ~ 28mV (TYP) ^(*) |

^(*) Refer to SPEC TABLE.

PIN CONFIGURATION

Type : A/B



Type : C/D



*The dissipation pad for the USPQ-4B05 package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to V_{SS} (No. 3) pin.

■ PIN ASSIGNMENT

| PIN NUMBER | | | PIN NAME | FUNCTION |
|------------|---------|--------|-----------------|--|
| USPQ-4B05 | SSOT-24 | SOT-25 | | |
| 1 | 3 | 1 | RESETB | Reset Output (Active Low) ^{(*)1} |
| | | | RESET | Reset Output (Active High) ^{(*)2} |
| 2 | 1 | 4, 5 | NC | No Connection |
| 3 | 2 | 3 | V _{SS} | Ground |
| 4 | 4 | 2 | V _{IN} | Power Input |

^{(*)1} Type A,B (Refer to the ④ in Ordering Information table.)

^{(*)2} Type C,D (Refer to the ④ in Ordering Information table.)

■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | | RATINGS | UNITS | |
|--------------------------------------|-------------------------|---------------------|--------------------|--|-------|--|
| Input Voltage | | V _{IN} | | -0.3 ~ 7.0 | V | |
| Output Voltage | XC6136C ^{(*)2} | V _{RESETB} | V _{RESET} | V _{SS} - 0.3 ~ V _{IN} + 0.3 or 7.0 ^{(*)1} | V | |
| | XC6136N ^{(*)3} | | | V _{SS} - 0.3 ~ 7.0 | V | |
| Output Current | XC6136C ^{(*)2} | I _{RBOUT} | I _{ROUT} | ±50 | mA | |
| | XC6136N ^{(*)3} | | | 50 | | |
| Power Dissipation (Ta=25°C) | USPQ-4B05 | Pd | | 100 | mW | |
| | | | | 550 (40mm x 40mm Standard board) ^{(*)4} | | |
| | | | | 150 | | |
| | SSOT-24 | | | 500 (40mm x 40mm Standard board) ^{(*)4} | | |
| | | | | 680 (JESD51-7 board) ^{(*)4} | | |
| | SOT-25 | | | 250 | | |
| | | | | 600 (40mm x 40mm Standard board) ^{(*)4} | | |
| 760 (JESD51-7 board) ^{(*)4} | | | | | | |
| Operating Ambient Temperature | | Topr | | -40 ~ 105 | °C | |
| Storage Temperature | | Tstg | | -55 ~ 125 | °C | |

* All voltages are described based on the V_{SS}.

^{(*)1} The maximum value should be either V_{IN}+0.3V or 7.0V in the lowest.

^{(*)2} CMOS output

^{(*)3} Nch open drain output

^{(*)4} The power dissipation figure shown is PCB mounted and is for reference only.

Please refer to PACKAGING INFORMATION for the mounting condition.

ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | Ta=25°C | | | -40°C ≤ Ta ≤ 105°C ⁽⁵⁾ | | | UNITS | CIRCUIT | |
|--|--|--|------------------------------|--------------------------|------------------------------|-----------------------------------|--------------------------|------------------------------|---------------------|---------|---|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | | |
| Operating Voltage | V _{IN} | | 1.1 | | 6.0 | 1.1 | | 6.0 | V | ① | |
| MIN Voltage Holding the Detection ⁽³⁾ | V _{INL} | V _{IN} =V _{SEN} | - | - | 0.4 | - | - | 0.4 | V | | |
| Detect Voltage | V _{DF} | V _{DF(T)} ⁽¹⁾ =1.2V~3.0V | V _{DF(T)} x0.992 | V _{DF(T)} | V _{DF(T)} x1.008 | V _{DF(T)} x0.975 | V _{DF(T)} | V _{DF(T)} x1.025 | V | | |
| | | V _{DF(T)} ⁽¹⁾ =3.1V~5.0V | V _{DF(T)} x0.990 | V _{DF(T)} | V _{DF(T)} x1.010 | V _{DF(T)} x0.973 | V _{DF(T)} | V _{DF(T)} x1.027 | V | | |
| Temperature Characteristics | ΔV _{DF} / (ΔT _{opr} · V _{DF}) | -40°C ≤ T _{opr} ≤ 105°C | - | ±50 | - | - | ±50 | - | ppm/°C | | |
| Hysteresis Width (TYPE: A/C) | V _{HYS} | | V _{DF} x0.032 | V _{DF} x0.05 | V _{DF} x0.068 | V _{DF} x0.03 | V _{DF} x0.05 | V _{DF} x0.07 | V | | |
| Hysteresis Width (TYPE: B/D) | | | - | E-1 ⁽²⁾ | - | E-2 ⁽²⁾ | V | | | | |
| Supply Current1 (TYPE:A/B) CMOS output | I _{ss1} | V _{IN} =V _{DF} x0.9 | - | E-3 ⁽²⁾ | - | - | - | - | E-4 ⁽²⁾ | nA | ② |
| Supply Current1 (TYPE:C/D) CMOS output | | | | | | | | | E-5 ⁽²⁾ | | |
| Supply Current1 (TYPE:A/B/C/D) Nch open drain output | | | | | | | | | E-6 ⁽²⁾ | | |
| Supply Current2 (TYPE:A/B) CMOS output | I _{ss2} | V _{IN} =V _{DF} x1.1 | - | E-7 ⁽²⁾ | - | - | - | - | E-8 ⁽²⁾ | | |
| Supply Current2 (TYPE:C/D) CMOS output | | | | | | | | | E-9 ⁽²⁾ | | |
| Supply Current2 (TYPE:A/B/C/D) Nch open drain output | | | | | | | | | E-10 ⁽²⁾ | | |
| Peak of Undefined Operation ⁽⁴⁾ (TYPE:A/B) | V _{UNO} | V _{IN} <0.4V | - | 0.1 | 0.38 | - | 0.1 | 0.38 | V | ③ | |
| UVLO Release Voltage | V _{UVLOR} | V _{IN} =0V→1.1V | - | 0.82 | - | - | 0.82 | - | V | - | |
| UVLO Detect Voltage | V _{UVLOD} | V _{IN} =1.1V→0V | - | 0.79 | - | - | 0.79 | - | V | - | |
| UVLO Release Delay Time | t _{UVLOR} | V _{IN} = 0V→1.1V | - | 157 | - | - | 157 | - | μs | - | |

⁽¹⁾ V_{DF(T)}: Nominal detect voltage

⁽²⁾ Refer to SPEC TABLE(P.8,9).

⁽³⁾ For XC6136C (CMOS output) only. V_{IN} value where RESETB <0.05V or RESET > V_{IN}.0.05V.

⁽⁴⁾ XC6136C(CMOS output)only.

⁽⁵⁾ The ambient temperature range (-40°C ≤ Ta ≤ 105°C) is a design value.

ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | Ta=25°C | | | -40°C ≤ Ta ≤ 105°C ⁽¹⁷⁾ | | | UNITS | CIRCUIT |
|--|--|---|---------|-------|------|------------------------------------|-------|-------|-------|---------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | |
| Release Delay Time ⁽⁶⁾ | t _{DR0} | V _{IN} = V _{DF} × 0.9 → V _{DF} × 1.1 | - | 44 | 200 | - | 44 | 224 | μs | ④ |
| Detect Delay Time ⁽⁷⁾ | t _{DF0} | V _{IN} = V _{DF} × 1.1 → V _{DF} × 0.9 | - | 40 | 170 | - | 40 | 184 | | |
| RESETB Output Current | I _{RBOUTN} | Nch. V _{RESETB} = 0.3V | | | | | | | mA | ⑤ |
| | | V _{IN} = 1.1V | 0.3 | 1.4 | - | 0.2 | 1.4 | - | | |
| | | V _{IN} = 2.0V ⁽⁸⁾ | 4.1 | 6.2 | - | 3.1 | 6.2 | - | | |
| | | V _{IN} = 3.0V ⁽⁹⁾ | 8.1 | 10.8 | - | 4.3 | 10.8 | - | | |
| | V _{IN} = 4.0V ⁽¹⁰⁾ | 11.2 | 14.3 | - | 6.2 | 14.3 | - | | | |
| | I _{RBOUTP} ⁽¹¹⁾ | Pch. V _{RESETB} = V _{IN} - 0.3V | | | | | | | | |
| V _{IN} = 3.0V ⁽¹²⁾ | | - | -3.2 | -1.4 | - | -3.2 | -1.3 | | | |
| V _{IN} = 6.0V | | - | -5.1 | -2.9 | - | -5.1 | -2.6 | | | |
| RESET Output Current | I _{ROUTN} | Nch. V _{RESET} = 0.3V | | | | | | | mA | ⑤ |
| | | V _{IN} = 2.0V ⁽¹³⁾ | 4.1 | 6.2 | - | 3.1 | 6.2 | - | | |
| | | V _{IN} = 3.0V ⁽¹²⁾ | 8.1 | 10.8 | - | 4.3 | 10.8 | - | | |
| | | V _{IN} = 4.0V ⁽¹⁴⁾ | 11.2 | 14.3 | - | 6.2 | 14.3 | - | | |
| | | V _{IN} = 5.0V ⁽¹⁵⁾ | 13.7 | 17.1 | - | 7.3 | 17.1 | - | | |
| | V _{IN} = 6.0V | 15.7 | 19.3 | - | 8.1 | 19.3 | - | | | |
| | I _{ROUTP} ⁽¹⁶⁾ | Pch. V _{RESET} = V _{IN} - 0.3V | | | | | | | | |
| | | V _{IN} = 1.1V | - | -0.7 | -0.2 | - | -0.7 | -0.15 | | |
| V _{IN} = 3.0V ⁽⁹⁾ | | - | -3.2 | -1.4 | - | -3.2 | -1.3 | | | |
| RESETB Output Leakage Current | I _{LEAKN} ⁽¹⁶⁾ | V _{IN} = 6.0V, Nch. V _{RESETB} = 6.0V | - | 0.01 | 0.1 | - | 0.01 | 0.3 | μA | |
| | I _{LEAKP} | V _{IN} = 1.1V, Pch. V _{RESETB} = 0V | - | -0.01 | - | - | -0.01 | - | | |
| RESET Output Leakage Current | I _{LEAKN} ⁽¹⁶⁾ | V _{IN} = 1.1V, Nch. V _{RESET} = 6.0V | - | 0.01 | 0.1 | - | 0.01 | 0.3 | | |
| | I _{LEAKP} | V _{IN} = 6.0V, Pch. V _{RESET} = 0V | - | -0.01 | - | - | -0.01 | - | | |

⁽⁶⁾ RESETB product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches V_{IN} × 90%.

RESET product: Time from when the V_{IN} pin voltage reaches the release voltage until the reset output pin reaches V_{IN} × 10%
Release voltage (V_{DR}) = Detect voltage (V_{DF}) + Hysteresis width (V_{HYS}).

⁽⁷⁾ RESETB product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches V_{IN} × 10%.

RESET product: Time from when the V_{IN} pin voltage reaches the detect voltage until the reset output pin reaches V_{IN} × 90%.

⁽⁸⁾ For V_{DF(T)} ≥ 2.1V only

⁽⁹⁾ For V_{DF(T)} ≥ 3.1V only.

⁽¹⁰⁾ For V_{DF(T)} ≥ 4.1V only.

⁽¹¹⁾ For XC6136C (CMOS output) only.

⁽¹²⁾ For V_{DF(T)} ≤ 2.9V only.

⁽¹³⁾ For V_{DF(T)} ≤ 1.9V only.

⁽¹⁴⁾ For V_{DF(T)} ≤ 3.8V only.

⁽¹⁵⁾ For V_{DF(T)} ≤ 4.8V only.

⁽¹⁶⁾ Max. value is for XC6136N (Nch open drain).

⁽¹⁷⁾ The ambient temperature range (-40°C ≤ Ta ≤ 105°C) is a design Value.

ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

| NOMINAL DETECT VOLTAGE(V) | E-1 | | E-2 | | E-3 | | E-4 | | E-5 | | E-6 | |
|---------------------------------|-----------------------|------|--------------------|------|----------------------|------|--------------------|------|------|------|------|------|
| | Ta=25°C | | -40°C ≤ Ta ≤ 105°C | | Ta=25°C | | -40°C ≤ Ta ≤ 105°C | | | | | |
| | Hysteresis Width (mV) | | | | Supply Current1 (nA) | | | | | | | |
| V _{DF(T)} | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. |
| 1.2 | 2 | 4.8 | 2 | 5.3 | 91 | 213 | 91 | 431 | 91 | 325 | 91 | 338 |
| 1.3 | 2 | 5.2 | 2 | 5.7 | 94 | 218 | 94 | 437 | 94 | 331 | 94 | 345 |
| 1.4 | 2 | 5.6 | 2 | 6.2 | 98 | 224 | 98 | 444 | 98 | 338 | 98 | 351 |
| 1.5 | 2 | 6.0 | 2 | 6.6 | 101 | 229 | 101 | 451 | 101 | 344 | 101 | 358 |
| 1.6 | 2 | 6.4 | 2 | 7.1 | 104 | 235 | 104 | 457 | 104 | 351 | 104 | 364 |
| 1.7 | 3 | 6.8 | 3 | 7.5 | 108 | 240 | 108 | 464 | 108 | 357 | 108 | 371 |
| 1.8 | 3 | 7.2 | 3 | 8.0 | 111 | 245 | 111 | 471 | 111 | 363 | 111 | 377 |
| 1.9 | 3 | 7.9 | 3 | 8.7 | 114 | 251 | 114 | 478 | 114 | 370 | 114 | 384 |
| 2.0 | 3 | 8.6 | 3 | 9.5 | 117 | 256 | 117 | 484 | 117 | 376 | 117 | 390 |
| 2.1 | 4 | 9.4 | 4 | 10 | 121 | 262 | 121 | 491 | 121 | 383 | 121 | 397 |
| 2.2 | 4 | 10 | 4 | 11 | 124 | 267 | 124 | 498 | 124 | 389 | 124 | 403 |
| 2.3 | 5 | 11 | 5 | 12 | 127 | 272 | 127 | 504 | 127 | 395 | 127 | 410 |
| 2.4 | 5 | 12 | 5 | 13 | 131 | 278 | 131 | 511 | 131 | 402 | 131 | 416 |
| 2.5 | 6 | 13 | 6 | 14 | 134 | 283 | 134 | 518 | 134 | 408 | 134 | 423 |
| 2.6 | 6 | 14 | 6 | 15 | 137 | 289 | 137 | 524 | 137 | 415 | 137 | 429 |
| 2.7 | 7 | 15 | 7 | 16 | 140 | 294 | 140 | 531 | 140 | 421 | 140 | 436 |
| 2.8 | 8 | 16 | 8 | 17 | 144 | 299 | 144 | 538 | 144 | 427 | 144 | 442 |
| 2.9 | 8 | 17 | 8 | 18 | 147 | 305 | 147 | 545 | 147 | 434 | 147 | 449 |
| 3.0 | 9 | 18 | 9 | 19 | 150 | 310 | 150 | 551 | 150 | 440 | 150 | 455 |
| 3.1 | 9 | 19 | 9 | 20 | 154 | 316 | 154 | 558 | 154 | 447 | 154 | 462 |
| 3.2 | 10 | 20 | 10 | 21 | 157 | 321 | 157 | 565 | 157 | 453 | 157 | 468 |
| 3.3 | 11 | 21 | 11 | 23 | 160 | 326 | 160 | 571 | 160 | 459 | 160 | 475 |
| 3.4 | 12 | 22 | 12 | 24 | 163 | 332 | 163 | 578 | 163 | 466 | 163 | 481 |
| 3.5 | 12 | 23 | 12 | 25 | 167 | 337 | 167 | 585 | 167 | 472 | 167 | 488 |
| 3.6 | 13 | 25 | 13 | 26 | 170 | 343 | 170 | 591 | 170 | 479 | 170 | 494 |
| 3.7 | 14 | 26 | 14 | 28 | 173 | 348 | 173 | 598 | 173 | 485 | 173 | 501 |
| 3.8 | 15 | 27 | 15 | 29 | 177 | 353 | 177 | 605 | 177 | 491 | 177 | 507 |
| 3.9 | 16 | 29 | 16 | 30 | 180 | 359 | 180 | 612 | 180 | 498 | 180 | 514 |
| 4.0 | 17 | 30 | 17 | 32 | 183 | 364 | 183 | 618 | 183 | 504 | 183 | 520 |
| 4.1 | 18 | 32 | 18 | 33 | 186 | 370 | 186 | 625 | 186 | 511 | 186 | 527 |
| 4.2 | 19 | 33 | 19 | 35 | 190 | 375 | 190 | 632 | 190 | 517 | 190 | 533 |
| 4.3 | 20 | 35 | 20 | 36 | 193 | 380 | 193 | 638 | 193 | 523 | 193 | 540 |
| 4.4 | 21 | 36 | 21 | 38 | 196 | 386 | 196 | 645 | 196 | 530 | 196 | 546 |
| 4.5 | 22 | 38 | 22 | 40 | 200 | 391 | 200 | 652 | 200 | 536 | 200 | 553 |
| 4.6 | 23 | 39 | 23 | 41 | 203 | 397 | 203 | 658 | 203 | 543 | 203 | 559 |
| 4.7 | 24 | 41 | 24 | 43 | 206 | 402 | 206 | 665 | 206 | 549 | 206 | 566 |
| 4.8 | 25 | 43 | 25 | 45 | 210 | 407 | 210 | 672 | 210 | 555 | 210 | 572 |
| 4.9 | 26 | 44 | 26 | 46 | 213 | 413 | 213 | 679 | 213 | 562 | 213 | 579 |
| 5.0 | 28 | 46 | 28 | 48 | 216 | 418 | 216 | 685 | 216 | 568 | 216 | 585 |

■ ELECTRICAL CHARACTERISTICS (SPEC TABLE)

Table of Characteristics by Voltage Setting

| NOMINAL DETECT VOLTAGE(V) | E-7 | | E-8 | | E-9 | | E-10 | |
|---------------------------------|----------------------|------|--------------------|------|------|------|------|------|
| | Ta=25°C | | -40°C ≤ Ta ≤ 105°C | | | | | |
| | Supply Current2 (nA) | | | | | | | |
| V _{DF(T)} | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. | TYP. | MAX. |
| 1.2 | 88 | 204 | 88 | 325 | 88 | 474 | 88 | 327 |
| 1.3 | 92 | 211 | 92 | 334 | 92 | 482 | 92 | 336 |
| 1.4 | 95 | 217 | 95 | 342 | 95 | 490 | 95 | 344 |
| 1.5 | 99 | 224 | 99 | 350 | 99 | 498 | 99 | 352 |
| 1.6 | 103 | 230 | 103 | 358 | 103 | 506 | 103 | 360 |
| 1.7 | 107 | 237 | 107 | 366 | 107 | 515 | 107 | 368 |
| 1.8 | 111 | 243 | 111 | 374 | 111 | 523 | 111 | 376 |
| 1.9 | 115 | 250 | 115 | 382 | 115 | 531 | 115 | 384 |
| 2.0 | 119 | 256 | 119 | 390 | 119 | 539 | 119 | 392 |
| 2.1 | 123 | 263 | 123 | 398 | 123 | 547 | 123 | 400 |
| 2.2 | 127 | 269 | 127 | 406 | 127 | 556 | 127 | 408 |
| 2.3 | 131 | 276 | 131 | 415 | 131 | 564 | 131 | 417 |
| 2.4 | 135 | 282 | 135 | 423 | 135 | 572 | 135 | 425 |
| 2.5 | 139 | 289 | 139 | 431 | 139 | 580 | 139 | 433 |
| 2.6 | 143 | 295 | 143 | 439 | 143 | 588 | 143 | 441 |
| 2.7 | 147 | 302 | 147 | 447 | 147 | 597 | 147 | 449 |
| 2.8 | 151 | 308 | 151 | 455 | 151 | 605 | 151 | 457 |
| 2.9 | 155 | 315 | 155 | 463 | 155 | 613 | 155 | 465 |
| 3.0 | 158 | 321 | 158 | 471 | 158 | 621 | 158 | 473 |
| 3.1 | 162 | 328 | 162 | 479 | 162 | 629 | 162 | 481 |
| 3.2 | 166 | 334 | 166 | 487 | 166 | 638 | 166 | 489 |
| 3.3 | 170 | 341 | 170 | 496 | 170 | 646 | 170 | 498 |
| 3.4 | 174 | 347 | 174 | 504 | 174 | 654 | 174 | 506 |
| 3.5 | 178 | 354 | 178 | 512 | 178 | 662 | 178 | 514 |
| 3.6 | 182 | 360 | 182 | 520 | 182 | 670 | 182 | 522 |
| 3.7 | 186 | 367 | 186 | 528 | 186 | 679 | 186 | 530 |
| 3.8 | 190 | 373 | 190 | 536 | 190 | 687 | 190 | 538 |
| 3.9 | 194 | 380 | 194 | 544 | 194 | 695 | 194 | 546 |
| 4.0 | 198 | 386 | 198 | 552 | 198 | 703 | 198 | 554 |
| 4.1 | 202 | 393 | 202 | 560 | 202 | 711 | 202 | 562 |
| 4.2 | 206 | 399 | 206 | 568 | 206 | 720 | 206 | 570 |
| 4.3 | 210 | 406 | 210 | 577 | 210 | 728 | 210 | 579 |
| 4.4 | 214 | 412 | 214 | 585 | 214 | 736 | 214 | 587 |
| 4.5 | 218 | 419 | 218 | 593 | 218 | 744 | 218 | 595 |
| 4.6 | 222 | 425 | 222 | 601 | 222 | 752 | 222 | 603 |
| 4.7 | 225 | 432 | 225 | 609 | 225 | 761 | 225 | 611 |
| 4.8 | 229 | 438 | 229 | 617 | 229 | 769 | 229 | 619 |
| 4.9 | 233 | 445 | 233 | 625 | 233 | 777 | 233 | 627 |
| 5.0 | 237 | 451 | 237 | 633 | 237 | 785 | 237 | 635 |

TEST CIRCUITS

CIRCUIT①



CIRCUIT②



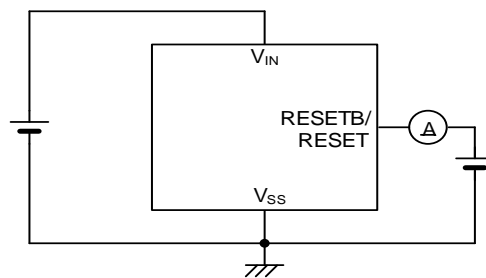
CIRCUIT③



CIRCUIT④



CIRCUIT⑤



**RESETB" is A/B type, and "RESET" is C/D type.

OPERATIONAL DESCRIPTION



Fig. 1: Typical block diagram (CMOS output/Active Low product)

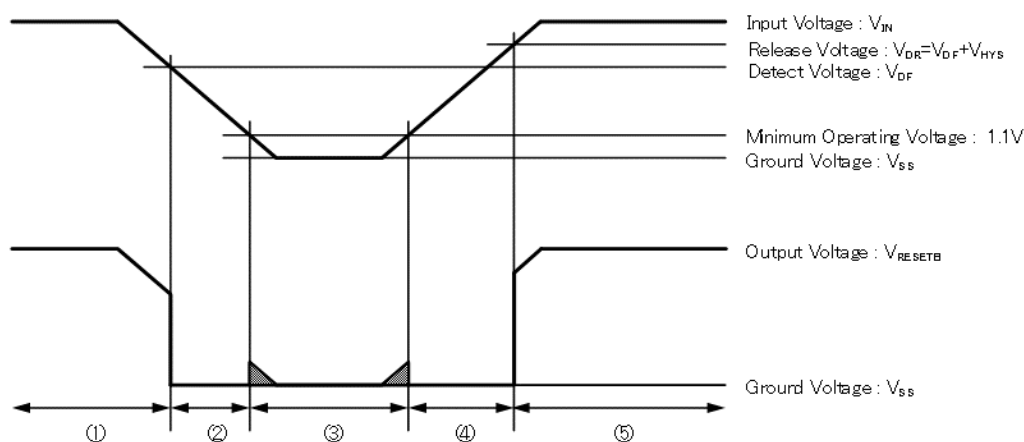


Fig. 2: Timing chart of Fig. 1

The circuit operation in the above representative circuit example will be explained using the timing chart.

- (1) Assume that the input voltage (V_{IN}) in the initial state is higher than the release voltage (V_{DR}), and V_{IN} gradually decreases. In a state where a voltage higher than the detection voltage (V_{DF}) is applied to the input voltage (V_{IN}), the input voltage (V_{IN}) is output to the RESETB pin (released state).
 - * In the case of N-ch open drain output products, the RESETB pin goes into a high impedance state. When the output is pulled up, the pull-up voltage is output to the RESETB pin.
- (2) When the input voltage (V_{IN}) drops below the detection voltage (V_{DF}), the ground potential (V_{SS}) is output to the RESETB pin (detection state).
 - * N-ch open drain output products are also the same.
- (3) If the input voltage (V_{IN}) further decreases and becomes lower than the minimum operating voltage (1.1V), the output becomes undefined. However, the XC6136C series (CMOS output product) has an under-voltage lockout (UVLO) circuit to prevent undefined operation due to a decrease in V_{IN} . Therefore, the floating of the RESETB terminal caused by less than the minimum operating voltage is minimized.
 - * Pull-up voltage may be output to the RESETB terminal when the output terminal is pulled up with an N-ch open drain output product.
- (4) The RESETB pin holds the ground potential (V_{SS}) until the input voltage (V_{IN}) rises above the minimum operating voltage (1.1V) and reaches the release voltage (V_{DR}).
- (5) When the input voltage (V_{IN}) becomes equal to or higher than the release voltage (V_{DR}), the input voltage (V_{IN}) is output to the RESETB pin.
 - * In the case of N-ch open drain output products, the RESETB pin goes into a high-impedance state in the same way as in 1), and if the output is pulled up, the pull-up voltage is output to the RESETB pin.
- (6) The difference between the release voltage (V_{DR}) and the detect voltage (V_{DF}) is the hysteresis width (V_{HYS}).
 - Note: In the above explanation, the operation time of the circuit is omitted for simplicity of explanation. In addition, above explanation is the operation using Active Low product. For Active High products, please reverse the output logic of RESETB pin voltage.

NOTES ON USE

- (1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
- (2) The power input pin voltage may fall due to the flow through current during IC operation and the resistance component between the power supply and the power input pin.
In the case of CMOS output, a drop in the power input pin voltage may occur in the same way due to the output current. When this happens, if the power input pin voltage drops below the minimum operating voltage, a malfunction may occur.
- (3) Note that large, sharp changes of the power input pin voltage may lead to malfunction.
- (4) Since the power supply noise may cause malfunction, please fully evaluate with an actual system. As necessary, please take measures such as inserting a capacitor between V_{IN} and V_{SS} .
- (5) When an N-ch open drain output is used, the V_{RESETB} voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.

At detection:

$$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{ON})$$

V_{pull} : Voltage after pull-up

$R_{ON}^{(*)}$: ON resistance of N-ch driver M1 (calculated from V_{RESETB}/I_{RBOUN} based on electrical characteristics)

Example: When $V_{IN}=2.0V^{(2)}$, $R_{ON} = 0.3V / (4.1 \times 10^{-3} A) \cong 73.2\Omega$ (MAX.)

If it is desired to make V_{RESETB} at detection 0.1V or less when V_{pull} is 3.0V,

$$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{ON} = \{ (3V / 0.1V) - 1 \} \times 73.2\Omega \cong 2.1k\Omega$$

Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.1k Ω or higher.

^(*) Note that R_{ON} becomes larger as V_{IN} becomes smaller.

⁽²⁾ For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

At release:

$$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{off})$$

V_{pull} : Voltage after pull-up

R_{off} : Resistance when N-ch driver M1 is OFF (calculated from V_{RESETB}/I_{LEAKN} based on electrical characteristics)

Example: When V_{pull} is 6.0V, $R_{off} = 6V / (0.1 \times 10^{-6} A) = 60M\Omega$ (MIN.).

If it is desired to make V_{RESETB} 5.99V or higher,

$$R_{pull} = \{ (V_{pull} / V_{RESETB}) - 1 \} \times R_{off} = \{ (6V / 5.99V) - 1 \} \times 60 \times 10^6\Omega \cong 100k\Omega$$

Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100k Ω or less.

The above V_{RESETB} voltage is an example calculation of Active Low products.

To calculate the V_{RESET} voltage (Active High product), calculate by inverting the logic at detection and release.

- (6) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(1) Detect, Release Voltage vs. Ambient Temperature



(2) Output Voltage vs. Input Voltage



(3) Hysteresis Width vs. Ambient Temperature



(4) Supply Current vs. Ambient Temperature



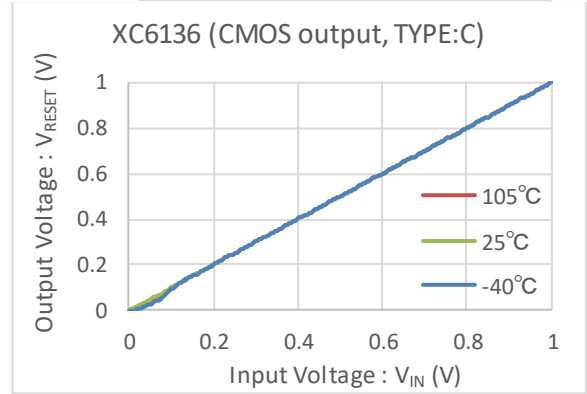
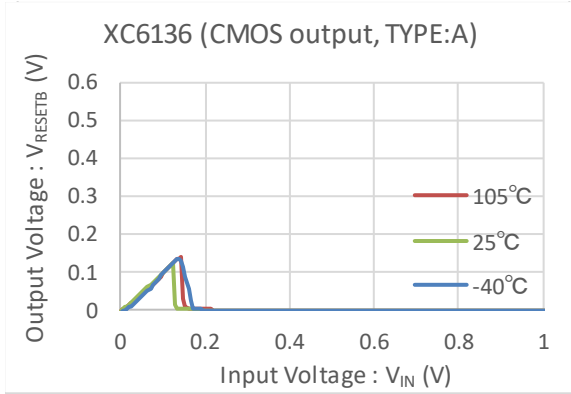
(5) Supply Current vs. Input Voltage



XC6136 Series

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

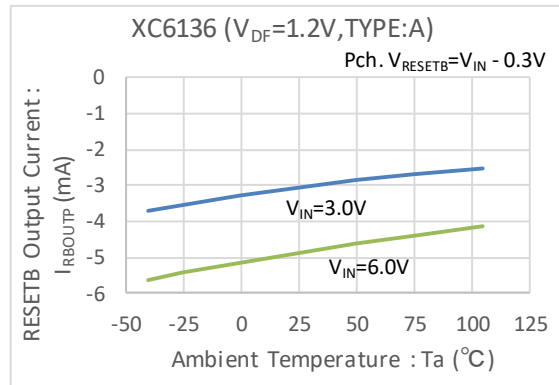
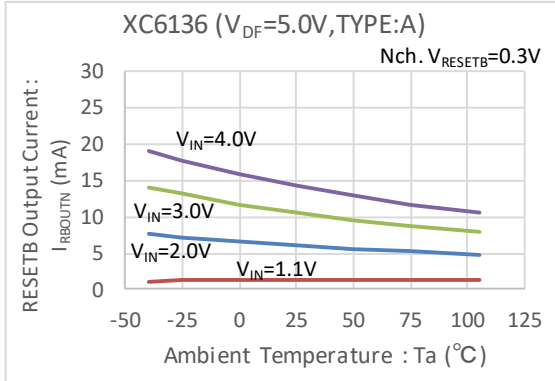
(6) Output Voltage vs. Input Voltage ($V_{IN} < \text{Operating Voltage}$)



(7) Release, Detect Delay Time vs. Ambient Temperature



(8) RESETB Output Current vs. Ambient Temperature



(9) RESETB Output Leakage Current vs. Ambient Temperature



■ PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

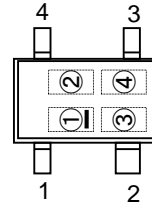
| PACKAGE | OUTLIN / LAND PATTERN | THERMAL CHARACTERISTICS | |
|-----------|-------------------------------|-------------------------|---|
| SSOT-24 | SSOT-24 PKG | Standard Board | SSOT-24 Power Dissipation |
| | | JESD51-7 Board | |
| SOT-25 | SOT-25 PKG | Standard Board | SOT-25 Power Dissipation |
| | | JESD51-7 Board | |
| USPQ-4B05 | USPQ-4B05 PKG | Standard Board | USPQ-4B05 Power Dissipation |

MARKING RULE

USPQ-4B05 (with underline mark ①)



SSOT-24 (with underline mark) ①



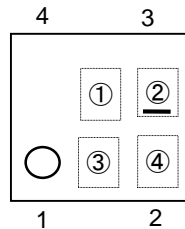
USPQ-4B05 (with overline mark) ①



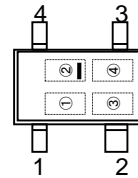
SSOT-24 (with overline mark) ①



USPQ-4B05 (with underline mark ②)



SSOT-24 (with underline mark ②)



① represents products series

| MARK | Registration order | PRODUCT SERIES |
|---------------------------|--------------------|----------------|
| <u>X</u> (with underline) | 1 | XC6136*****-G |
| <u>1</u> (with overline) | 2 | |
| <u>3</u> (with overline) | 3 | |
| <u>5</u> (with overline) | 4 | |
| <u>A</u> | 5 | |
| <u>B</u> | 6 | |
| <u>C</u> | 7 | |

*Mark ① is a common symbol and Mark ② is assigned a sequential number.
(The sequential numbers of Mark ② are numbered stating from "0".)

② represents internal sequential number

| MARK① | MARK ①Line | MARK ②Line |
|----------|----------------|----------------|
| <u>X</u> | with underline | - |
| <u>1</u> | with overline | - |
| <u>3</u> | with overline | - |
| <u>5</u> | with overline | - |
| A | - | with underline |
| B | - | with underline |
| C | - | with underline |

sequential number 0~9, A~Z repeated.(G, I, J, O, Q, W excluded)

③,④ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~A9, AA~Z9 repeated.

(G, I, J, O, Q, W excluded)

MARKING RULE

SOT-25 (under dot)



① represents products series

| MARK | PRODUCT SERIES |
|------|----------------|
| X | XC6136*****-G |

※Mark ① gets a serial number with a common symbol.

※Under dot

②③ represents internal sequential number

01~09, 10~99, A0~A9, B0~B9...Z0~Z9, AA~AZ, BA~BZ...ZA~ZZ repeated.

(G, I, J, O, Q, W excluded)

④⑤ represents production lot number

01~09, 0A~0Z, 11...9Z, A1~A9, AA...Z9, ZA~ZZ repeated

(G, I, J, O, Q, W excluded)

* No character inversion used.