

# XC6705 Series

ETR03127-001a

20V input voltage, 200mA low supply current 1.2  $\mu$ A, high speed voltage regulator

☆Green Operation compatible

## GENERAL DESCRIPTION

The XC6705 series is a high-speed LDO regulator IC using CMOS process. This series are low supply current 1.2 $\mu$ A, despite achieves high accuracy, and high ripple rejection.

Internal circuitry includes a reference voltage supply, error amplifier, Pch driver FET, current limit circuit, thermal shutdown circuit, and phase compensation circuit.

The output voltage is fixed internally by laser trimming, and product selections from 2.5V to 5.5V (0.1V increments) are available.

In addition, the A type is built-in with  $C_L$  discharge function that can return the charged in the output stabilization capacitor ( $C_L$ ) to the high-speed  $V_{SS}$  level in the stand-by mode.

The XC6705 series is built-in with soft start function to suppress inrush current and overshoot at startup. The series start up the output voltage in 1.0ms.

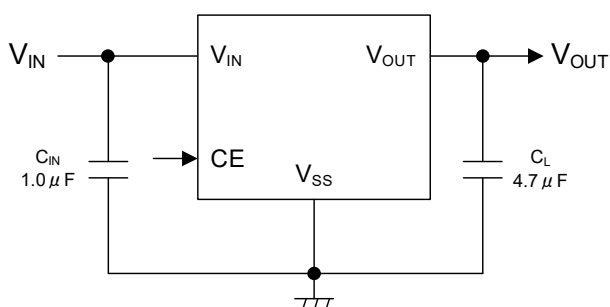
## APPLICATION

- Industrial equipment
  - Smart meters, gas detectors, smoke detectors
  - Sensor / IoT devices
  - FA devices
- Domestic electrical appliances
- Consumer equipments
- Energy harvest
- Others
  - Devices with 2~4 Li-ion rechargeable battery directly connection
  - Devices with 2 Li-ion battery directly connection / 4 or more dry batteries

## FEATURE

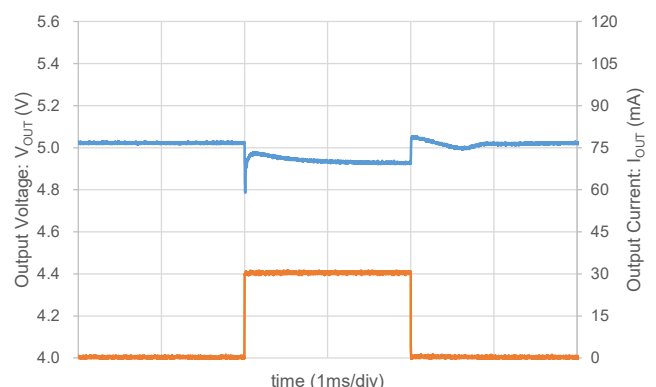
Low Supply Current	:	1.2 $\mu$ A
Operating Voltage Range	:	3.5V ~ 20.0V
Output Voltage Range	:	2.5V ~ 5.5V (0.1V increments)
Accuracy	:	$\pm$ 1.5%
Maximum Output Current	:	200mA
Stand-by Current	:	0.15 $\mu$ A
High Ripple Rejection	:	50dB @ 1kHz
Function	:	CE Seamless GO Soft-Start $C_L$ Discharge (A TYPE)
Protection Function	:	Current Limit Thermal Shutdown
Input / output Capacitor	:	Ceramic capacitor
Package	:	SOT-25 (2.8 x 2.9 x 1.3mm) USP-4 (1.2 x 1.6 x 0.6mm)
Operating Ambient Temperature	:	-40 $^{\circ}$ C ~ 105 $^{\circ}$ C
Environmentally Friendly	:	EU RoHS Compliant, Pd Free

## TYPICAL APPLICATION CIRCUIT



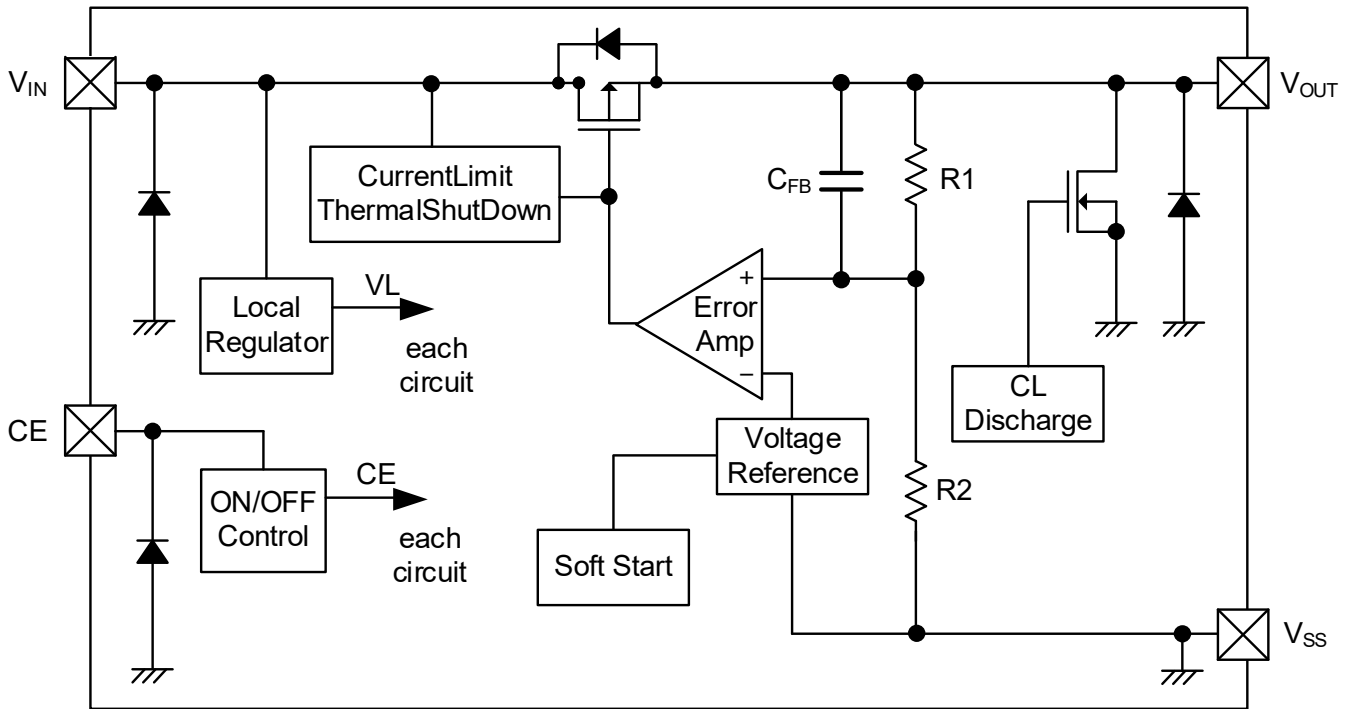
## TYPICAL PERFORMANCE CHARACTERISTICS

XC6705x501 ( $V_{OUT}=5.0V$ )  
 $V_{IN}=7.0V$ ,  $t_r=1\mu s$ ,  $T_a=25^{\circ}C$   
 $C_{IN}=1.0\mu F$  (GRM155C71A105ME11#)  
 $C_L=1.0\mu F$  (GRM219R7YA105MA12#)



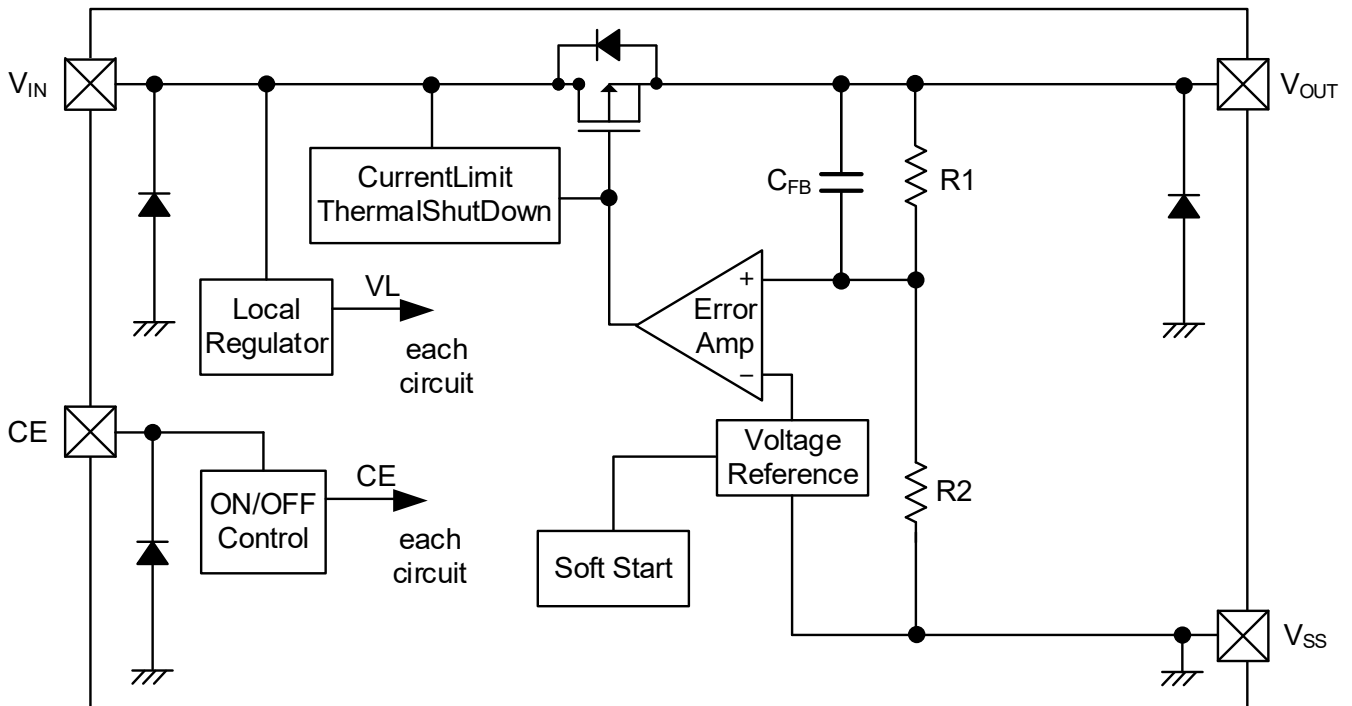
## ■ BLOCK DIAGRAMS

### 1) A TYPE



Diodes inside the circuits are ESD protection diodes and parasitic diodes.

### 2) B TYPE



Diodes inside the circuits are ESD protection diodes and parasitic diodes.

## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

XC6705①②③④⑤⑥-⑦<sup>(\*)</sup>

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Refer to Selection Guide
		B	
②③	Output Voltage	25 ~ 55	Output Voltage {x.xV} e.g. 2.8V ②=2, ③=8 (0.1V increments)
④	Fixed No.	1	-
⑤⑥-⑦	Packages (Order Unit)	GR-G <sup>(*)</sup>	USP-4 (3,000pcs/Reel)
		MR-G <sup>(*)</sup>	SOT-25 (3,000pcs/Reel) <sup>(*)</sup>

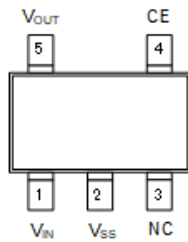
<sup>(\*)</sup> SOT-25 uses Cu bonding wires.

<sup>(\*)</sup> "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

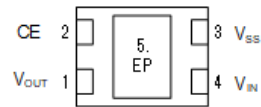
### ● Selection Guide

TYPE	CE function	CL Auto-Discharge	Soft-Start
A	Yes	Yes	Yes
B	Yes	No	Yes

## ■ PIN CONFIGURATION



SOT-25  
(TOP VIEW)



USP-4  
(BOTTOM VIEW)

## ■ PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-4		
1	4	$V_{IN}$	Power Input
2	3	$V_{SS}$	Ground
5	1	$V_{OUT}$	Output
4	2	CE	ON/OFF Control
3	-	NC	No Connection
-	5	EP	Exposed thermal pad. The Exposed pad must be connected to $V_{SS}$ (Pin3).

## ■ FUNCTION CHART

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active
	OPEN	Undefined state <sup>(*)</sup>

<sup>(\*)</sup> Please do not leave the CE pin open. Each should have a certain voltage.

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V <sub>IN</sub> Pin Voltage		V <sub>IN</sub>	-0.3 ~ 24.0	V
V <sub>OUT</sub> Pin Voltage		V <sub>OUT</sub>	-0.3 ~ V <sub>IN</sub> + 0.3 or 6.5 <sup>(*)1</sup>	V
CE Pin Voltage		V <sub>CE</sub>	-0.3 ~ 24.0	V
Power Dissipation (Ta=25°C)	SOT-25	Pd	760 (JESD51-7 board) <sup>(*)2</sup>	mW
	USP-4		1000 (40mm x 40mm board) <sup>(*)2</sup>	
Junction Temperature		T <sub>j</sub>	-40 ~ 125	°C
Storage Temperature		T <sub>stg</sub>	-55 ~ 125	°C

All voltages are described based on the V<sub>SS</sub>.

<sup>(\*)1</sup> The maximum rating corresponds to the lowest value between V<sub>IN</sub>+0.3V or 6.5V.

<sup>(\*)2</sup> The power dissipation figure shown is PCB mounted and is for reference only.

Please refer to PACKAGING INFORMATION for the mounting condition.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS
V <sub>IN</sub> Pin Voltage		V <sub>IN</sub>	3.5	-	20.0	V
Output Current <sup>(*)2</sup>		I <sub>OUT</sub>	0	-	200	mA
CE Pin Voltage		V <sub>CE</sub>	0.0	-	20.0	V
Operating Ambient Temperature		T <sub>opr</sub>	-40	-	105	°C
Input Capacitor (Effective Value)		C <sub>IN</sub> <sup>(*)3,4)</sup>	0.4	1.0	Any	μF
Output Capacitor (Effective Value)	V <sub>OUT(T)</sub> <sup>(*)1</sup> ≤ 2.9V	C <sub>L</sub> <sup>(*)3)</sup>	0.4	2.2	220	μF
	2.9V < V <sub>OUT(T)</sub>		0.4	1.0	220	

All voltages are described based on the V<sub>SS</sub>.

<sup>(\*)1</sup> V<sub>OUT(T)</sub> : Nominal output voltage.

<sup>(\*)2</sup> Use within a range where the junction temperature does not exceed the maximum junction temperature.

<sup>(\*)3</sup> Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

<sup>(\*)4</sup> If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

## ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Input Voltage	V <sub>IN</sub>		3.5	-	20.0	V	①
Output Voltage	V <sub>OUT(E)</sub> <sup>(*)1</sup>	I <sub>OUT</sub> =10mA	V <sub>OUT(T)</sub> ×0.985	V <sub>OUT(T)</sub>	V <sub>OUT(T)</sub> ×1.015	V	①
Maximum Output Current	I <sub>OUTMAX</sub>		200	-	-	mA	①
Load Regulation	ΔV <sub>OUT</sub>	V <sub>OUT@10mA</sub> - V <sub>OUT@100mA</sub>	0	V <sub>OUT(T)</sub> ×0.007	V <sub>OUT(T)</sub> ×0.027	V	①
Load Regulation2	ΔV <sub>OUT2</sub>	V <sub>OUT@0.01mA</sub> - V <sub>OUT@10mA</sub>	0	V <sub>OUT(T)</sub> ×0.028	V <sub>OUT(T)</sub> ×0.05		
Dropout Voltage	V <sub>dif</sub> <sup>(*)3</sup>	I <sub>OUT</sub> = 100mA	-	E-1		V	①
Quiescent Current	I <sub>SS</sub>	V <sub>CE</sub> =V <sub>IN</sub> , I <sub>OUT</sub> =0mA	-	1.2	3.0	μA	②
Stand-by Current	I <sub>STB</sub>	V <sub>IN</sub> =8.0V, V <sub>CE</sub> =V <sub>SS</sub>	-	0.15	0.30	μA	②
Line Regulation	ΔV <sub>OUT</sub> / (ΔV <sub>IN</sub> ·V <sub>OUT</sub> )	V <sub>OUT(T)</sub> +2V ≤ V <sub>IN</sub> ≤ 20V, I <sub>OUT</sub> =10mA	-	0.02	0.10	%/V	①
Output Voltage Temperature Characteristics	ΔV <sub>OUT</sub> / (ΔT <sub>opr</sub> · V <sub>OUT</sub> )	T <sub>oprMIN</sub> ≤ T <sub>opr</sub> ≤ T <sub>oprMAX</sub>	-	±100	-	ppm/°C	①
Ripple Rejection	PSRR	V <sub>IN</sub> = {V <sub>OUT(T)</sub> +2.0V} + 0.5V <sub>P-PAC</sub> V <sub>CE</sub> =V <sub>IN</sub> , I <sub>OUT</sub> =30mA, f=1kHz	-	50	-	dB	④
Current Limit	I <sub>LIM</sub>	V <sub>IN</sub> =V <sub>OUT(T)</sub> +3.0V, V <sub>CE</sub> =V <sub>IN</sub> , V <sub>OUT</sub> = V <sub>OUT(T)</sub> ×0.95	220	300	-	mA	①
Short-Circuit Current	I <sub>SHORT</sub>	V <sub>OUT</sub> =V <sub>SS</sub>	-	30	-	mA	①
Soft-Start Time-	t <sub>SS</sub>	V <sub>IN</sub> = 8.5V, V <sub>CE</sub> = 0V→8.5V After "H" is fed to CE, the time by when V <sub>OUT</sub> rises to V <sub>OUT(T)</sub> × 0.9	0.65	1.00	1.70	ms	①
CE "H" Level Voltage	V <sub>CEH</sub>	Ta=25°C T <sub>oprMIN</sub> ≤ T <sub>opr</sub> ≤ T <sub>oprMAX</sub> <sup>(*)4</sup>	1.4	-	20.0	V	③
CE "L" Level Voltage	V <sub>CEL</sub>	Ta=25°C T <sub>oprMIN</sub> ≤ T <sub>opr</sub> ≤ T <sub>oprMAX</sub> <sup>(*)4</sup>	V <sub>SS</sub>	-	0.25	V	③
CE "H" Level Current	I <sub>CEH</sub>	V <sub>CE</sub> =V <sub>IN</sub>	-	0.05	0.3	μA	③
CE "L" Level Current	I <sub>CEL</sub>	V <sub>CE</sub> =V <sub>SS</sub>	-0.1	0.0	0.1	μA	③
Thermal Shutdown Detect Temperature	T <sub>TSD</sub>	Junction Temperature I <sub>OUT</sub> =10mA	-	165	-	°C	①
Thermal Shutdown Release Temperature	T <sub>TSR</sub>	Junction Temperature	-	140	-	°C	①
CL Auto-Discharge Resistance (A TYPE)	R <sub>DCHG</sub>	V <sub>IN</sub> =8.0V, V <sub>OUT</sub> =1.0V, V <sub>CE</sub> =V <sub>SS</sub>	125	250	547	Ω	①

Unless otherwise stated regarding input voltage conditions, V<sub>IN</sub> = V<sub>OUT(T)</sub>+2.0V, V<sub>CE</sub> = V<sub>IN</sub>

(\*)1 V<sub>OUT(E)</sub> : Effective output voltage

(\*)2 V<sub>OUT(T)</sub> : Nominal output voltage

(\*)3 V<sub>dif</sub> = { V<sub>IN1</sub> - V<sub>OUT1</sub> }

V<sub>IN1</sub> : The input voltage when V<sub>OUT1</sub> appears as input voltage is gradually decreased.

V<sub>OUT1</sub> : A voltage equal to 98% of the output voltage whenever an amply stabilized V<sub>IN</sub> and I<sub>OUT</sub>=10mA is input.

(\*)4 Design value

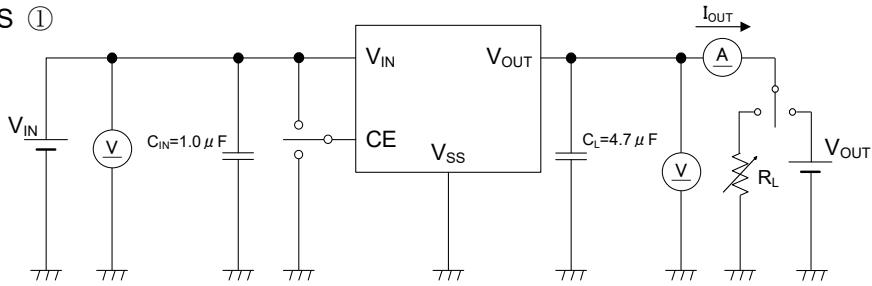
**■ ELECTRICAL CHARACTERISTICS (Continued)**

●SPEC Table

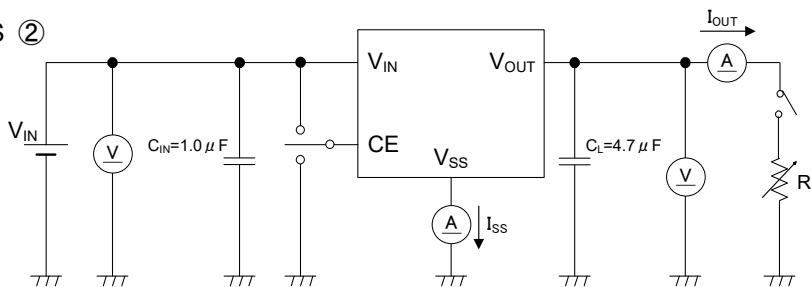
SYMBOL	E-1	
NOMINAL OUTPUT VOLTAGE (V)	Dropout Voltage Vdif (V) I <sub>OUT</sub> =100mA	
V <sub>OUT(T)</sub>	TYP.	MAX
2.5	0.53	0.81
2.6	0.52	
2.7	0.51	
2.8	0.50	
2.9	0.50	
3.0	0.49	
3.1	0.48	
3.2	0.48	
3.3	0.47	0.69
3.4	0.47	
3.5	0.47	
3.6	0.46	
3.7	0.46	
3.8	0.46	
3.9	0.46	
4.0	0.45	
4.1	0.45	0.66
4.2	0.45	
4.3	0.45	
4.4	0.44	
4.5	0.44	
4.6	0.44	
4.7	0.43	
4.8	0.43	
4.9	0.43	
5.0	0.43	
5.1	0.42	
5.2	0.42	
5.3	0.42	
5.4	0.41	
5.5	0.41	

## TEST CIRCUITS

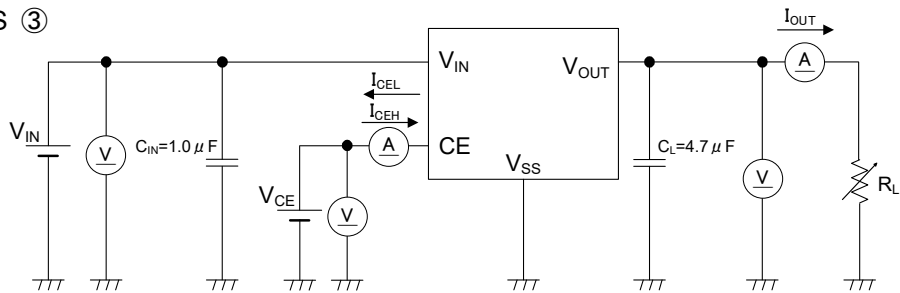
TEST CIRCUITS ①



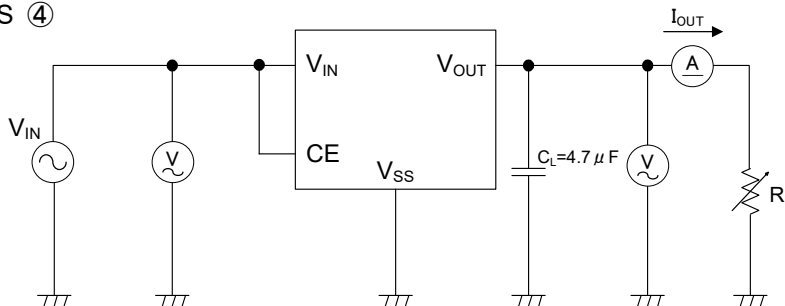
TEST CIRCUITS ②



TEST CIRCUITS ③

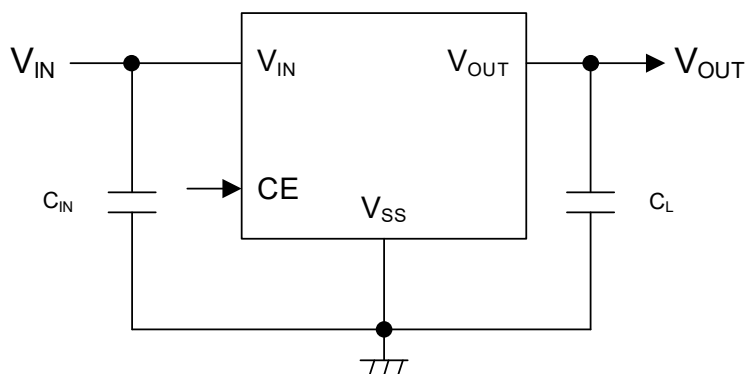


TEST CIRCUITS ④





## ■ TYPICAL APPLICATION CIRCUIT



### 【Typical Examples】

	CONDITION	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE (L × W × T)
$C_{IN}^{(*1,2)}$	-	Murata	GRM219R7YA105MA12	1.0 $\mu$ F / 35V	2.0 × 1.25 × 0.85(mm)
$C_L^{(*1)}$	$V_{OUT(T)} \leq 2.9V$	Murata	GRM155C71A225ME11	2.2 $\mu$ F / 10V	1.0 × 0.5 × 0.5(mm)
	$2.9V < V_{OUT(T)}$	Murata	GRM155C71A105ME11	1.0 $\mu$ F / 10V	1.0 × 0.5 × 0.5(mm)

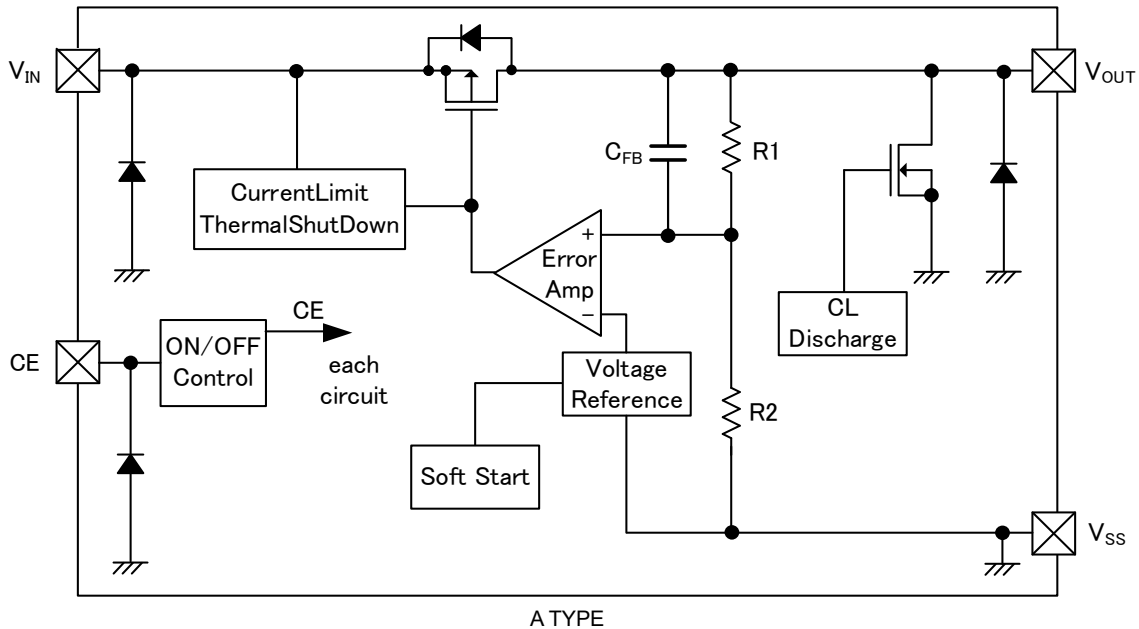
(\*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(\*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

## OPERATIONAL EXPLANATION

The voltage divided by resistors R1 & R2 is compared with the internal voltage reference by the error amplifier. The P-channel MOSFET, which is connected to the  $V_{IN}$  pin, is then driven by the subsequent output signal. The output voltage is controlled and stabilized by a system of negative feedback.

In addition, in order to improving the responsiveness of the error amplifier according to the output current, both low current consumption at light load and high-speed response at heavy load are achieved.



### <Low ESR capacitor support>

An internal phase compensation circuit is incorporated in the XC6705 series to enable a stable output voltage to be obtained even when a low ESR capacitor is used. To stabilize the effect of the phase compensation circuit, always connect the output capacitor ( $C_L$ ) in direct proximity to the  $V_{OUT}$  pin and  $V_{SS}$  pin. In addition, to stabilize the input power, connect the input capacitor ( $C_{IN}$ ) in direct proximity to the  $V_{IN}$  pin and  $V_{SS}$  pin.

## ■ OPERATIONAL EXPLANATION(Continued)

### <CE function>

When "H" voltage  $V_{CEH}$  is input to the CE pin, the output voltage is raised by the soft start function, and then normal operation is performed.

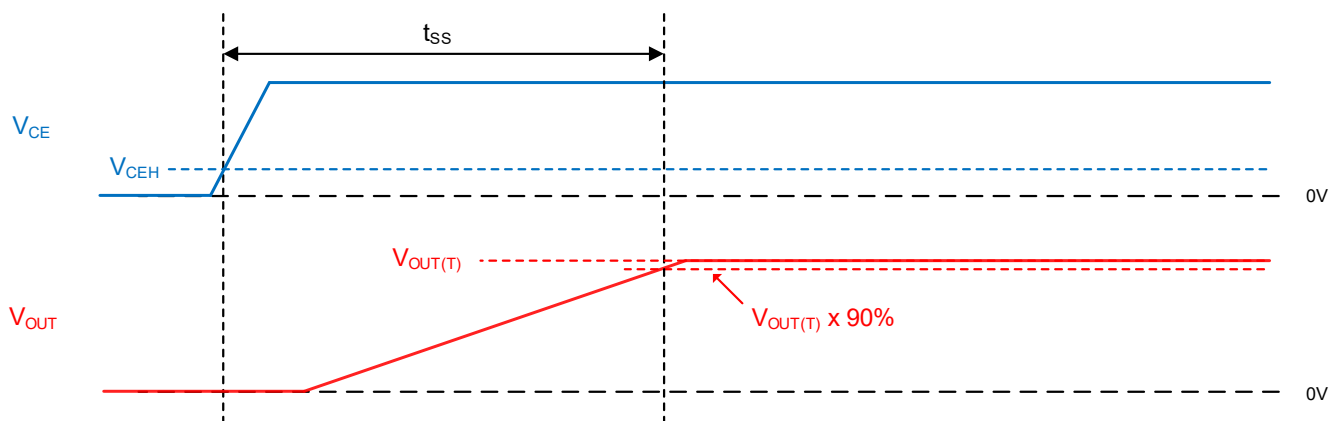
When "L" voltage  $V_{CEL}$  is input to the CE pin, the standby mode is set, the current consumption is suppressed to the standby current  $I_{STB}$  (TYP.  $0.15\mu A$ ), and the Pch driver MOSFET is turned off.

The output voltage becomes unstable when the CE pin is open. Please input a certain voltage within an electrical characteristic into CE pin.

### <Startup operation : soft start>

This is a function to gently raise the output voltage and suppress the inrush current.

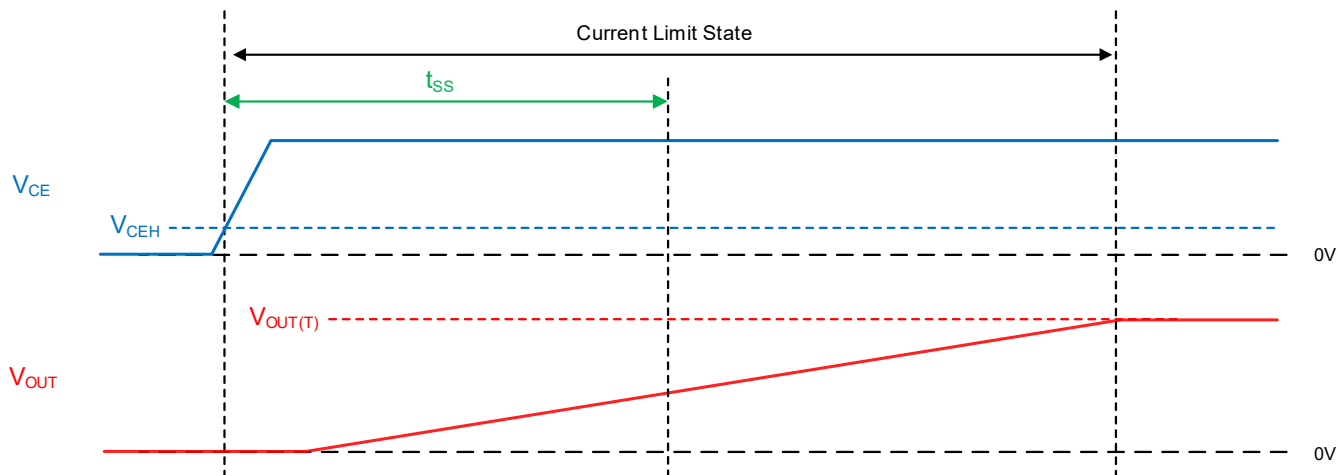
After inputting the "H" voltage ( $V_{CEH}$ ) to the CE pin, the reference voltage connected to the error amplifier is configured to linearly increase to the soft start period  $t_{SS}$  (TYP.  $1.0ms$ ). As a result, the output voltage rises in proportion to the increase in the reference voltage. This operation prevents the input current inrush and allows the output voltage to rise smoothly.



### Output capacitor using at the large-capacity or heavy load

If a large-capacity output capacitor is used or a heavy load is applied during startup, the output voltage may not rise to the set output voltage during the soft start period.

If the output voltage does not rise to the set output voltage during the soft start period, the current limit function is activated to raise the output voltage.



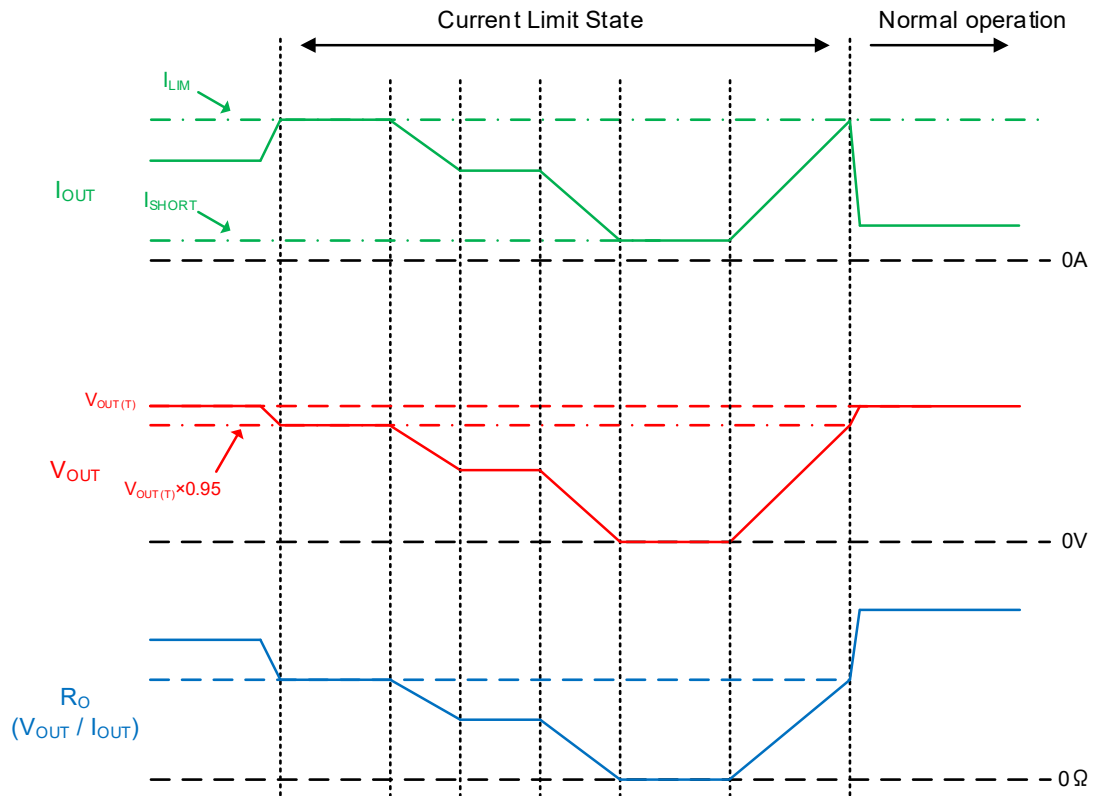
## OPERATIONAL EXPLANATION(Continued)

### <Current Limit>

The XC6705 series uses a current fold-back circuit as a current limit.

When the output current reaches  $I_{LIM}$ (TYP. 300mA), the current fold-back circuit operates. As a result, the output current also drops as the output voltage drops.

When the output voltage drops and the  $V_{OUT}$  pin is short-circuited, the output current is  $I_{SHORT}$ (TYP. 30mA).



### <thermal shutdown circuit>

The XC6705 series incorporates a thermal shutdown circuit for overheating protection.

When the junction temperature reaches the detection temperature  $T_{TSD}$ (TYP. 165°C), the Pch driver FET is forcibly turned off. The thermal shutdown function operates and the Pch driver FET continues to be off. When the junction temperature falls to the release temperature (TYP. 140°C), the thermal shutdown function is canceled.

When the thermal shutdown function is canceled, the soft start function works to raise the output voltage.

If the output current is less than 10mA, in order to reduce the current consumption during light roads, reduce the supply current to the thermal shutdown circuit. If the output current is less than 10mA due to this operation, the thermal shutdown function will stop operating.

## ■ OPERATIONAL EXPLANATION(Continued)

<C<sub>L</sub> discharge>

The A type quickly discharges the charge of the output capacitor by Nch FET to prevent the application from malfunctioning due to the charge remaining in the output capacitor during standby.

An Nch FET is connected between the V<sub>OUT</sub> pin and the V<sub>SS</sub> pin, and the Nch FET quickly discharge the charge in C<sub>L</sub> by turning on the Nch FET in the standby mode.

The discharge time and output voltage at this time depend on the input voltage, discharge resistance R<sub>DCHG</sub> and output capacitor.

## ■ NOTES ON USE

1) For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

Also, if IC is used under the conditions out of the recommended operating range, the IC may not operate normally or may cause deterioration.

2) The current limit function is operating even the output is started. If the IC is started with a current load that exceeds the fold-back curve, a start failure may occur due to the current limiting characteristics. In this case, after the output voltage rises to near the set output voltage, please control the sequence so that the load current is pulled.

3) Note on board layout

1. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please strengthen  $V_{IN}$  and  $V_{SS}$  wiring in particular.

2. The input capacitor ( $C_{IN}$ ) and the output capacitor ( $C_L$ ) should be placed to the IC as close as possible.

4) The output voltage may become unstable near the maximum junction temperature.

5) Torex places an importance on improving our products and its reliability. However, by any possibility, we would request user all-safe design and post-aging treatment on system or equipment.

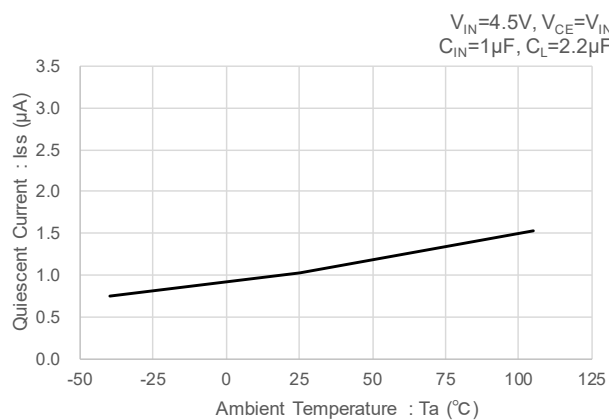
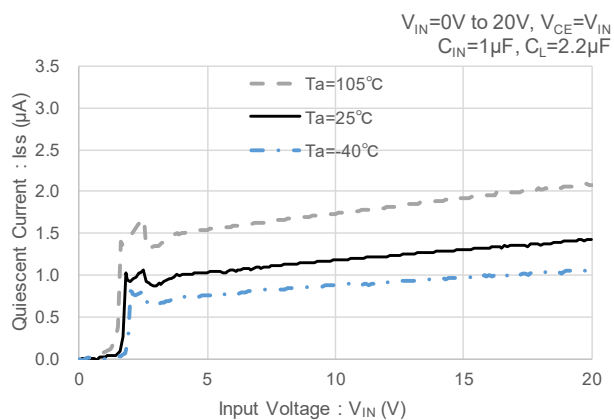
## TYPICAL PERFORMANCE CHARACTERISTICS

(1) Quiescent Current vs. Input Voltage

(2) Quiescent Current vs. Ambient Temperature

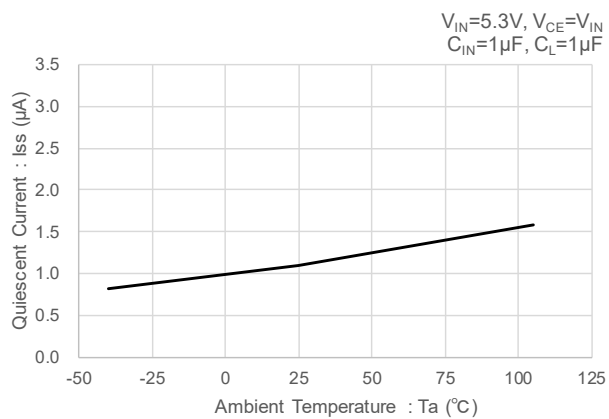
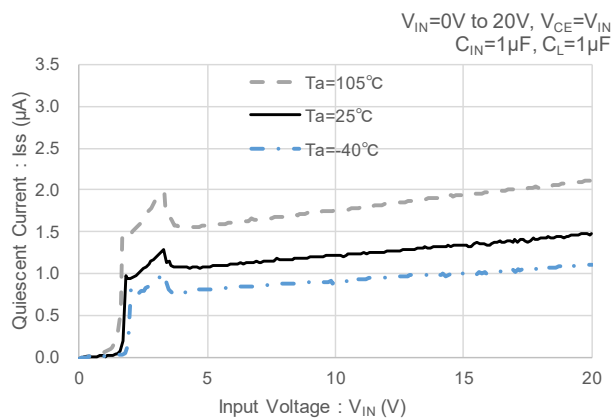
(1-1)  $V_{OUT(T)}=2.5V$

(2-1)  $V_{OUT(T)}=2.5V$



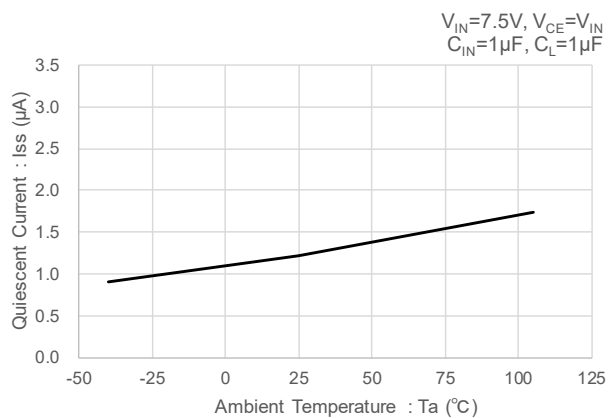
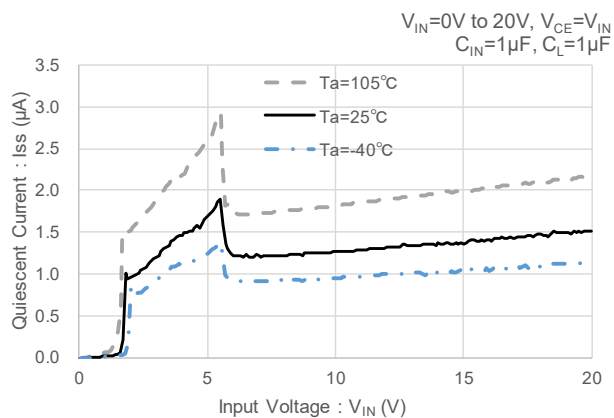
(1-2)  $V_{OUT(T)}=3.3V$

(2-2)  $V_{OUT(T)}=3.3V$



(1-3)  $V_{OUT(T)}=5.5V$

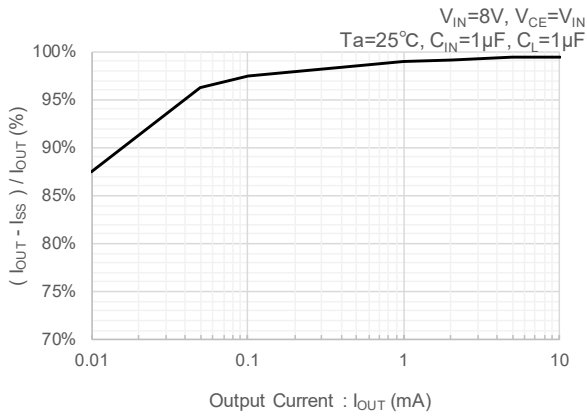
(2-3)  $V_{OUT(T)}=5.5V$



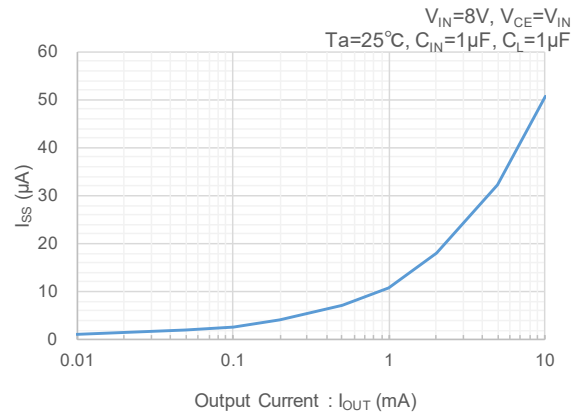
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (3) Quiescent Current vs. Output Current

(3-1)  $(I_{OUT} - I_{SS}) / I_{OUT}$  vs. Output Current ( $V_{OUT(T)}=2.5V$ )

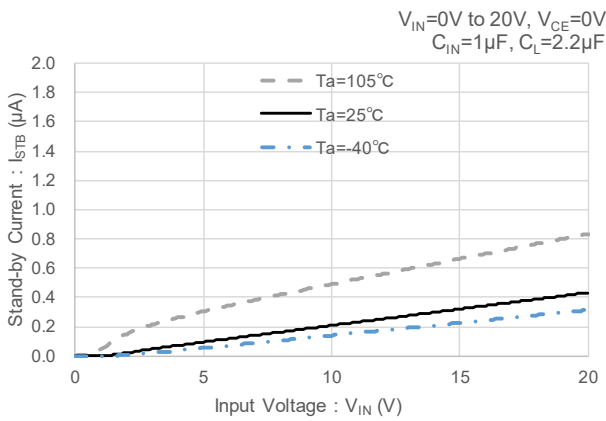


(3-2) Quiescent Current vs. Output Current ( $V_{OUT(T)}=2.5V$ )



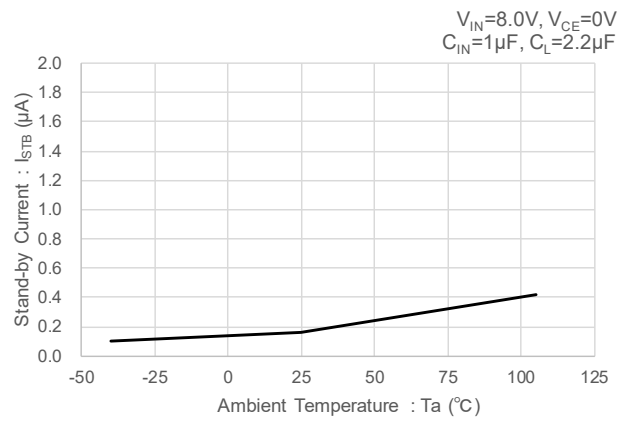
### (4) Stand-by Current vs. Input Voltage

(4-1)  $V_{OUT(T)}=2.5V$



### (5) Stand-by Current vs. Ambient Temperature

(5-1)  $V_{OUT(T)}=2.5V$





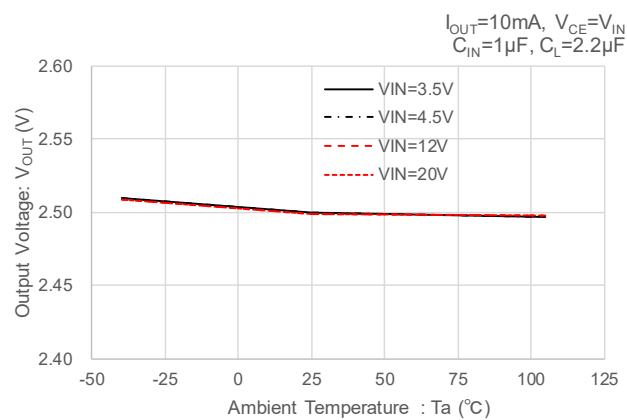
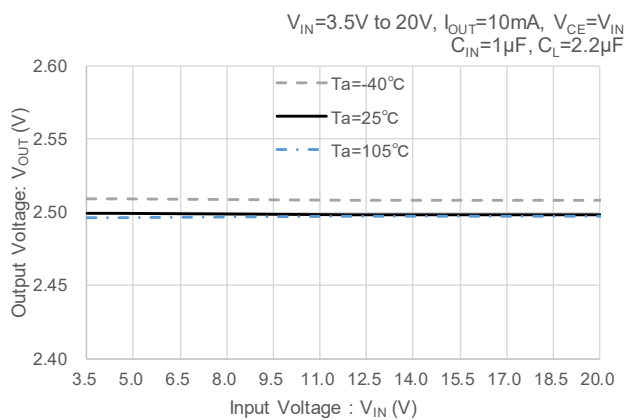
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) Output Voltage vs. Input Voltage

(7) Output Voltage vs. Ambient Temperature

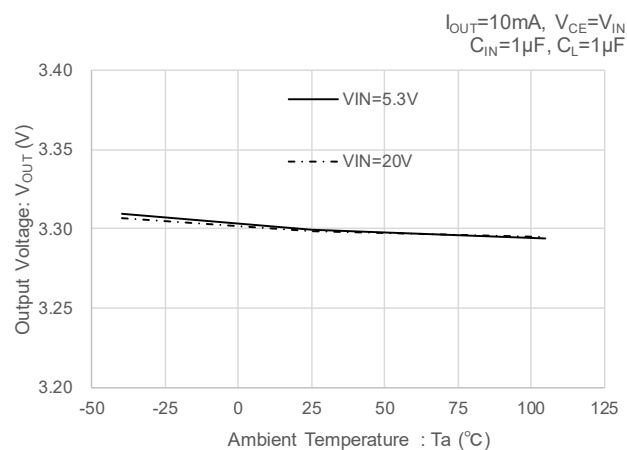
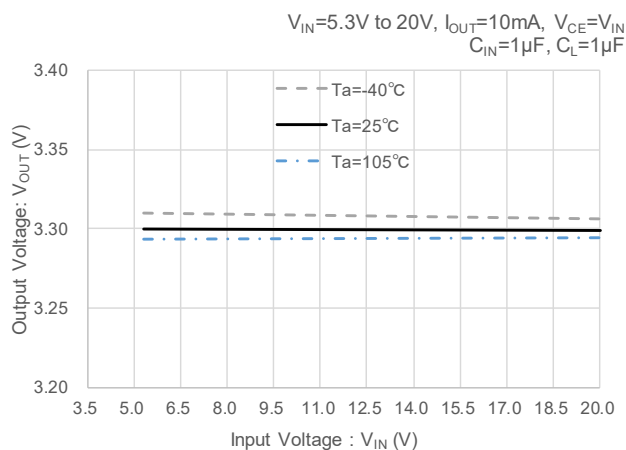
(6-1)  $V_{OUT(T)}=2.5V$

(7-1)  $V_{OUT(T)}=2.5V$



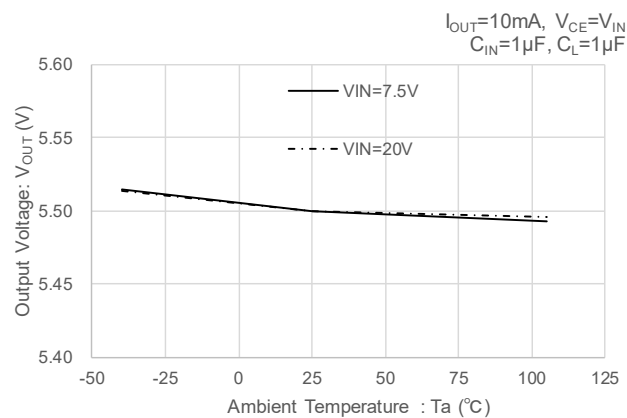
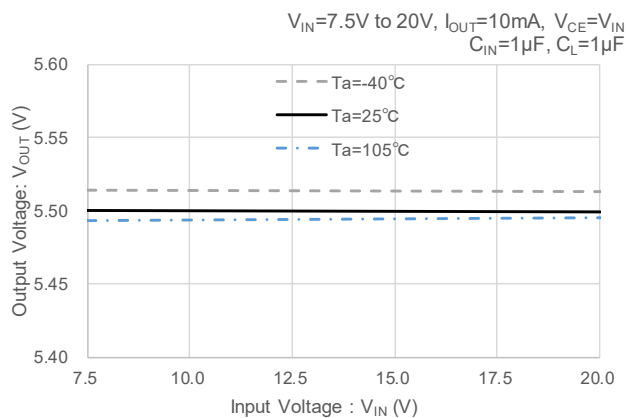
(6-2)  $V_{OUT(T)}=3.3V$

(7-2)  $V_{OUT(T)}=3.3V$



(6-3)  $V_{OUT(T)}=5.5V$

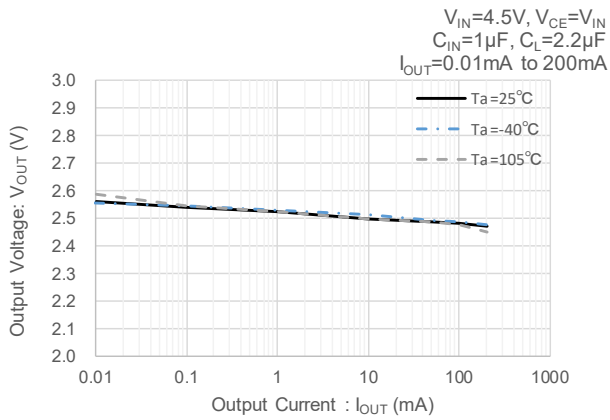
(7-3)  $V_{OUT(T)}=5.5V$



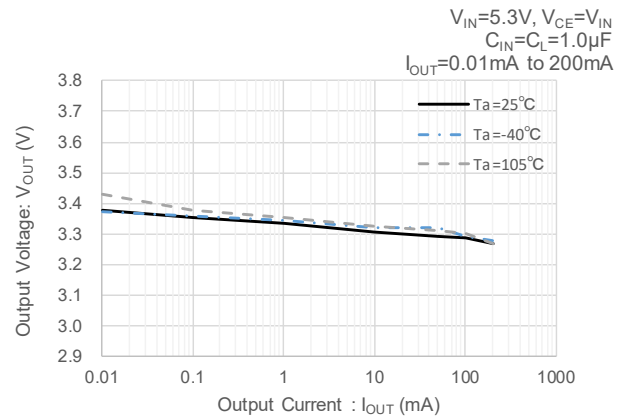
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (8) Output Voltage vs. Output Current

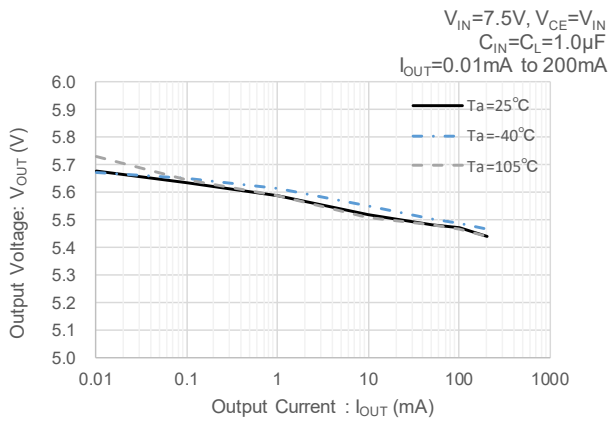
(8-1)  $V_{OUT(T)}=2.5V$



(8-2)  $V_{OUT(T)}=3.3V$



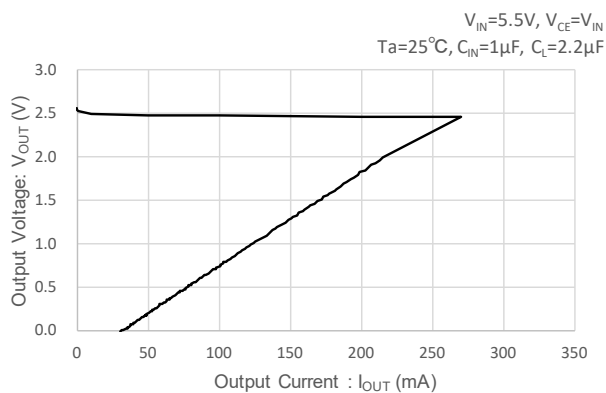
(8-3)  $V_{OUT(T)}=5.5V$



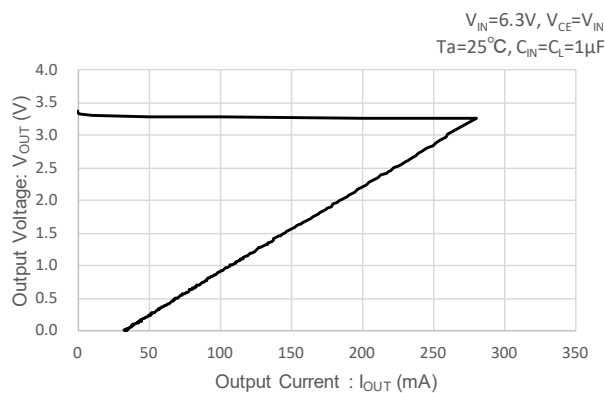
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(9) Output Voltage vs. Output Current (Current Limit)

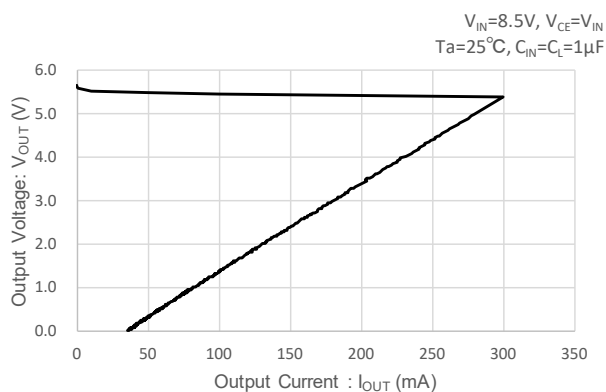
(9-1)  $V_{OUT(T)}=2.5V$



(9-2)  $V_{OUT(T)}=3.3V$



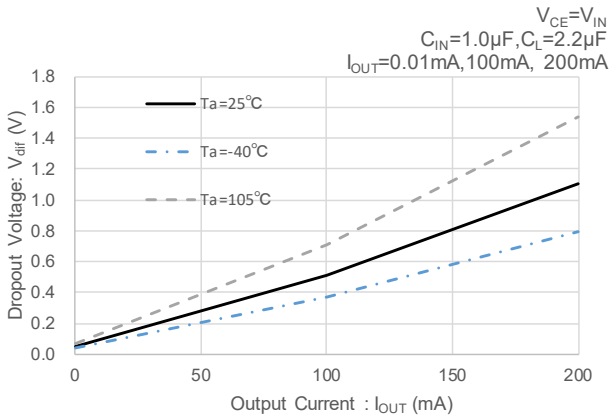
(9-3)  $V_{OUT(T)}=5.5V$



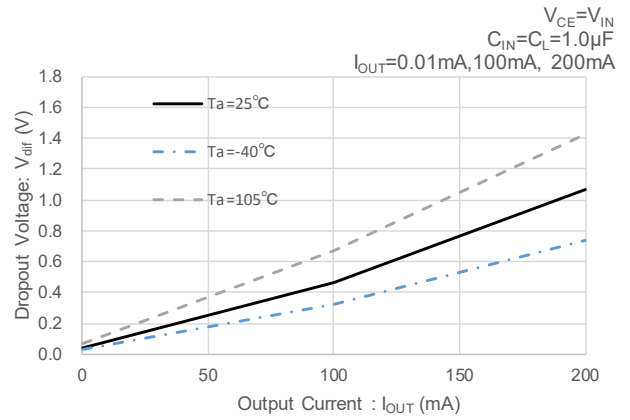
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (10) Dropout Voltage vs. Output Current

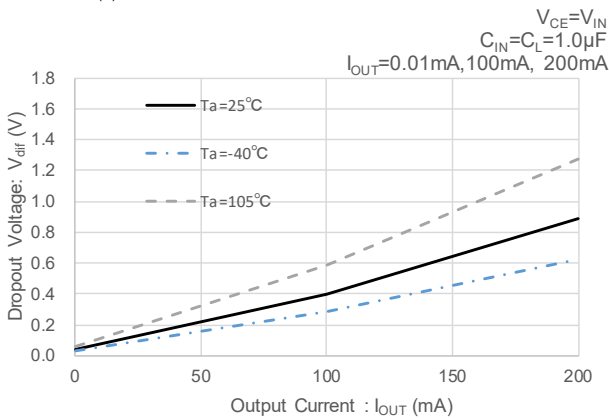
(10-1)  $V_{OUT(T)}=2.5V$



(10-2)  $V_{OUT(T)}=3.3V$

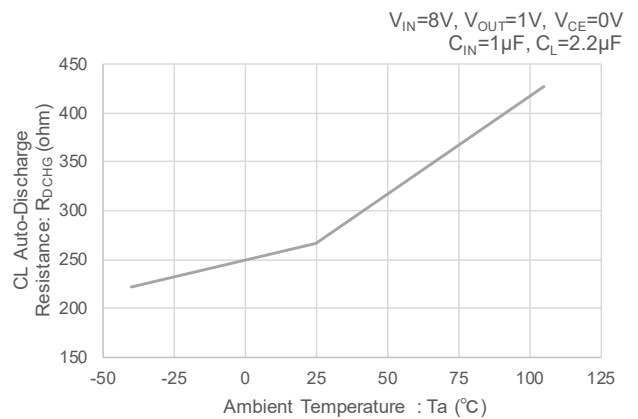


(10-3)  $V_{OUT(T)}=5.5V$



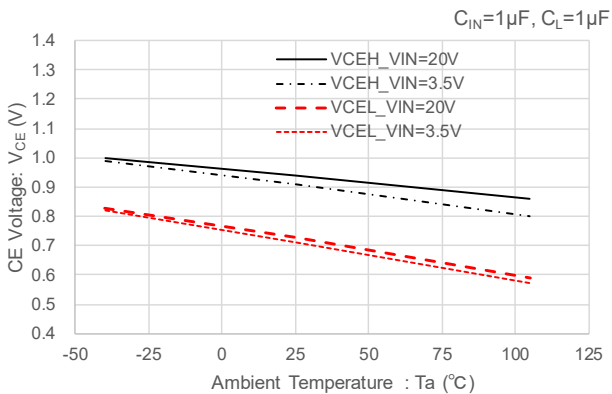
(11)  $C_L$  Auto-Discharge Resistance vs. Ambient Temperature (Type A)

(11-1)  $V_{OUT(T)}=2.5V$



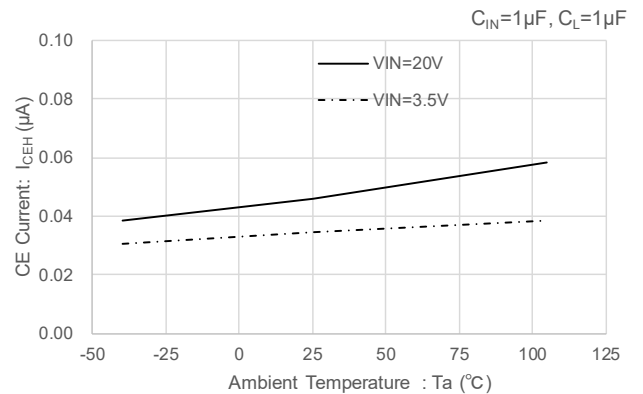
### (12) CE "H", CE "L" Level Voltage vs. Ambient Temperature

(12-1)  $V_{OUT(T)}=2.5V$



### (13) CE "H" Level Current vs. Ambient Temperature

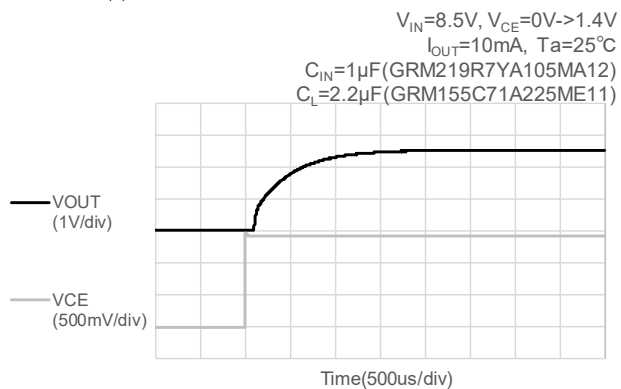
(13-1)  $V_{OUT(T)}=2.5V$



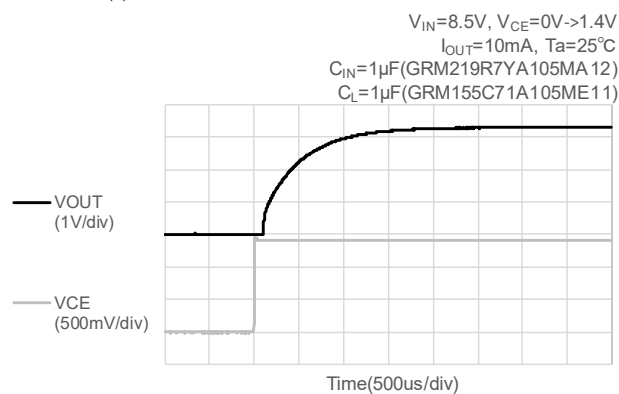
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (14) CE Rising Response Time

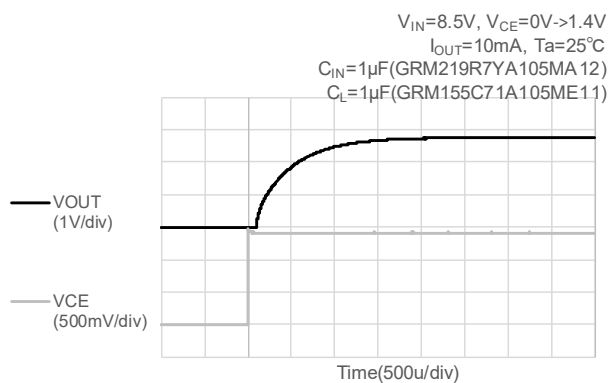
(14-1)  $V_{OUT(\tau)}=2.5V$



(14-2)  $V_{OUT(\tau)}=3.3V$

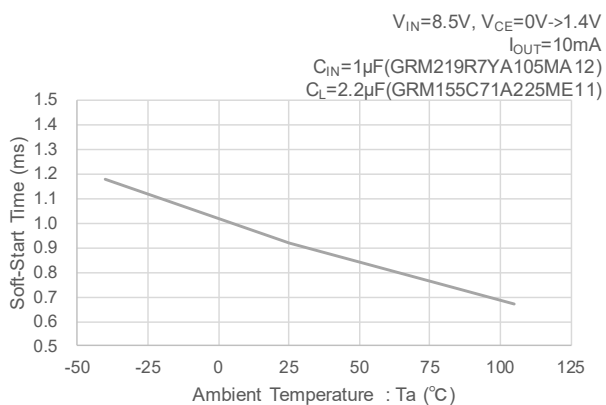


(14-3)  $V_{OUT(\tau)}=5.5V$



### (15) Soft-Start Time vs. Ambient Temperature

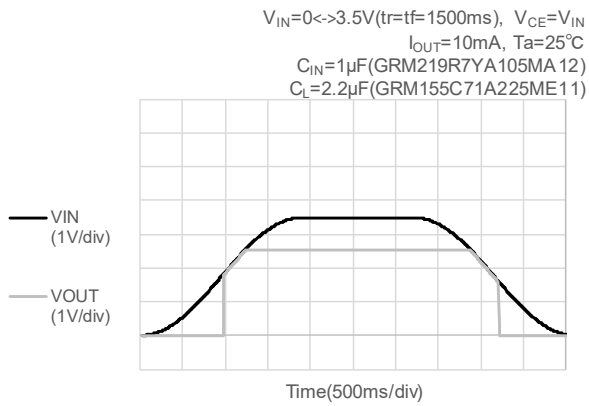
(15-1)  $V_{OUT(\tau)}=2.5V$



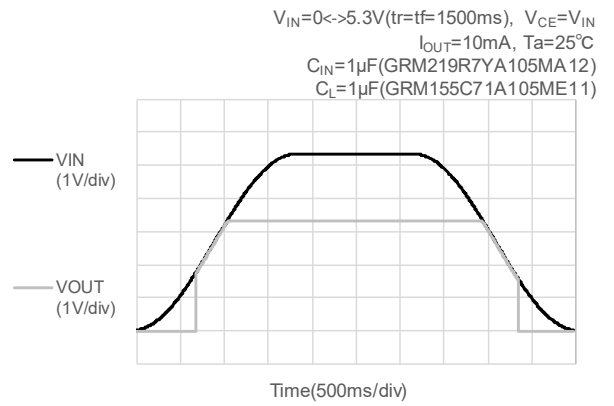
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (16) Input Voltage Rising Response

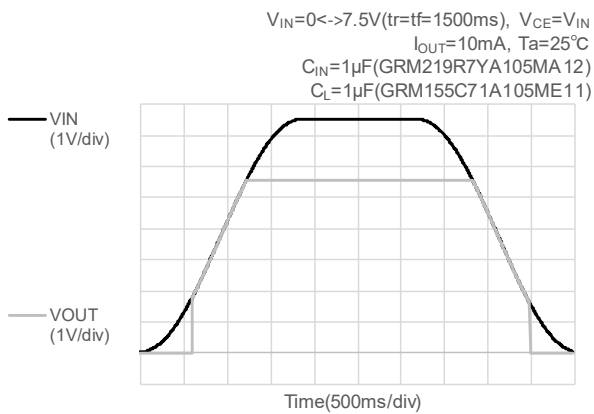
(16-1)  $V_{OUT(T)}=2.5V$



(16-2)  $V_{OUT(T)}=3.3V$



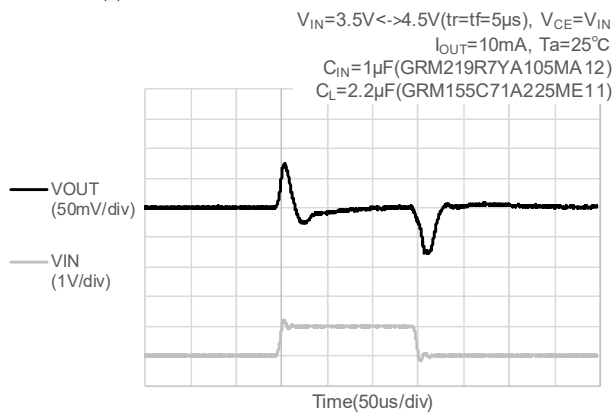
(16-3)  $V_{OUT(T)}=5.5V$



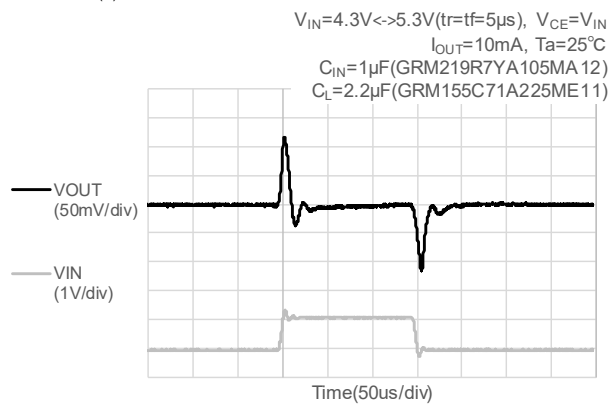
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (17) Input Voltage Transient Response

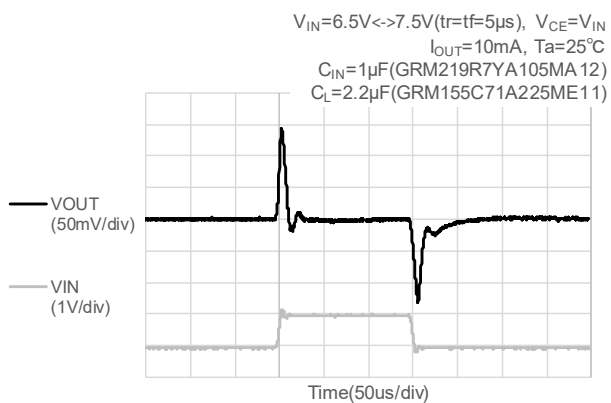
(17-1)  $V_{OUT(T)}=2.5V$



(17-2)  $V_{OUT(T)}=3.3V$



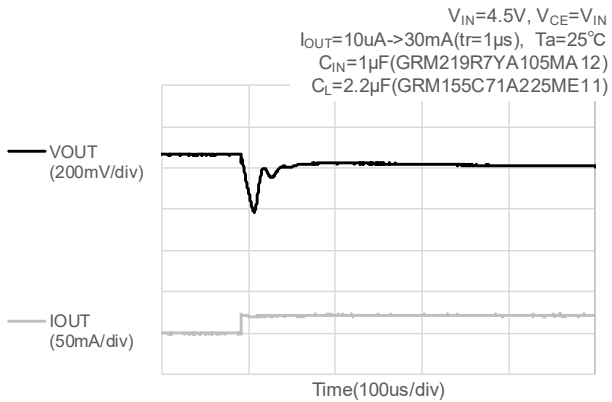
(17-3)  $V_{OUT(T)}=5.5V$



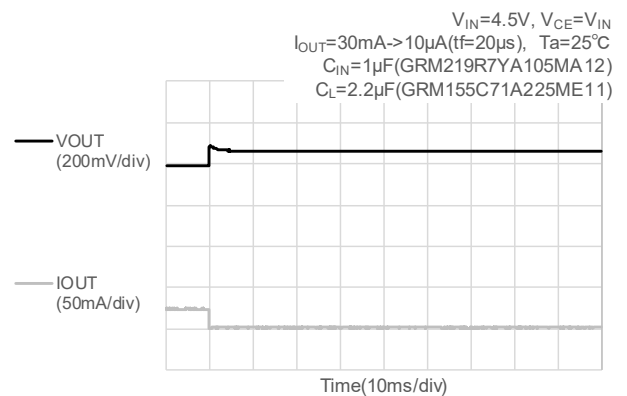
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (18) Load Transient Response1

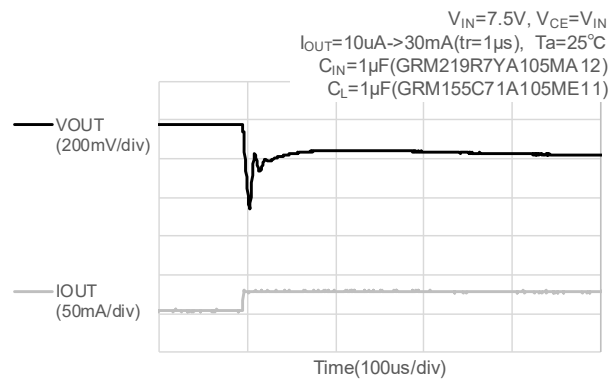
(18-1-1)  $V_{OUT(T)}=2.5V$  (Rising Edge)



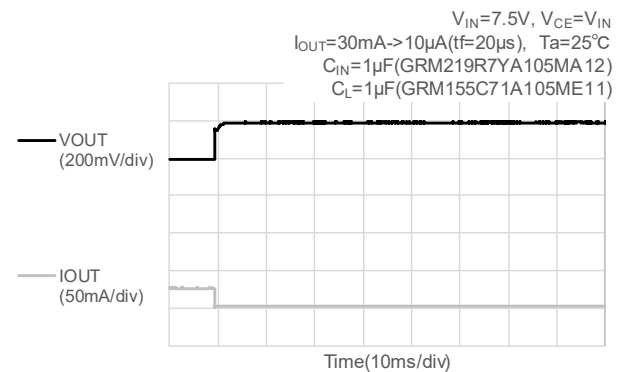
(18-1-2)  $V_{OUT(T)}=2.5V$  (Falling Edge)



(18-2-1)  $V_{OUT(T)}=5.5V$  (Rising Edge)



(18-2-2)  $V_{OUT(T)}=5.5V$  (Falling Edge)

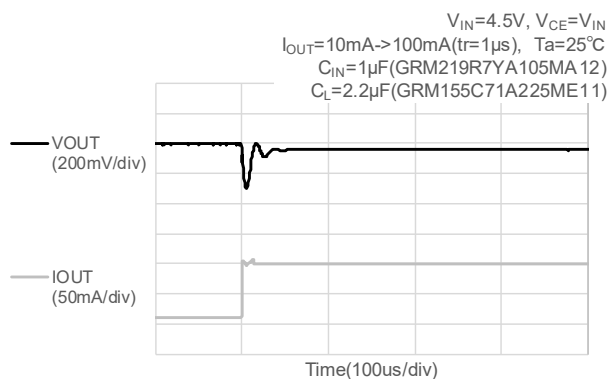




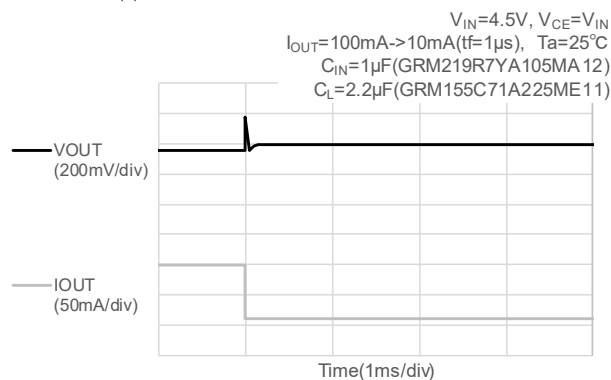
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (19) Load Transient Response2

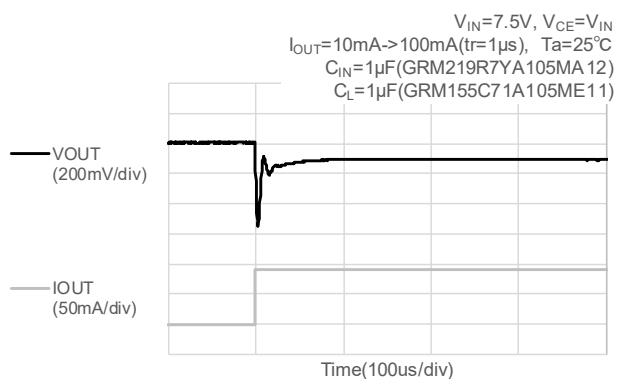
(19-1-1)  $V_{OUT(T)}=2.5V$  (Rising Edge)



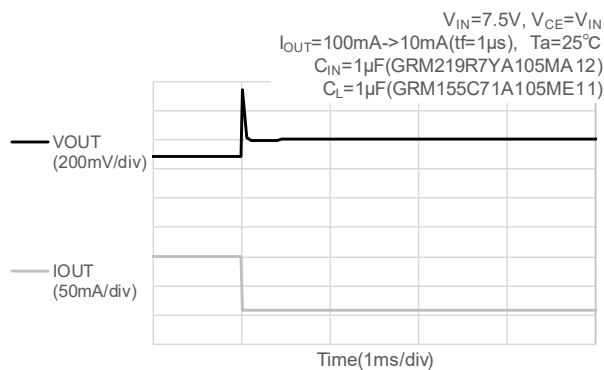
(19-1-2)  $V_{OUT(T)}=2.5V$  (Falling Edge)



(19-2-1)  $V_{OUT(T)}=5.5V$  (Rising Edge)



(19-2-2)  $V_{OUT(T)}=5.5V$  (Falling Edge)

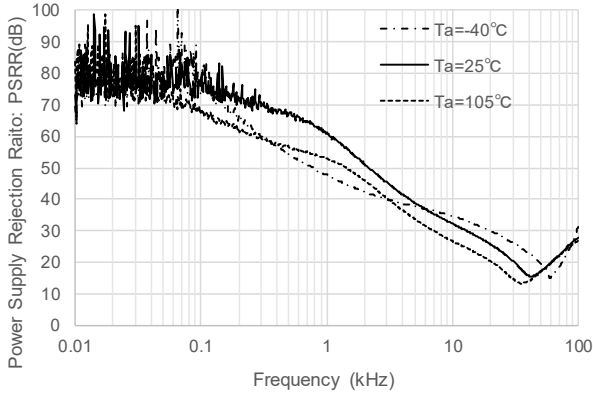


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (20) Power Supply Rejection Ratio

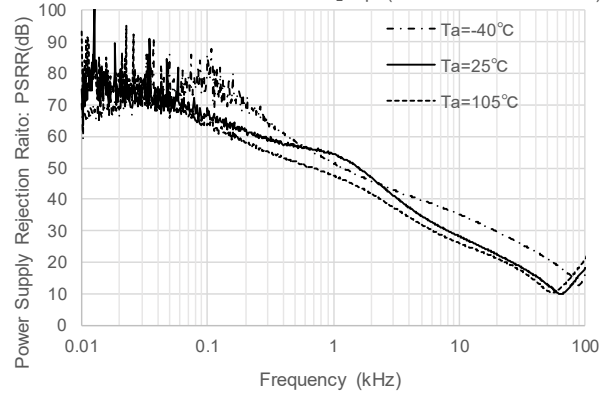
(20-1)  $V_{OUT(T)}=2.5V$

$V_{IN}=4.5V+0.5Vp-pAC$ ,  $V_{CE}=V_{IN}$ ,  $I_{OUT}=30mA$   
 $C_{IN}=1\mu F$ (GRM219R7YA105MA12)  
 $C_L=2\mu F$ (GRM155C71A225ME11)



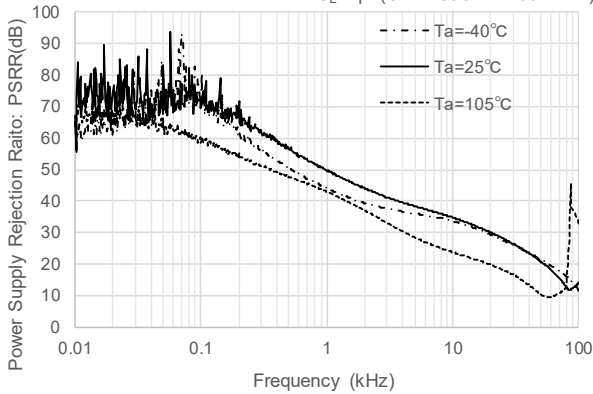
(20-2)  $V_{OUT(T)}=3.3V$

$V_{IN}=5.3V+0.5Vp-pAC$ ,  $V_{CE}=V_{IN}$ ,  $I_{OUT}=30mA$   
 $C_{IN}=1\mu F$ (GRM219R7YA105MA12)  
 $C_L=1\mu F$ (GRM155C71A105ME11)



(20-3)  $V_{OUT(T)}=5.5V$

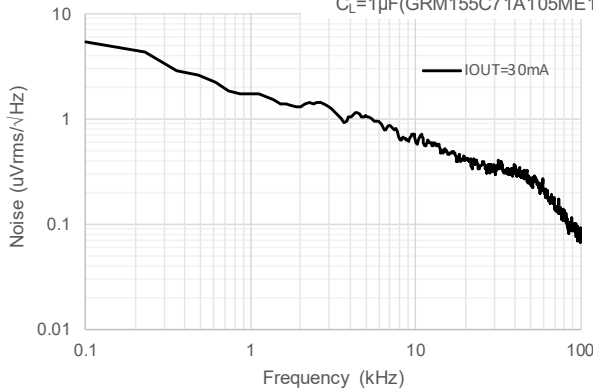
$V_{IN}=7.5V+0.5Vp-pAC$ ,  $V_{CE}=V_{IN}$ ,  $I_{OUT}=30mA$   
 $C_{IN}=1\mu F$ (GRM219R7YA105MA12)  
 $C_L=1\mu F$ (GRM155C71A105ME11)



### (21) Output Noise Density

(21-1) XC6705A331M ( $V_{OUT(T)}=3.3V$ )

$V_{IN}=V_{OUT(T)}+2.0V$ ,  $V_{CE}=V_{IN}$ ,  $T_a=25^\circ C$   
 $C_{IN}=1\mu F$ (GRM219R7YA105MA12)  
 $C_L=1\mu F$ (GRM155C71A105ME11)



## ■ PACKAGING INFORMATION

For the latest package information go to, [www.torexsemi.com/technical-support/packages](http://www.torexsemi.com/technical-support/packages)

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-25	<a href="#">SOT-25 PKG</a>	<a href="#">SOT-25 Power Dissipation</a>
USP-4	<a href="#">USP-4 PKG</a>	<a href="#">USP-4 Power Dissipation</a>

## MARKING RULE

### ● SOT-25

MARK① Represents products series

MARK	PRODUCT SERIESIES
M	XC6705A/B***M*-G

MARK② Represents type, output voltage range

MARK	Type	Output Voltage Range (V)	PRODUCT SERIESIES
A	A	2.5~3.6	XC6705A***M*-G
B		3.7~4.8	
C		4.9~5.5	
D	B	2.5~3.6	XC6705B***M*-G
E		3.7~4.8	
F		4.9~5.5	

MARK③ Represents output voltage

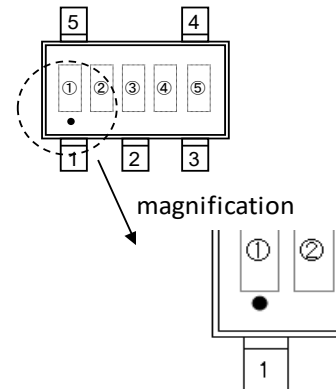
MARK	OUTPUT VOLTAGE (V)			MARK	OUTPUT VOLTAGE (V)		
0	2.5	3.7	4.9	6	3.1	4.3	5.5
1	2.6	3.8	5.0	7	3.2	4.4	/
2	2.7	3.9	5.1	8	3.3	4.5	/
3	2.8	4.0	5.2	9	3.4	4.6	/
4	2.9	4.1	5.3	A	3.5	4.7	/
5	3.0	4.2	5.4	B	3.6	4.8	/

MARK④,⑤ represents production lot number

01~09, 0A~0Z, 11...9Z, A1~A9, AA...Z9, ZA~ZZ in order. (G, I, J, O, Q, W excluded)

\* No character inversion used.

SOT-25



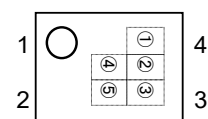
## MARKING RULE (Continued)

### ● USP-4

USP-4

MARK① Represents products series

MARK	PRODUCT SERIESIES
4	XC6705****G*-G



MARK② Represents type, output voltage range

MARK	Type	Output Voltage Range (V)	PRODUCT SERIESIES
A	A	2.5~3.6	XC6705A***G*-G
B		3.7~4.8	
C		4.9~5.5	
D	B	2.5~3.6	XC6705B***G*-G
E		3.7~4.8	
F		4.9~5.5	

MARK③ Represents output voltage

MARK	OUTPUT VOLTAGE (V)			MARK	OUTPUT VOLTAGE (V)		
0	2.5	3.7	4.9	6	3.1	4.3	5.5
1	2.6	3.8	5.0	7	3.2	4.4	/
2	2.7	3.9	5.1	8	3.3	4.5	/
3	2.8	4.0	5.2	9	3.4	4.6	/
4	2.9	4.1	5.3	A	3.5	4.7	/
5	3.0	4.2	5.4	B	3.6	4.8	/

MARK④,⑤ represents production lot number

01~09, 0A~0Z, 11···9Z, A1~A9, AA···Z9, ZA~ZZ in order. (G, I, J, O, Q, W excluded)

\* No character inversion used.