Spartan-6 Family Overview

DS160 (v2.0) October 25, 2011 **Product Specification**

General Description

The Spartan®-6 family provides leading system integration capabilities with the lowest total cost for high-volume applications. The thirteen-member family delivers expanded densities ranging from 3,840 to 147,443 logic cells, with half the power consumption of previous Spartan families, and faster, more comprehensive connectivity. Built on a mature 45 nm low-power copper process technology that delivers the optimal balance of cost, power, and performance, the Spartan-6 family offers a new, more efficient, dual-register 6-input look-up table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb (2 x 9 Kb) block RAMs, second generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, SelectIO™ technology, power-optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease of use. Spartan-6 FPGAs offer the best solution for high-volume logic designs, consumer-oriented DSP designs, and cost-sensitive embedded applications. Spartan-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components that enable designers to focus on innovation as soon as their development cycle begins.

Summary of Spartan-6 FPGA Features

- Spartan-6 Family:
  - Spartan-6 LX FPGA: Logic optimized
  - Spartan-6 LXT FPGA: High-speed serial connectivity
- Designed for low cost
  - Multiple efficient integrated blocks
  - Optimized selection of I/O standards
  - Staggered pads
  - High-volume plastic wire-bonded packages
- Low static and dynamic power
  - 45 nm process optimized for cost and low power
  - Hibernate power-down mode for zero power
  - Suspend mode maintains state and configuration with multi-pin wake-up, control enhancement
  - Lower-power 1.0V core voltage (LX FPGAs, -1L only)
  - High performance 1.2V core voltage (LX and LXT FPGAs, -2, -3, and -3N speed grades)
- Multi-voltage, multi-standard SelectIO™ interface banks
  - Up to 1,080 Mb/s data transfer rate per differential I/O
  - Selectable output drive, up to 24 mA per pin
  - 3.3V to 1.2V I/O standards and protocols
  - Low-cost HSTL and SSTL memory interfaces
  - Hot swap compliance
  - Adjustable I/O slew rates to improve signal integrity
- High-speed GTP serial transceivers in the LXT FPGAs
  - Up to 3.2 Gb/s
  - High-speed interfaces including: Serial ATA, Aurora, 1G Ethernet, PCI Express, OBSAI, CPRI, EPON, GPON, DisplayPort, and XAUI
- Integrated Endpoint block for PCI Express designs (LXT)
- Low-cost PCI® technology support compatible with the 33 MHz, 32- and 64-bit specification.
- Efficient DSP48A1 slices
  - High-performance arithmetic and signal processing
  - Fast 18 x 18 multiplier and 48-bit accumulator
  - Pipelining and cascading capability
  - Pre-adder to assist filter applications
- Integrated Memory Controller blocks
  - DDR, DDR2, DDR3, and LPDDR support
  - Data rates up to 800 Mb/s (12.8 Gb/s peak bandwidth)
  - Multi-port bus structure with independent FIFO to reduce design timing issues
- Abundant logic resources with increased logic capacity
  - Optional shift register or distributed RAM support
  - Efficient 6-input LUTs improve performance and minimize power
  - LUT with dual flip-flops for pipeline centric applications
- Block RAM with a wide range of granularity
  - Fast block RAM with byte write enable
  - 18 Kb blocks that can be optionally programmed as two independent 9 Kb block RAMs
- Clock Management Tile (CMT) for enhanced performance
  - Low noise, flexible clocking
  - Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion
  - Phase-Locked Loops (PLLs) for low-jitter clocking
  - Frequency synthesis with simultaneous multiplication, division, and phase shifting
  - Sixteen low-skew global clock networks
- Simplified configuration, supports low-cost standards
  - 2-pin auto-detect configuration
  - Broad third-party SPI (up to x4) and NOR flash support
  - Feature rich Xilinx Platform Flash with JTAG
  - MultiBoot support for remote upgrade with multiple bitstreams, using watchdog protection
- Enhanced security for design protection
  - Unique Device DNA identifier for design authentication
  - AES bitstream encryption in the larger devices
- Faster embedded processing with enhanced, low cost, MicroBlaze™ soft processor
- Industry-leading IP and reference designs

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Spartan-6 FPGA Feature Summary

Table 1: **Spartan-6 FPGA Feature Summary by Device**

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[5]	Memory Controller Blocks (Max)[6]	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

Notes:

1. Spartan-6 FPGA logic cell ratings reflect the increased logic cell capability offered by the new 6-input LUT architecture.
2. Each Spartan-6 FPGA slice contains four LUTs and eight flip-flops.
3. Each DSP48A1 slice contains an 18 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.
5. Each CMT contains two DCMs and one PLL.
6. Memory Controller Blocks are not supported in the -3N speed grade.

Spartan-6 FPGA Device-Package Combinations and Available I/Os

Spartan-6 FPGA package combinations with the available I/Os and GTP transceivers per package are shown in Table 2. Due to the transceivers, the LX and LXT pinouts are not compatible.

Table 2: **Spartan-6 Device-Package Combinations and Maximum Available I/Os**

Package	CPG196[1]	TQG144[1]	CSG225[2]	FT(G)256[3]	CSG324		FG(G)484[3,4]		CSG484[4]		FG(G)676[3]		FG(G)900[3]	
Body Size (mm)	8 x 8	20 x 20	13 x 13	17 x 17	15 x 15		23 x 23		19 x 19		27 x 27		31 x 31	
Pitch (mm)	0.5	0.5	0.8	1.0	0.8		1.0		0.8		1.0		1.0	
Device	User I/O	User I/O	User I/O	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O
XC6SLX4	106	102	132											
XC6SLX9	106	102	160	186	NA	200								
XC6SLX16	106		160	186	NA	232								
XC6SLX25				186	NA	226	NA	266						
XC6SLX45					NA	218	NA	316	NA	320	NA	358		
XC6SLX75							NA	280	NA	328	NA	408		
XC6SLX100							NA	326	NA	338	NA	480		
XC6SLX150							NA	338	NA	338	NA	498	NA	576
XC6SLX25T					2	190	2	250						
XC6SLX45T					4	190	4	296	4	296				
XC6SLX75T							4	268	4	292	8	348		
XC6SLX100T							4	296	4	296	8	376	8	498
XC6SLX150T							4	296	4	296	8	396	8	540

Notes:
1. There is no memory controller on the devices in these packages.
2. Memory controller block support is x8 on the XC6SLX9 and XC6SLX16 devices in the CSG225 package. There is no memory controller in the XC6SLX4.
3. These devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.
4. These packages support two of the four memory controllers in the XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T devices.

Configuration

Spartan-6 FPGAs store the customized configuration data in SRAM-type internal latches. The number of configuration bits is between 3 Mb and 33 Mb depending on device size and user-design implementation options. The configuration storage is volatile and must be reloaded whenever the FPGA is powered up. This storage can also be reloaded at any time by pulling the PROGRAM_B pin Low. Several methods and data formats for loading configuration are available.

Bit-serial configurations can be either master serial mode, where the FPGA generates the configuration clock (CCLK) signal, or slave serial mode, where the external configuration data source also clocks the FPGA. For byte-wide configurations, master SelectMAP mode generates the CCLK signal while slave SelectMAP mode receives the CCLK signal for the 8- and 16-bit-wide transfer. In master serial mode, the beginning of the bitstream can optionally switch the clocking source to an external clock, which can be faster or more precise than the internal clock. The available JTAG pins use boundary-scan protocols to load bit-serial configuration data.

The bitstream configuration information is generated by the ISE® software using a program called BitGen. The configuration process typically executes the following sequence:

- Detects power-up (power-on reset) or PROGRAM_B when Low.
- Clears the whole configuration memory.
- Samples the mode pins to determine the configuration mode: master or slave, bit-serial or parallel.
- Loads the configuration data starting with the bus-width detection pattern followed by a synchronization word, checks for the proper device code, and ends with a cyclic redundancy check (CRC) of the complete bitstream.
- Starts a user-defined sequence of events: releasing the internal reset (or preset) of flip-flops, optionally waiting for the DCMs and/or PLLs to lock, activating the output drivers, and transitioning the DONE pin to High.

The Master Serial Peripheral Interface (SPI) and the Master Byte-wide Peripheral Interface (BPI) are two common methods used for configuring the FPGA. The Spartan-6 FPGA configures itself from a directly attached industry-standard SPI serial flash PROM. The Spartan-6 FPGA can configure itself via BPI when connected to an industry-standard parallel NOR flash. Note that BPI configuration is not supported in the XC6SLX4, XC6SLX25, and XC6SLX25T nor is BPI available when using Spartan-6 FPGAs in TQG144 and CPG196 packages.

Spartan-6 FPGAs support MultiBoot configuration, where two or more FPGA configuration bitstreams can be stored in a single configuration source. The FPGA application controls which configuration to load next and when to load it.

Spartan-6 FPGAs also include a unique, factory-programmed Device DNA identifier that is useful for tracking purposes, anti-cloning designs, or IP protection. In the largest devices, bitstreams can be copy protected using AES encryption.

Readback

Most configuration data can be read back without affecting the system's operation.

CLBs, Slices, and LUTs

Each configurable logic block (CLB) in Spartan-6 FPGAs consists of two slices, arranged side-by-side as part of two vertical columns. There are three types of CLB slices in the Spartan-6 architecture: SLICEM, SLICEL, and SLICEX. Each slice contains four LUTs, eight flip-flops, and miscellaneous logic. The LUTs are for general-purpose combinatorial and sequential logic support. Synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features. Expert designers can also instantiate them.

SLICEM

One quarter (25%) of Spartan-6 FPGA slices are SLICEMs. Each of the four SLICEM LUTs can be configured as either a 6-input LUT with one output, or as dual 5-input LUTs with identical 5-bit addresses and two independent outputs. These LUTs can also be used as distributed 64-bit RAM with 64 bits or two times 32 bits per LUT, as a single 32-bit shift register (SRL32), or as two 16-bit shift registers (SRL16s) with addressable length. Each LUT output can be registered in a flip-flop within the CLB. For arithmetic operations, a high-speed carry chain propagates carry signals upwards in a column of slices.

SLICEL

One quarter (25%) of Spartan-6 FPGA slices are SLICELs, which contain all the features of the SLICEM except the memory/shift register function.

SLICEX

One half (50%) of Spartan-6 FPGA slices are SLICEXs. The SLICEXs have the same structure as SLICELs except the arithmetic carry option and the wide multiplexers.

Clock Management

Each Spartan-6 FPGA has up to six CMTs, each consisting of two DCMs and one PLL, which can be used individually or cascaded.

DCM

The DCM provides four phases of the input frequency (CLKIN): shifted 0°, 90°, 180°, and 270° (CLK0, CLK90, CLK180, and CLK270). It also provides a doubled frequency CLK2X and its complement CLK2X180. The CLKDV output provides a fractional clock frequency that can be phase-aligned to CLK0. The fraction is programmable as every integer from 2 to 16, as well as 1.5, 2.5, 3.5 . . . 7.5. CLKIN can optionally be divided by 2. The DCM can be a zero-delay clock buffer when a clock signal drives CLKIN, while the CLK0 output is fed back to the CLKFB input.

Frequency Synthesis

Independent of the basic DCM functionality, the frequency synthesis outputs CLKFX and CLKFX180 can be programmed to generate any output frequency that is the DCM input frequency (F_{IN}) multiplied by M and simultaneously divided by D, where M can be any integer from 2 to 32 and D can be any integer from 1 to 32.

Phase Shifting

With CLK0 connected to CLKFB, all nine CLK outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, CLKDV, CLKFX, and CLKFX180) can be shifted by a common amount, defined as any integer multiple of a fixed delay. A fixed DCM delay value (fraction of the input period) can be established by configuration and can also be incremented or decremented dynamically.

Spread-Spectrum Clocking

The DCM can accept and track typical spread-spectrum clock inputs, provided they abide by the input clock specifications listed in the *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*. Spartan-6 FPGAs can generate a spread-spectrum clock source from a standard fixed-frequency oscillator.

PLL

The PLL can serve as a frequency synthesizer for a wider range of frequencies and as a jitter filter for incoming clocks in conjunction with the DCMs. The heart of the PLL is a voltage-controlled oscillator (VCO) with a frequency range of 400 MHz to 1,080 MHz, thus spanning more than one octave. Three sets of programmable frequency dividers (D, M, and O) adapt the VCO to the required application.

The pre-divider D (programmable by configuration) reduces the input frequency and feeds one input of the traditional PLL phase comparator. The feedback divider (programmable by configuration) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its controllable frequency range.

The VCO has eight equally spaced outputs (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be selected to drive one of the six output dividers, O0 to O5 (each programmable by configuration to divide by any integer from 1 to 128).

Clock Distribution

Each Spartan-6 FPGA provides abundant clock lines to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew.

Global Clock Lines

In each Spartan-6 FPGA, 16 global-clock lines have the highest fanout and can reach every flip-flop clock. Global clock lines must be driven by global clock buffers, which can also perform glitchless clock multiplexing and the clock enable function. Global clocks are often driven from the CMTs, which can completely eliminate the basic clock distribution delay.

I/O Clocks

I/O clocks are especially fast and serve only the localized input and output delay circuits and the I/O serializer/deserializer (SERDES) circuits, as described in the I/O Logic section.

Block RAM

Every Spartan-6 FPGA has between 12 and 268 dual-port block RAMs, each storing 18 Kb. Each block RAM has two completely independent ports that share only the stored data.

Synchronous Operation

Each memory access, whether read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. The data output is always latched, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation in dual-port mode, the data output can reflect either the previously stored data, the newly written data, or remain unchanged.

Programmable Data Width

- Each port can be configured as 16K × 1, 8K × 2, 4K × 4, 2K × 9 (or 8), 1K × 18 (or 16), or 512 x 36 (or 32).
- The x9, x18, and x36 configurations include parity bits. The two ports can have different aspect ratios.
- Each block RAM can be divided into two completely independent 9 Kb block RAMs that can each be configured to any aspect ratio from 8K x 1 to 512 x 18, with 256 x 36 supported in simple dual-port mode.

Memory Controller Block

Most Spartan-6 devices include dedicated memory controller blocks (MCBs), each targeting a single-chip DRAM (either DDR, DDR2, DDR3, or LPDDR), and supporting access rates of up to 800 Mb/s.

The MCB has dedicated routing to predefined FPGA I/Os. If the MCB is not used, these I/Os are available as general purpose FPGA I/Os. The memory controller offers a complete multi-port arbitrated interface to the logic inside the Spartan-6 FPGA. Commands can be pushed, and data can be pushed to and pulled from independent built-in FIFOs, using conventional FIFO control signals. The multi-port memory controller can be configured in many ways. An internal 32-, 64-, or 128-bit data interface provides a simple and reliable interface to the MCB.

The MCB can be connected to 4-, 8-, or 16-bit external DRAM. The MCB, in many applications, provides a faster DRAM interface compared to traditional internal data buses, which are wider and are clocked at a lower frequency. The FPGA logic interface can be flexibly configured irrespective of the physical memory device. The MCB functionality is not supported in the -3N speed grade.

Digital Signal Processing—DSP48A1 Slice

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All Spartan-6 FPGAs have many dedicated, full-custom, low-power DSP slices, combining high speed with small size, while retaining system design flexibility.

Each DSP48A1 slice consists of a dedicated 18 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating at up to 390 MHz. The DSP48A1 slice provides extensive pipelining and extension capabilities that enhance speed and efficiency of many applications, even beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter. The multiplier can perform barrel shifting.

Input/Output

The number of I/O pins varies from 102 to 576, depending on device and package size. Each I/O pin is configurable and can comply with a large number of standards, using up to 3.3V. The *Spartan-6 FPGA SelectIO Resources User Guide* describes the I/O compatibilities of the various I/O options. With the exception of supply pins and a few dedicated configuration pins, all other package pins have the same I/O capabilities, constrained only by certain banking rules. All user I/O is bidirectional; there are no input-only pins.

All I/O pins are organized in banks, with four banks on the smaller devices and six banks on the larger devices. Each bank has several common V_{CCO} output supply-voltage pins, which also powers certain input buffers. Some single-ended input buffers require an externally applied reference voltage (V_{REF}). There are several dual-purpose V_{REF}-I/O pins in each bank. In a given bank, when I/O standard calls for a V_{REF} voltage, each V_{REF} pin in that bank must be connected to the same voltage rail and can not be used as an I/O pin.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure, driving High towards V_{CCO} or Low towards ground, and can be put into high-Z state. Many I/O features are available to the system designer to optionally invoke in each I/O in their design, such as weak internal pull-up and pull-down resistors, strong internal split-termination input resistors, adjustable output drive-strengths and slew-rates, and differential termination resistors. See the *Spartan-6 FPGA SelectIO Resources User Guide* for more details on available options for each I/O standard.

I/O Logic

Input and Output Delay

This section describes the available logic resources connected to the I/O interfaces. All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 256 increments (except in the -1L speed grade). This is implemented as IODELAY2. The identical delay value is available either for data input or output. For a bidirectional data line, the transfer from input to output delay is automatic. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

Because these tap delays vary with supply voltage, process, and temperature, an optional calibration mechanism is built into each IODELAY2:

- For source synchronous designs where more accuracy is required, the calibration mechanism can (optionally) determine dynamically how many taps are needed to delay data by one full I/O clock cycle, and then programs the IODELAY2 with 50% of that value, thus centering the I/O clock in the middle of the data eye.
- A special mode is available only for differential inputs, which uses a phase-detector mechanism to determine whether the incoming data signal is being accurately sampled in the middle of the eye. The results from the phase-detector logic can be used to either increment or decrement the input delay, one tap at a time, to ensure error-free operation at very high bit rates.

ISERDES and OSERDES

Many applications combine high-speed bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each input has access to its own deserializer (serial-to-parallel converter) with programmable parallel width of 2, 3, or 4 bits. Where differential inputs are used, the two serializers can be cascaded to provide parallel widths of 5, 6, 7, or 8 bits. Each output has access to its own serializer (parallel-to-serial converter) with programmable parallel width of 2, 3, or 4 bits. Two serializers can be cascaded when a differential driver is used to give access to bus widths of 5, 6, 7, or 8 bits.

When distributing a double data rate clock, all SerDes data is actually clocked in/out at single data rate to eliminate the possibility of bit errors due to duty cycle distortion. This faster single data rate clock is either derived via frequency multiplication in a PLL, or doubled locally in each IOB by differentiating both clock edges when the incoming clock uses double data rate.

Low-Power Gigabit Transceiver

Ultra-fast data transmission between ICs, over the backplane, or over longer distances is becoming increasingly popular and important. It requires specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues at these high data rates.

All Spartan-6 LXT devices have 2–8 gigabit transceiver circuits. Each GTP transceiver is a combined transmitter and receiver capable of operating at data rates up to 3.2 Gb/s. The transmitter and receiver are independent circuits that use separate PLLs to multiply the reference frequency input by certain programmable numbers between 2 and 25, to become the bit-serial data clock. Each GTP transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 8, 10, 16, or 20. The transmitter output drives the PC board with a single-channel differential current-mode logic (CML) output signal.

TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through a small FIFO and can optionally be modified with the 8B/10B algorithm to guarantee a sufficient number of transitions. The bit-serial output signal drives two package pins with complementary CML signals. This output signal pair has programmable signal swing as well as programmable pre-emphasis to compensate for PC board losses and other interconnect characteristics.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit serial differential signal into a parallel stream of words, each 8, 10, 16, or 20 bits wide. The receiver takes the incoming differential data stream, feeds it through a programmable equalizer (to compensate for the PC board and other interconnect characteristics), and uses the F_{REF} input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the 8B/10B encoding scheme. Parallel data is then transferred into the FPGA logic using the RXUSRCLK clock. The serial-to-parallel conversion ratio can be 8, 10, 16, or 20.

Integrated Endpoint Block for PCI Express Designs

The PCI Express standard is a packet-based, point-to-point serial interface standard. The differential signal transmission uses an embedded clock, which eliminates the clock-to-data skew problems of traditional wide parallel buses.

The PCI Express Base Specification 1.1 defines bit rate of 2.5 Gb/s per lane, per direction (transmit and receive). When using 8B/10B encoding, this supports a data rate of 2.0 Gb/s per lane.

The Spartan-6 LXT devices include one integrated Endpoint block for PCI Express technology that is compliant with the PCI Express Base Specification Revision 1.1. This block is highly configurable to system design requirements and operates as a compliant single lane Endpoint. The integrated Endpoint block interfaces to the GTP transceivers for serialization/de-serialization, and to block RAMs for data buffering. Combined, these elements implement the physical layer, data link layer, and transaction layer of the protocol.

Xilinx provides a light-weight (<200 LUT), configurable, easy-to-use LogiCORE™ IP that ties the various building blocks (the integrated Endpoint block for PCI Express technology, the GTP transceivers, block RAM, and clocking resources) into a compliant Endpoint solution. The system designer has control over many configurable parameters: maximum payload size, reference clock frequency, and base address register decoding and filtering.

More information and documentation on solutions for PCI Express designs can be found at:

http://www.xilinx.com/technology/protocols/pciexpress.htm

Spartan-6 FPGA Ordering Information

Table 3 shows the speed and temperature grades available in the different Spartan-6 devices. Some devices might not be available in every speed and temperature grade.

Table 3: **Speed Grade and Temperature Ranges**

Device Family	Speed Grade and Temperature Range	
	Commercial (C) 0°C to +85°C	Industrial (I) –40°C to +100°C
Spartan-6 LX	-3, -3N, -2, -1L	-3, -3N, -2, -1L
Spartan-6 LXT	-3, -3N, -2	-3, -3N, -2

The Spartan-6 FPGA ordering information shown in Figure 1 applies to all packages, including Pb-Free. Refer to the Package Marking section of UG385, *Spartan-6 FPGA Packaging and Pinouts* for a more detailed explanation of the device markings.

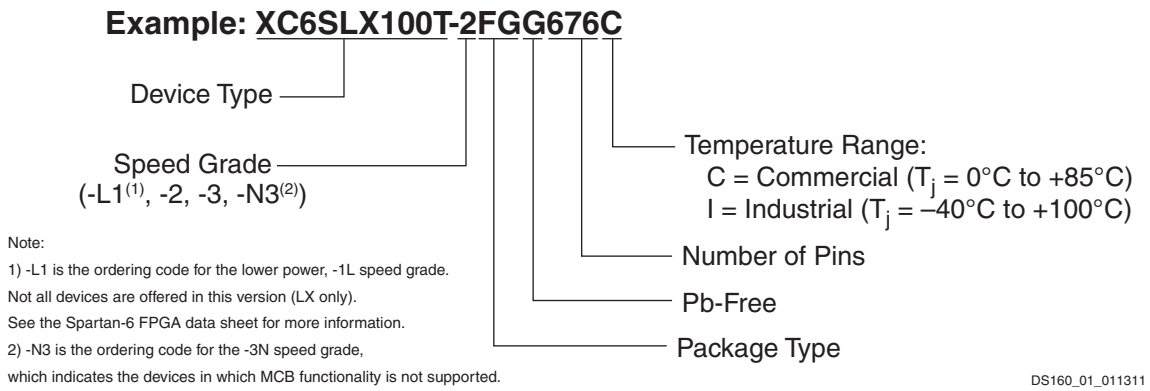

Figure 1: **Spartan-6 FPGA Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/02/09	1.0	Initial Xilinx release.
05/05/09	1.1	Updated and simplified Designed for low cost, Multi-voltage, multi-standard SelectIO™ interface banks, and Integrated Memory Controller blocks sections on page 1. Clarified PCI support on page 1is only for the 33 MHz specification. Revised number of logic cells, slices, and maximum user I/O, and added number of flip-flops to Table 1. In Table 2, revised user I/O counts, removed the XC6SLX25 in the CSG225 package and the XC6SLX45T in the FGG676 package, added XC6SLX9 in the FT(G)256 package and XC6SLX45 in the CSG324 package, and added notes. Clerical edits to the following sections: Dynamic Reconfiguration Port, Readback, CLBs, Slices, and LUTs, Frequency Synthesis, PLL, Programmable Data Width, and Memory Controller Block. Clarified I/O pin range, V_{REF} banks, and electrical characteristics in the Input/Output section.
06/24/09	1.2	Updated device/package combinations in Table 1 and Table 2 including adding the XC6SLX75 and XC6SLX75T devices. Added ordering information and FPGA documentation sections. Removed partial reconfiguration discussion from the Readback section.
11/05/09	1.3	Updated Figure 1, page 9 to show -4 speed grade. Added 64-bit PCI support on page 1. Updated User I/O numbers in Table 1and Table 2. Clarifying edits to these sections: Configuration, Digital Signal Processing—DSP48A1 Slice, Input/Output, and PCI Express documentation.

Date	Version	Description of Revisions
03/03/10	1.4	Updated the slice counts for the LX25 and LX25T in Table 1. Revised the Dynamic Reconfiguration Port section. Added to the Spread-Spectrum Clocking section. Changed the PLL VCO maximum frequency to 1080 MHz and the DSP48A1 slice maximum frequency to 320 MHz due to the addition of the -4 speed specification. Clarified configurations in the Programmable Data Width section. Updated Low-Power Gigabit Transceiver operating rate.
08/02/10	1.5	Updated data transfer rate per differential I/O from 1,050 Mb/s to 1,080 Mb/s in Summary of Spartan-6 FPGA Features. Added the -3N speed grade to appropriate section throughout the document, including Figure 1. Updated category in Table 2 from Size to Body Size. Updated the Configuration section with SPI and BPI interface information. Removed the Dynamic Reconfiguration Port section. Updated the operating speed of the DSP48A1 slice multiplier and accumulator to 390 MHz in Digital Signal Processing—DSP48A1 Slice. Updated Input and Output Delay.
11/05/10	1.6	In Summary of Spartan-6 FPGA Features and in Low-Power Gigabit Transceiver, updated GTP serial transceiver data rate to 3.2 Gb/s. Updated the notes in Figure 1. Added DS170, *XA Spartan-6 Automotive FPGA Family Overview* to the Spartan-6 FPGA Documentation.
03/21/11	1.7	Updated from Advance to Preliminary Specification. Removed -4 speed grade from Summary of Spartan-6 FPGA Features and Figure 1 per XCN11008. Updated Integrated Endpoint Block for PCI Express Designs and Input and Output Delay.
10/25/11	2.0	Updated from Preliminary Specification to Production Specification. Updated Configuration, including the range of configuration bits to 3 Mb and 33 Mb, and Input and Output Delay. Updated Spartan-6 FPGA Ordering Information and added Table 3. Added Defense-Grade Spartan-6Q Family Overview (DS172) to list of documentation.

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