XC95144XL High Performance CPLD

DS056 (v2.0) April 3, 2007

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-CSP (117 user I/O pins)
  - Pb-free available for all packages
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS Fast FLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC95144 device in the 100-pin TQFP package

WARNING: Programming temperature range of T_A = 0° C to +70° C

Description

The XC95144XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 5 ns. See Figure 2 for overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$I_{CC}(mA) = MC_{HS}(0.175*PT_{HS} + 0.345) + MC_{LP}(0.052*PT_{LP} + 0.272) + 0.04 * MC_{TOG}(MC_{HS} + MC_{LP})* f$$

where:

MC_{HS} = # macrocells in high-speed configuration

PT_{HS} = average number of high-speed product terms per macrocell

MC_{LP} = # macrocells in low power configuration

PT_{LP} = average number of low power product terms per macrocell

f = maximum clock frequency

MCTOG = average % of flip-flops toggling per clock (~12%)

This calculation was derived from laboratory measurements of an XC9500XL part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx

application note **XAPP114, "Understanding XC9500XL CPLD Power."**

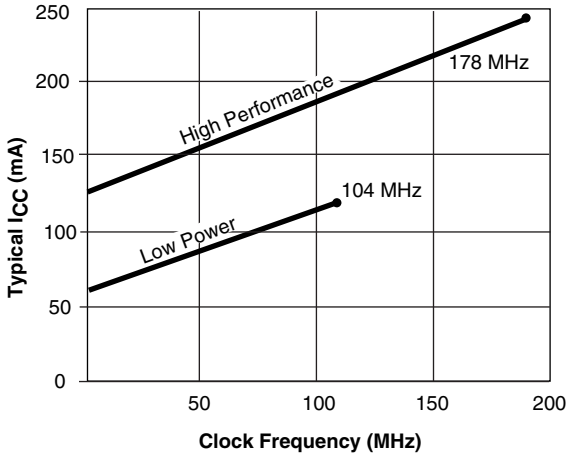


Figure 1: **Typical I_{CC} vs. Frequency for XC95144XL**

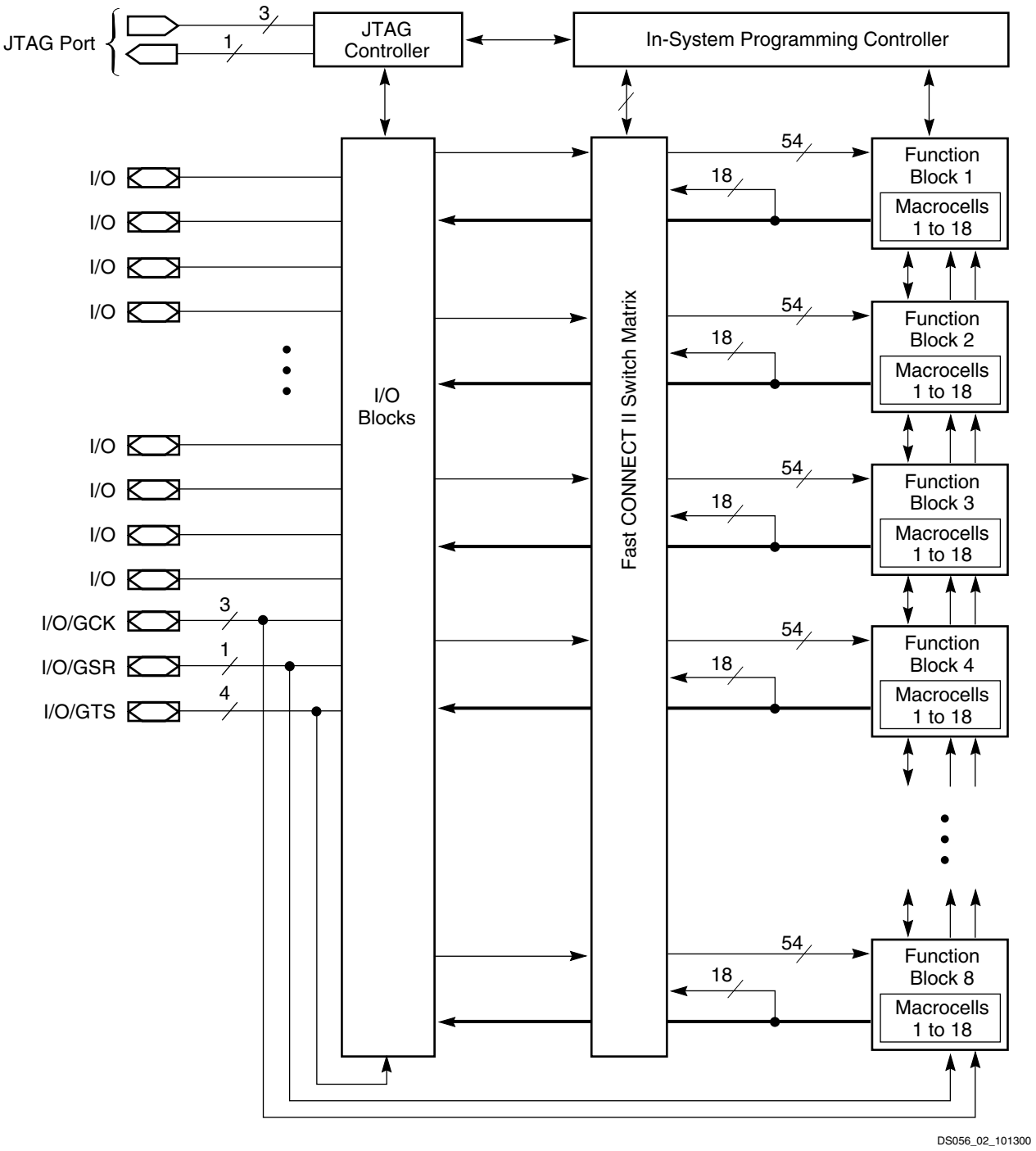


Figure 2: **XC95144XL Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings(2)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)(3)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. External I/O voltage may not exceed V_{CCINT} by 4.0V.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

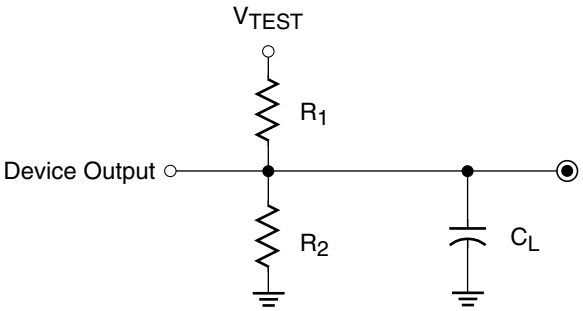
DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{CCIO} = Max; V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} Min < V_{IN} < 5.5V	-	±50	µA
C_{IN}	I/O capacitance	V_{IN} = GND; f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_{IN} = GND, No load; f = 1.0 MHz	45 (Typical)		mA

AC Characteristics

Symbol	Parameter	XC95144XL-5		XC95144XL-7		XC95144XL-10		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	7.5	-	10.0	ns
T_{SU}	I/O setup time before GCK	3.7	-	4.8	-	6.5	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.5	-	4.5	-	5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	178.6	-	125.0	-	100.0	MHz
T_{PSU}	I/O setup time before p-term clock input	1.7	-	1.6	-	2.1	-	ns
T_{PH}	I/O hold time after p-term clock input	2.0	-	3.2	-	4.4	-	ns
T_{PCO}	P-term clock output valid	-	5.5	-	7.7	-	10.2	ns
T_{OE}	GTS to output valid	-	4.0	-	5.0	-	7.0	ns
T_{OD}	GTS to output disable	-	4.0	-	5.0	-	7.0	ns
T_{POE}	Product term OE to output enabled	-	7.0	-	9.5	-	11.0	ns
T_{POD}	Product term OE to output disabled	-	7.0	-	9.5	-	11.0	ns
T_{AO}	GSR to output valid	-	10.0	-	12.0	-	14.5	ns
T_{PAO}	P-term S/R to output valid	-	10.5	-	12.6	-	15.3	ns
T_{WLH}	GCK pulse width (High or Low)	2.8	-	4.0	-	4.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320 Ω	360 Ω	35 pF
	2.5V	2.5V	250 Ω	660 Ω	35 pF

DS058_03_081500

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC95144XL-5		XC95144XL-7		XC95144XL-10		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.5	-	2.3	-	3.5	ns
T_{GCK}	GCK buffer delay	-	1.1	-	1.5	-	1.8	ns
T_{GSR}	GSR buffer delay	-	2.0	-	3.1	-	4.5	ns
T_{GTS}	GTS buffer delay	-	4.0	-	5.0	-	7.0	ns
T_{OUT}	Output buffer delay	-	2.0	-	2.5	-	3.0	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	1.6	-	2.4	-	2.7	ns
T_{PTSR}	Product term set/reset delay	-	1.0	-	1.4	-	1.8	ns
T_{PTTS}	Product term 3-state delay	-	5.5	-	7.2	-	7.5	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.5	-	1.3	-	1.7	ns
T_{SUI}	Register setup time	2.3	-	2.6	-	3.0	-	ns
T_{HI}	Register hold time	1.4	-	2.2	-	3.5	-	ns
T_{ECSU}	Register clock enable setup time	2.3	-	2.6	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	1.4	-	2.2	-	3.5	-	ns
T_{COI}	Register clock to output valid time	-	0.4	-	0.5	-	1.0	ns
T_{AOI}	Register async. S/R to output delay	-	6.0	-	6.4	-	7.0	ns
T_{RAI}	Register async. S/R recover before clock	5.0		7.5		10.0		ns
T_{LOGI}	Internal logic delay	-	1.0	-	1.4	-	1.8	ns
T_{LOGILP}	Internal low power logic delay	-	5.0	-	6.4	-	7.3	ns
Feedback Delays								
T_F	Fast CONNECT II feedback delay	-	1.9	-	3.5	-	4.2	ns
Time Adders								
T_{PTA}	Incremental product term allocator delay	-	0.7	-	0.8	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	3.0	-	4.0	-	4.5	ns

XC95144XL I/O Pins(2)

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order
1	1	-	23	H3	429	3	1	-	39	M3	321
1	2	11	16	F1	426	3	2(1)	23(1)	32(1)	L1(1)	318
1	3	12	17	G2	423	3	3	-	41	K4	315
1	4	-	25	J1	420	3	4	-	44	N4	312
1	5	13	19	G3	417	3	5	24	33	L2	309
1	6	14	20	G4	414	3	6	25	34	L3	306
1	7	-	-	-	411	3	7	-	46	L5	303
1	8	15	21	H1	408	3	8(1)	27(1)	38(1)	N2(1)	300
1	9	16	22	H2	405	3	9	28	40	N3	297
1	10	-	31	K3	402	3	10	-	48	N5	294
1	11	17	24	H4	399	3	11	29	43	M4	291
1	12	18	26	J2	396	3	12	30	45	K5	288
1	13	-	-	-	393	3	13	-	-	-	285
1	14	19	27	J3	390	3	14	32	49	K6	282
1	15	20	28	J4	387	3	15	33	50	L6	279
1	16	-	35	M1	384	3	16	-	-	-	276
1	17(1)	22(1)	30(1)	K2(1)	381	3	17	34	51	M6	273
1	18	-	-	-	378	3	18	-	-	-	270
2	1	-	142	C3	375	4	1	-	118	C9	267
2	2(1)	99(1)	143(1)	A2(1)	372	4	2	87	126	A7	264
2	3	-	-	-	369	4	3	-	133	A5	261
2	4	-	4	C1	366	4	4	-	-	-	258
2	5(1)	1(1)	2(1)	B1(1)	363	4	5	89	128	D7	255
2	6(1)	2(1)	3(1)	C2(1)	360	4	6	90	129	A6	252
2	7	-	-	-	357	4	7	-	-	-	249
2	8(1)	3(1)	5(1)	D4(1)	354	4	8	91	130	B6	246
2	9(1)	4(1)	6(1)	D3(1)	351	4	9	92	131	C6	243
2	10	-	7	D2	348	4	10	-	135	C5	240
2	11	6	9	E4	345	4	11	93	132	D6	237
2	12	7	10	E3	342	4	12	94	134	B5	234
2	13	-	12	E1	339	4	13	-	137	A4	231
2	14	8	11	E2	336	4	14	95	136	D5	228
2	15	9	13	F4	333	4	15	96	138	B4	225
2	16	-	14	F3	330	4	16	-	139	C4	222
2	17	10	15	F2	327	4	17	97	140	A3	219
2	18	-	-	-	324	4	18	-	-	-	216

Notes:
1. Global control pin.
2. The pin-outs are the same for Pb-free versions of packages.

XC95144XL (Continued)

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order
5	1	-	-	-	213
5	2	35	52	N6	210
5	3	-	59	L8	207
5	4	-	-	-	204
5	5	36	53	M7	201
5	6	37	54	N7	198
5	7	-	66	M10	195
5	8	39	56	K7	192
5	9	40	57	N8	189
5	10	–-	68	N11	186
5	11	41	58	M8	183
5	12	42	60	K8	180
5	13	-	70	L11	177
5	14	43	61	N9	174
5	15	46	64	K9	171
5	16	-	-	-	168
5	17	49	69	M11	165
5	18	-	-	-	162
6	1	-	-	-	159
6	2	74	106	C11	156
6	3	-	-	-	153
6	4	-	111	B11	150
6	5	76	110	A12	147
6	6	77	112	A11	144
6	7	-	-	-	141
6	8	78	113	D10	138
6	9	79	116	A10	135
6	10	-	115	B10	132
6	11	80	119	B9	129
6	12	81	120	A9	126
6	13	-	-	-	123
6	14	82	121	D8	120
6	15	85	124	A8	117
6	16	-	117	D9	114
6	17	86	125	B7	111
6	18	-	-	-	108
7	1	-	-	-	105
7	2	50	71	N12	102
7	3	-	75	L12	99
7	4	-	-	-	96
7	5	52	74	M13	93
7	6	53	76	L13	90
7	7	-	77	K10	87
7	8	54	78	K11	84
7	9	55	80	K13	81
7	10	-	79	K12	78
7	11	56	82	J11	75
7	12	58	85	H10	72
7	13	-	81	J10	69
7	14	59	86	H11	66
7	15	60	87	H12	63
7	16	-	83	J12	60
7	17	61	88	H13	57
7	18	-	-	-	54
8	1	-	-	-	51
8	2	63	91	G11	48
8	3	-	95	F11	45
8	4	-	97	E13	42
8	5	64	92	G10	39
8	6	65	93	F13	36
8	7	-	-	-	33
8	8	66	94	F12	30
8	9	67	96	F10	27
8	10	-	101	D13	24
8	11	68	98	E12	21
8	12	70	100	E10	18
8	13	-	103	D11	15
8	14	71	102	D12	12
8	15	72	104	C13	9
8	16	-	107	B13	6
8	17	73	105	C12	3
8	18	-	-	-	0

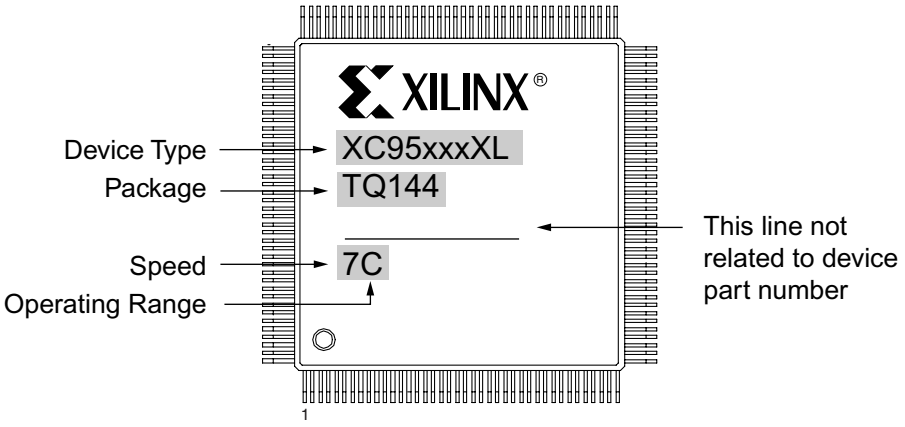
Notes:
1. The pin-outs are the same for Pb-free versions of packages.

XC95144XL Global, JTAG and Power Pins(1)

Pin Type	TQ100	TQ144	CS144
I/O/GCK1	22	30	K2
I/O/GCK2	23	32	L1
I/O/GCK3	27	38	N2
I/O/GTS1	3	5	D4
I/O/GTS2	4	6	D3
I/O/GTS3	1	2	B1
I/O/GTS4	2	3	C2
I/O/GSR	99	143	A2
TCK	48	67	L10
TDI	45	63	L9
TDO	83	122	C8
TMS	47	65	N10
V_{CCINT} 3.3V	5, 57, 98	8, 42, 84, 141	B3, D1, J13, L4
V_{CCIO} 2.5V/3.3V	26, 38, 51, 88	1, 37, 55, 73, 109, 127	A1, A13, C7, L7, N1, N13
GND	21, 31, 44, 62, 69, 75, 84, 100	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	B2, B8, B12, C10, E11, G1, G12, G13, K1, M2, M5, M9, M12
No Connects	-	–	–

Notes:
1. The pin-outs are the same for Pb-free versions of packages.

Device Part Marking and Ordering Combination Information.

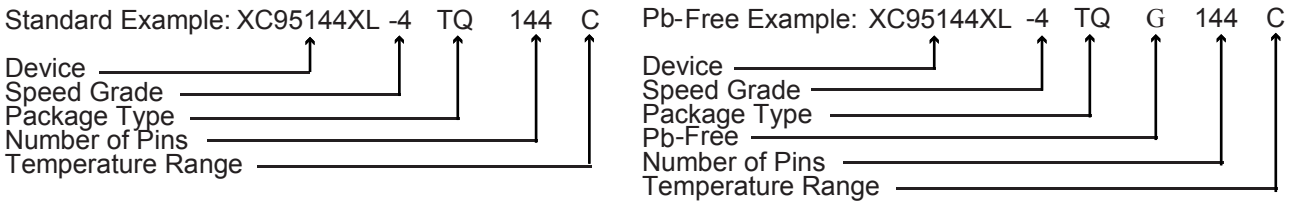


Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC95144XL-5TQ100C	5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-5TQ144C	5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-5CS144C	5 ns	CS144	144-ball	Chip Scale Package (CSP)	C
XC95144XL-7TQ100C	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-7TQ144C	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-7CS144C	7.5 ns	CS144	144-ball	Chip Scale Package (CSP)	C
XC95144XL-7TQ100I	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XL-7TQ144I	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XL-7CS144I	7.5 ns	CS144	144-ball	Chip Scale Package (CSP)	I
XC95144XL-10TQ100C	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-10TQ144C	10 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XL-10CS144C	10 ns	CS144	144-ball	Chip Scale Package (CSP)	C
XC95144XL-10TQ100I	10 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XL-10TQ144I	10 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XL-10CS144I	10 ns	CS144	144-ball	Chip Scale Package (CSP)	I
XC95144XL-5TQG100C	5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-5TQG144C	5 ns	TQG144	144-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-5CSG144C	5 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	C
XC95144XL-7TQG100C	7.5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-7TQG144C	7.5 ns	TQG144	144-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-7CSG144C	7.5 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	C
XC95144XL-7TQG100I	7.5 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	I
XC95144XL-7TQG144I	7.5 ns	TQG144	144-pin	Thin Quad Flat Pack (TQFP); Pb-free	I
XC95144XL-7CSG144I	7.5 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	I

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC95144XL-10TQG100C	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-10TQG144C	10 ns	TQG144	144-pin	Thin Quad Flat Pack (TQFP); Pb-free	C
XC95144XL-10CSG144C	10 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	C
XC95144XL-10TQG100I	10 ns	TQG100	100-pin	Thin Quad Flat Pack (TQFP); Pb-free	I
XC95144XL-10TQG144I	10 ns	TQG144	144-pin	Thin Quad Flat Pack (TQFP); Pb-free	I
XC95144XL-10CSG144I	10 ns	CSG144	144-ball	Chip Scale Package (CSP); Pb-free	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C



Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Further Reading

The following Xilinx links go to relevant XC9500XL CPLD documentation, including XAPP111, Using the XC9500XL Timing Model, and XAPP784, Bulletproof CPLD Design Practices. Simply click on the link and scroll down.

Data Sheets, Application Notes, and White Papers.

Packaging