XL1000-BD

Low Noise Amplifier
20 - 40 GHz

Rev. V2

Features

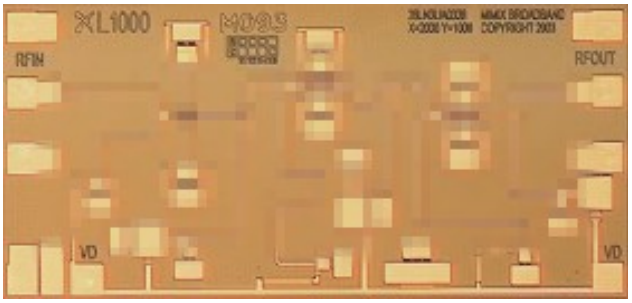
- Self Bias Architecture
- Small Size
- 3 or 5 V Operation
- 20 dB Small Signal Gain
- 2 dB Noise Figure
- 9 dBm P1dB Compression Point
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

The XL1000-BD is a 3-stage 20 - 40 GHz GaAs MMIC low noise amplifier that has a small signal gain of 20 dB with a noise figure of 2 dB across the band. This MMIC uses a GaAs pHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process.

This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Ordering Information

Part Number	Package
XL1000-BD-000V	"V" - vacuum release gel paks

Electrical Specifications: Freq. = 20 - 40 GHz, V_D = 5 V, I_D = 50 mA, T_A = +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Input Return Loss	22 - 36 GHz	dB	6	12	—
Output Return Loss	22 - 36 GHz	dB	4	10	—
Small Signal Gain	—	dB	12	20	—
Gain Flatness	—	dB	—	+/-4	—
Reverse Isolation	—	dB	30	45	—
Noise Figure	24 - 40 GHz	dB	—	2	3
Output Power for 1dB Compression Point	5 V	dBm	—	9	—
Output Third Order Intercept Point	5 V	dBm	—	16	—
Drain Bias Voltage	—	VDC	—	3	5
Supply Current	V_D = 3 V or 5 V	mA	—	35	50

Absolute Maximum Ratings

Parameter	Absolute Maximum
Supply Voltage	7 V_{DC}
Supply Current	70 mA
Input Power	12 dBm
Storage Temperature	-65°C to +165°C
Operating Temperature	-55°C to +85°C
Channel Temperature	+175°C

1. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

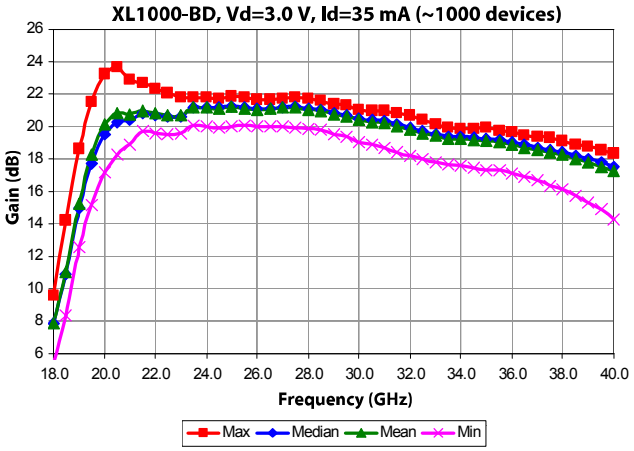
Handling Procedures

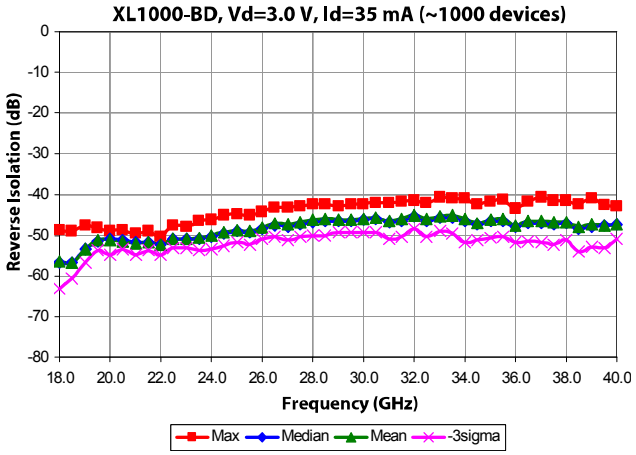
Please observe the following precautions to avoid damage:

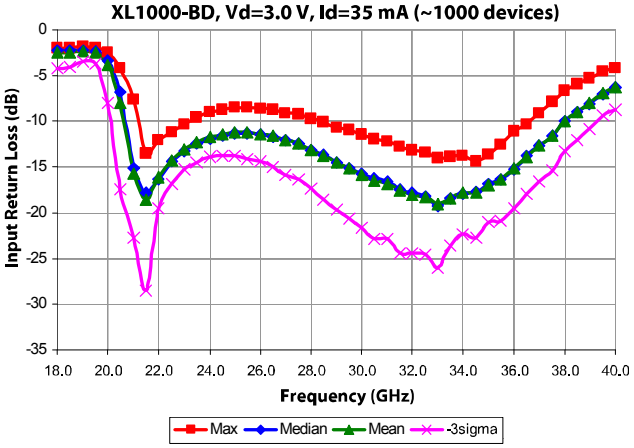
Static Sensitivity

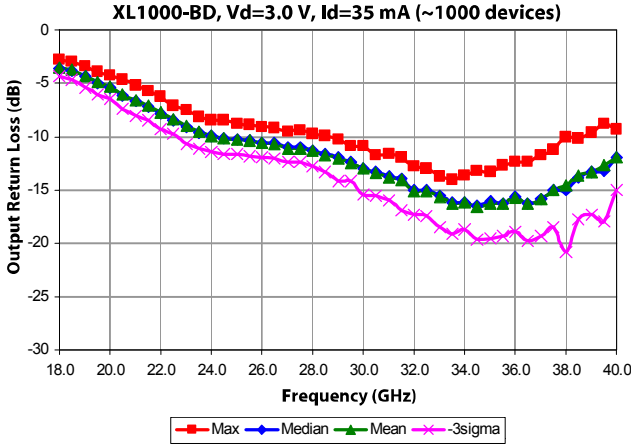
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

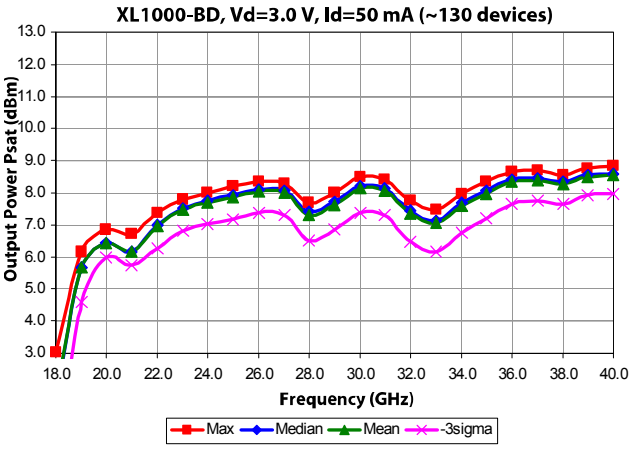
Typical Performance Curves (On-Wafer[1])

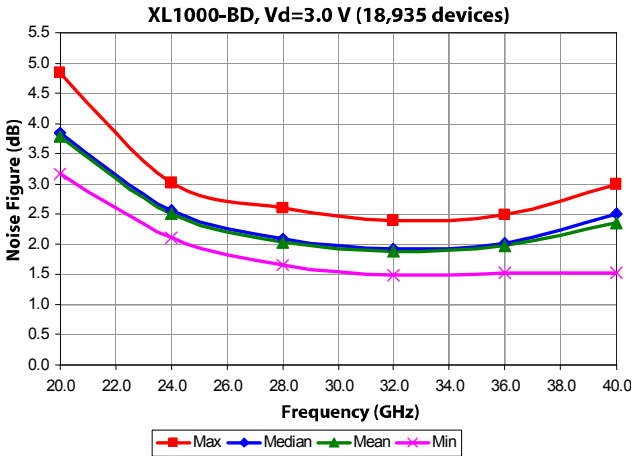






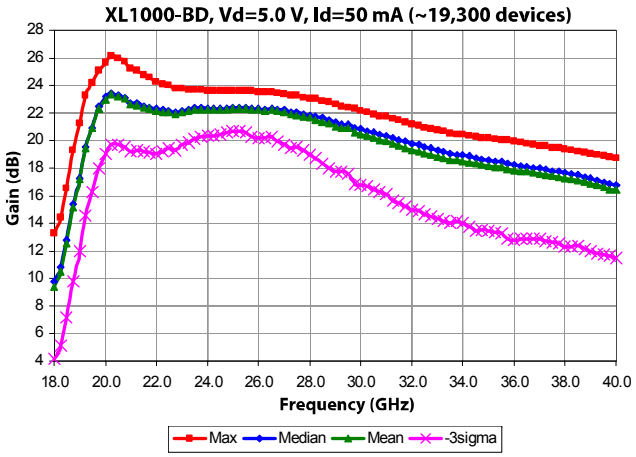


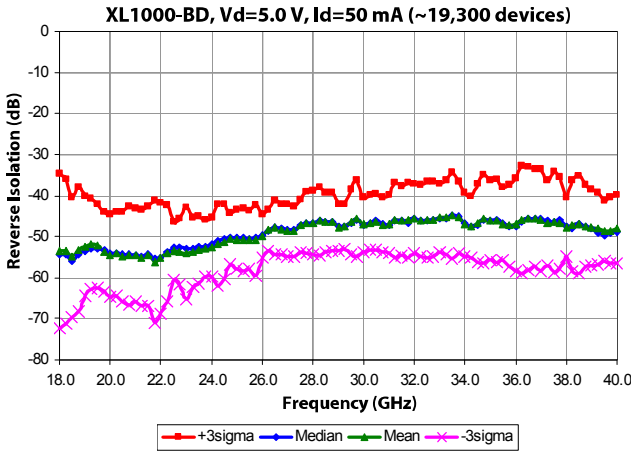


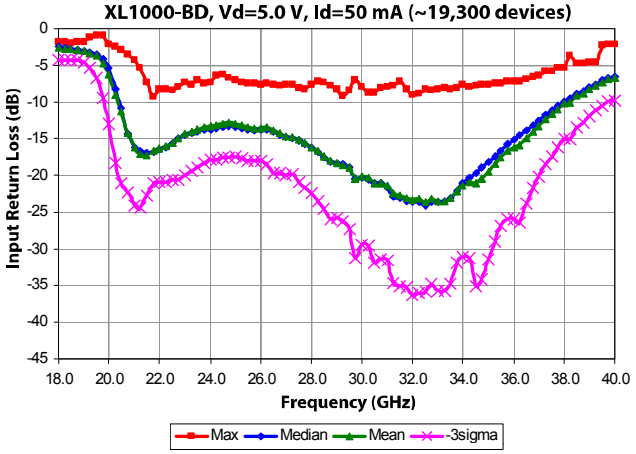


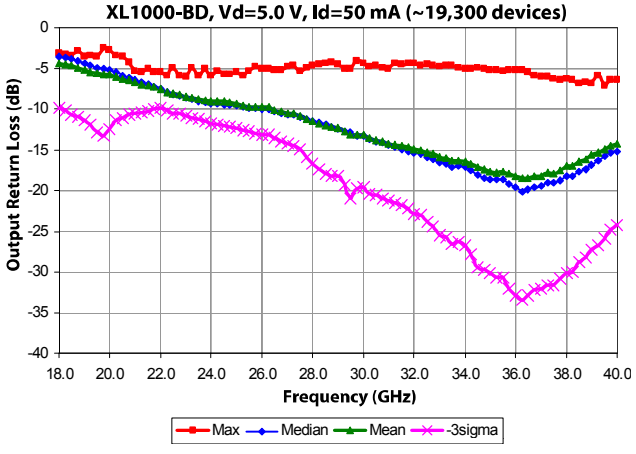
Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM-Tech T-pad transition is recommended. For additional information see the M/A-COM-Tech "T-Pad Transition" application note.

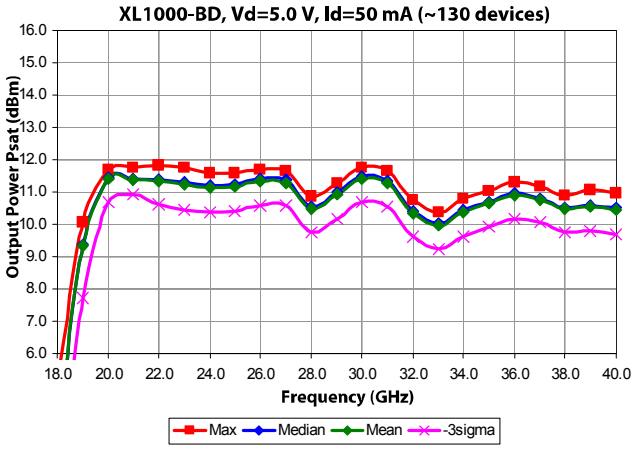
Typical Performance Curves (On-Wafer[1]) (cont.)

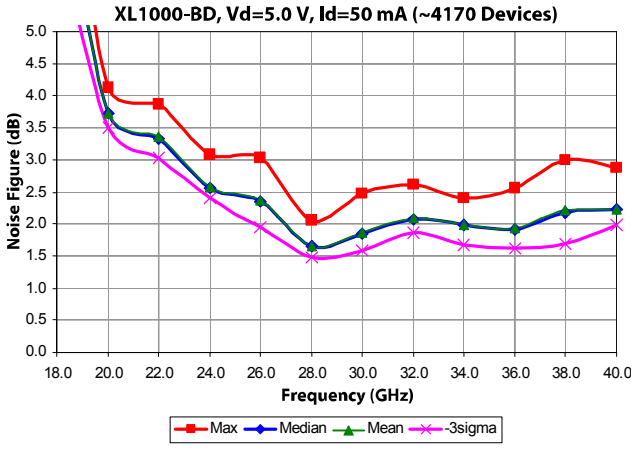












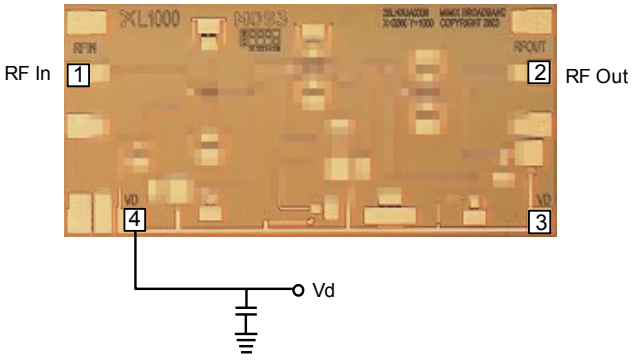
Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM-Tech T-pad transition is recommended. For additional information see the M/A-COM-Tech "T-Pad Transition" application note.

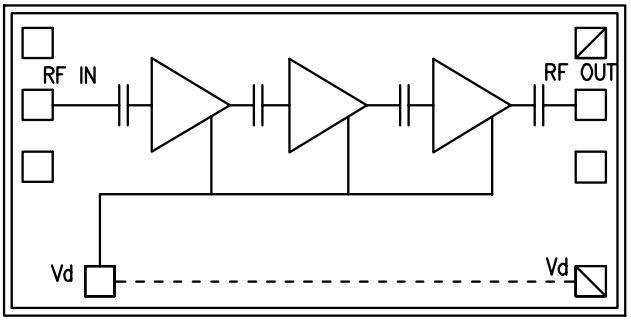
S-Parameters (On-Wafer[1]): V_D = 5 V, I_D = 52 mA

frequency (GHz)	S11 (mag.)	S11 (ang.)	S21 (mag.)	S21 (ang.)	S12 (mag.)	S12 (ang.)	S22 (mag.)	S22 (ang.)
18	0.746	-165.97	2.544	24.56	0.0017	168.35	0.684	-124.58
19	0.660	149.17	6.840	-14.35	0.0024	126.40	0.625	-138.66
20	0.142	2.00	14.715	-120.61	0.0021	52.59	0.534	-163.12
21	0.100	-163.20	13.152	-170.24	0.0018	12.19	0.474	176.63
22	0.140	129.51	12.237	154.80	0.0017	-16.42	0.395	152.50
23	0.170	86.23	11.946	125.13	0.0017	-49.65	0.337	128.14
24	0.200	42.30	12.003	84.11	0.0028	-88.17	0.286	90.54
25	0.211	21.38	11.981	58.08	0.0024	-116.99	0.274	65.73
26	0.212	3.82	11.914	33.30	0.0029	-127.87	0.269	43.21
27	0.191	-16.13	11.573	-2.82	0.0034	-150.83	0.263	15.00
28	0.176	-25.82	11.181	-25.58	0.0038	-173.21	0.254	-0.75
29	0.159	-34.54	10.740	-47.03	0.0037	-176.89	0.243	-14.39
30	0.127	-47.28	9.961	-77.92	0.0036	151.73	0.217	-32.44
31	0.121	-53.64	9.490	-96.70	0.0037	138.19	0.206	-42.09
32	0.111	-64.48	9.060	-115.14	0.0043	118.88	0.190	-51.51
33	0.111	-89.94	8.472	-141.75	0.0035	109.21	0.170	-67.19
34	0.122	-110.67	8.150	-158.94	0.0021	95.25	0.160	-80.04
35	0.138	-130.72	7.851	-176.20	0.0029	104.56	0.147	-92.90
36	0.185	-155.73	7.420	158.47	0.0038	59.79	0.139	-111.00
37	0.237	-171.07	7.107	140.91	0.0030	68.81	0.136	-128.23
38	0.271	175.33	6.778	124.00	0.0036	40.92	0.137	-144.49
39	0.382	158.32	6.264	98.04	0.0013	10.28	0.149	-167.73
40	0.446	148.19	5.900	80.75	0.0028	-17.50	0.162	179.76
41	0.506	138.34	5.471	63.80	0.0023	-7.95	0.176	167.50
42	0.591	124.05	4.767	38.77	0.0021	7.75	0.197	153.19
43	0.633	115.88	4.314	22.90	0.0020	-8.93	0.210	143.72

Note [1] S-Parameters – On-Wafer S-Parameters have been taken using bias conditions as shown. Measurements are referenced 150 µm in from RF In/Out pad edge.

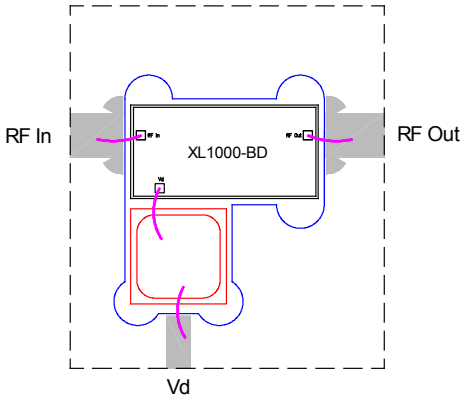
Bias Arrangement





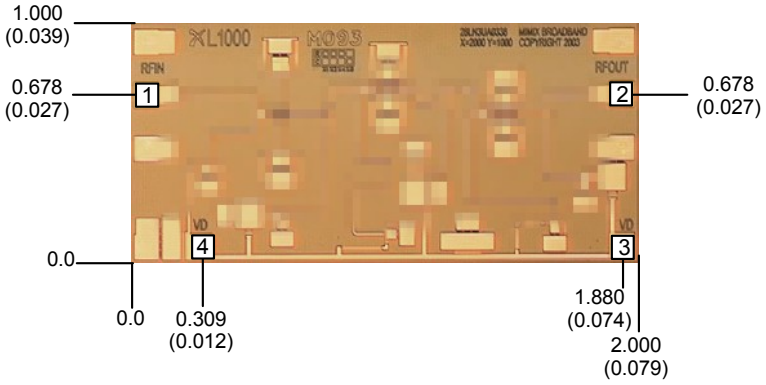
App Note [1]
Biasing - As shown in the bonding diagram, this device operates using a self-biased architecture and only requires one drain bias.
Bias is nominally:
V_D = 3 V, I_D = 35 mA or V_D = 5 V, I_D = 50 mA

App Note [2]
Bias Arrangement - Each DC pad (V_D) needs to have DC bypass capacitance (~100 - 200 pF) as close to the device as possible.
Additional DC bypass capacitance (~0.01 µF) is also recommended.



Bypass Capacitors

Mechanical Drawing



(Note: Engineering designator is 28LN3UA0338)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 1.239 mg.

Bond Pad #1 (RF In) Bond Pad #2 (RF Out) Bond Pad #3 (Vd) Bond Pad #4 (Vd)

MTTF Graphs

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at MACOM. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of device placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.