XL1002-BD

MACOM™

Low Noise Amplifier
20.0-36.0 GHz

Rev. V1

Features

- Balanced Design
- Excellent Input/Output Match
- Self-biased Architecture
- 23.0 dB Small Signal Gain
- 2.6 dB Noise Figure
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

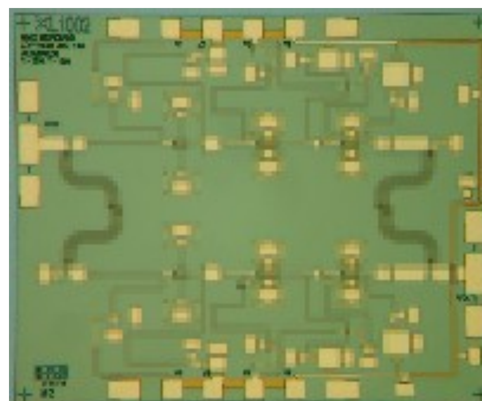
Description

M/A-COM Tech's three stage balanced 20.0-36.0 GHz GaAs MMIC low noise amplifier has a small signal gain of 23.0 dB with a noise figure of 2.6 dB across the band. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XL1002-BD-000V	"V" - vacuum release gel paks
XL1002-BD-EV1	evaluation module

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	120 mA
Input Power (Pin)	+15.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +85 °C
Channel Temperature (Tch)[1]	+175 °C

1. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

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Electrical Specifications: 20-36 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)[2]	dB	8.0	10.0	-
Output Return Loss (S22)[2]	dB	15.0	18.0	-
Small Signal Gain (S21)[2]	dB	18.0	23.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.5	-
Reverse Isolation (S12)[2]	dB	40.0	45.0	-
Noise Figure (NF)[2]	dB	-	2.6	4.0
Output Power for 1dB Compression Point (P1dB)	dBm	-	+4.0[1]	-
Output Third Order Intercept Point (OIP3)	dBm	-	+16.0[1]	-
Drain Bias Voltage (V5)	VDC	-	+5.0	+5.5
Supply Current (Id)	mA	-	85	95

1. See plots for additional information.
2. Unless otherwise indicated min/max over 20.0-36.0 GHz and biased at Vd=5 V, Id=85 mA.

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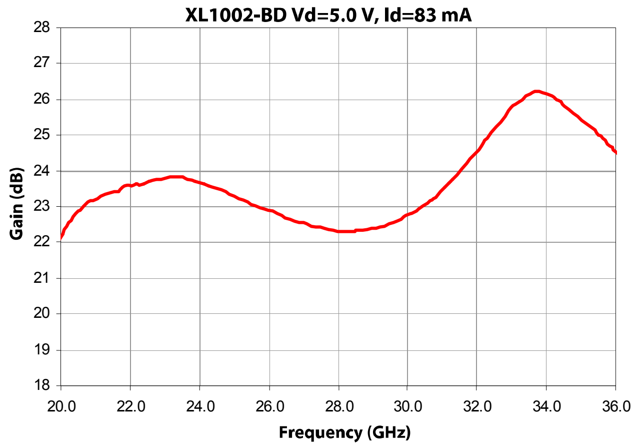
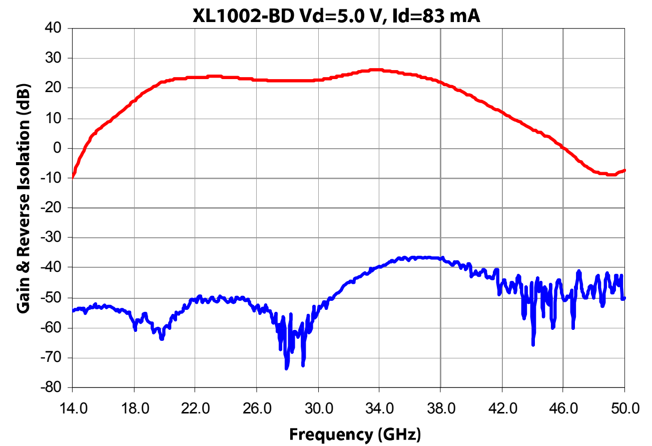
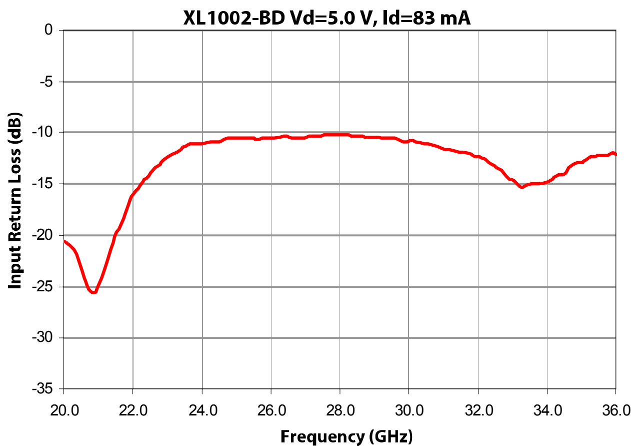
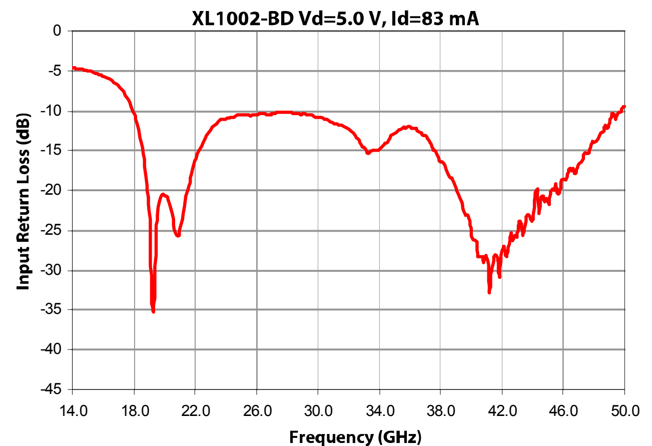
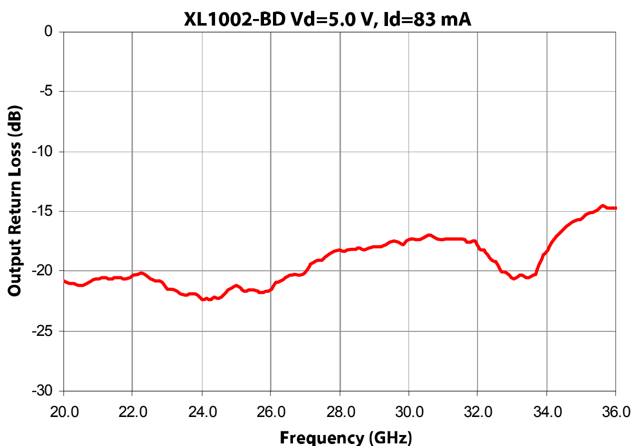
Typical Performance Curves (On-Wafer[1])

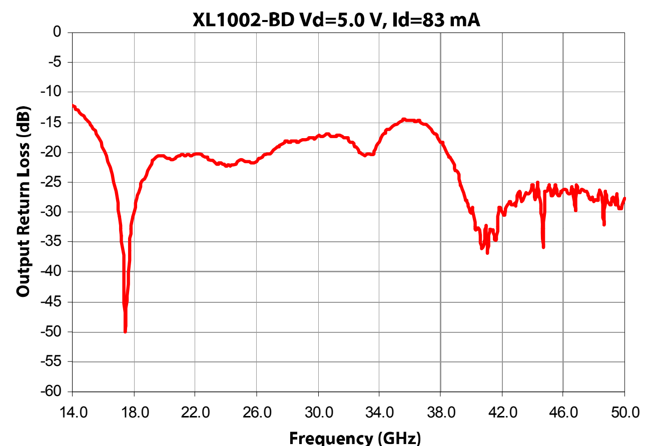












Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition is recommended. For additional information see the M/A-COM Tech “T-Pad Transition” application note.

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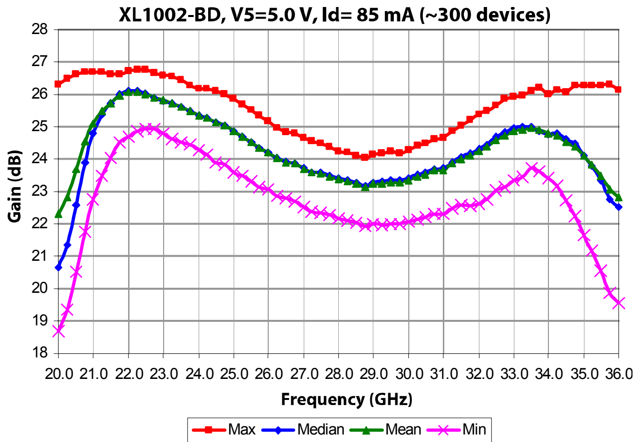

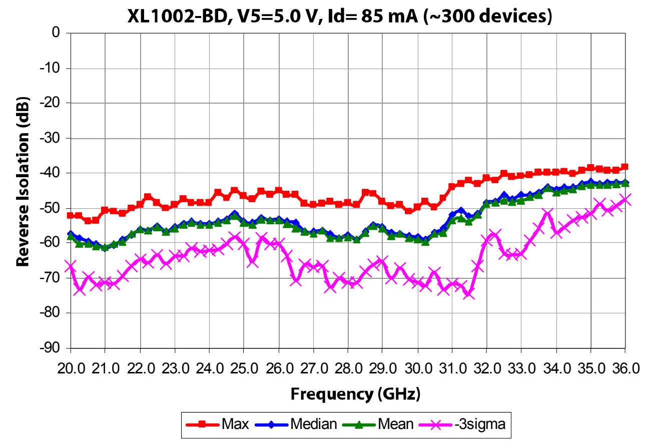

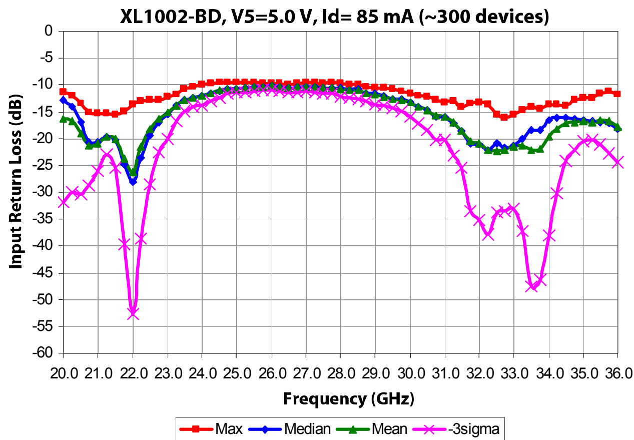

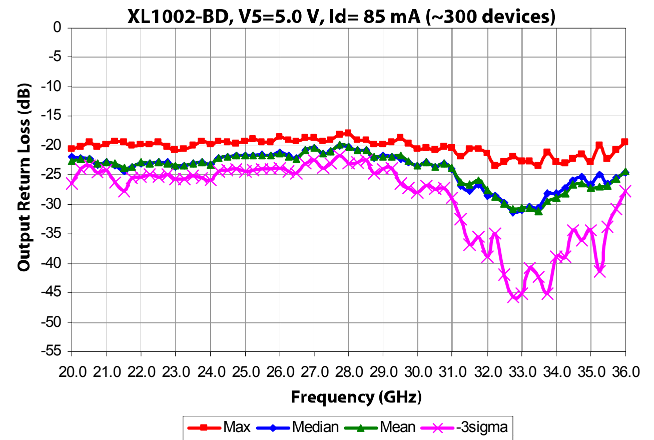

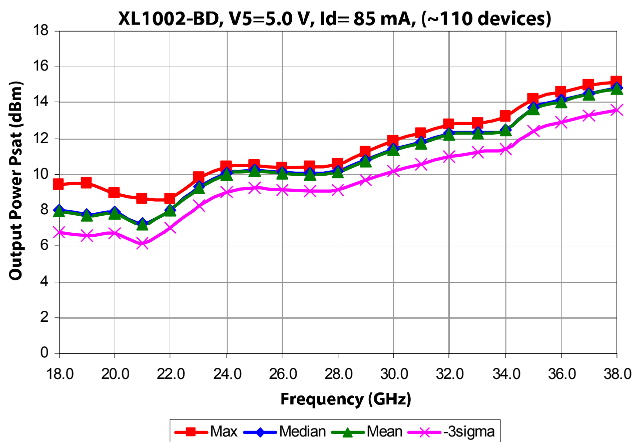

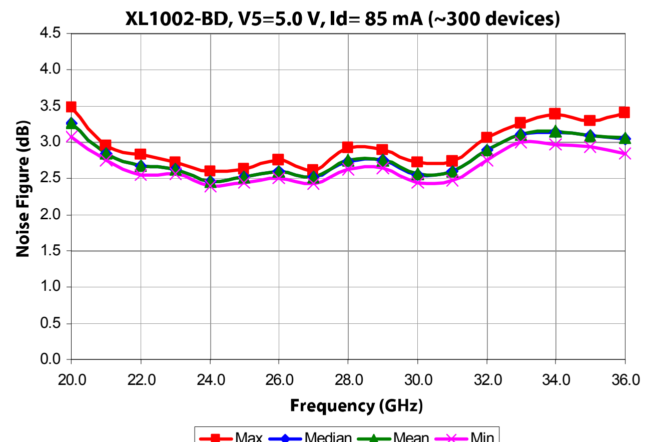

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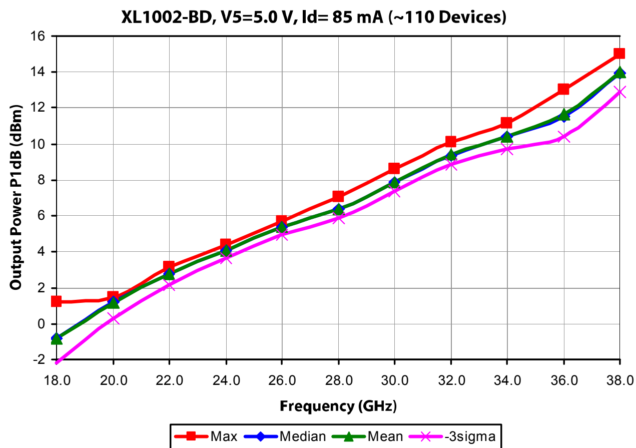

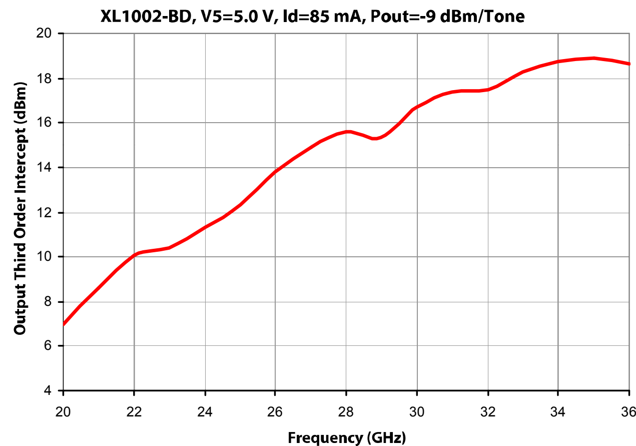

Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM-Tech T-pad transition is recommended. For additional information see the M/A-COM-Tech "T-Pad Transition" application note.

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S-Parameters (On-Wafer[1])

Typcial S-Parameter Data for XL1002-BD
Vd=5.0 V, Id=83 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
15.0	0.564	-178.06	1.188	-0.85	0.0020	147.49	0.184	68.29
16.0	0.525	163.99	2.314	-58.87	0.0022	133.71	0.112	49.27
17.0	0.456	140.66	3.626	-100.08	0.0020	112.54	0.038	32.34
18.0	0.316	109.41	5.986	-139.81	0.0013	85.19	0.029	178.18
19.0	0.056	59.74	9.885	168.14	0.0012	85.72	0.075	168.57
20.0	0.093	163.76	12.918	114.84	0.0010	144.44	0.090	146.46
21.0	0.058	-156.59	14.491	66.39	0.0018	140.58	0.093	144.99
22.0	0.160	-143.70	15.112	25.32	0.0029	125.69	0.096	140.86
23.0	0.242	-162.31	15.499	-11.89	0.0031	110.27	0.085	134.01
24.0	0.281	176.38	15.248	-47.77	0.0029	97.46	0.077	139.02
25.0	0.299	159.52	14.603	-80.38	0.0031	65.70	0.087	143.92
26.0	0.298	145.31	13.982	-109.27	0.0022	45.87	0.083	150.17
27.0	0.300	130.99	13.414	-136.06	0.0016	16.85	0.099	152.13
28.0	0.310	113.94	13.037	-161.27	0.0002	111.34	0.123	143.92
29.0	0.300	96.78	13.159	175.05	0.0011	-5.16	0.127	139.80
30.0	0.288	75.52	13.717	151.93	0.0017	-100.50	0.134	131.23
31.0	0.264	45.92	15.046	125.04	0.0033	-129.95	0.136	119.99
32.0	0.243	6.28	16.970	98.07	0.0058	-173.10	0.124	108.25
33.0	0.186	-58.03	19.555	65.63	0.0082	171.61	0.092	112.48
34.0	0.182	-153.97	20.286	27.29	0.0108	152.32	0.122	125.58
35.0	0.229	128.76	18.664	-8.42	0.0125	130.81	0.167	108.67
36.0	0.248	72.56	16.858	-42.32	0.0137	103.83	0.185	84.48
37.0	0.223	24.56	14.957	-75.99	0.0149	74.05	0.173	55.66
38.0	0.151	-13.76	12.471	-110.66	0.0138	60.14	0.120	31.74
39.0	0.103	-54.50	9.781	-143.05	0.0120	35.11	0.070	10.04
40.0	0.055	-103.89	7.306	-171.68	0.0073	5.53	0.031	15.51
41.0	0.039	-131.64	5.482	161.77	0.0072	16.95	0.024	65.20
42.0	0.039	165.29	3.987	137.96	0.0051	-9.93	0.033	89.31
43.0	0.051	138.97	2.903	116.93	0.0042	49.71	0.036	80.11
44.0	0.067	118.55	2.036	95.48	0.0005	-39.52	0.054	72.26
45.0	0.082	108.67	1.527	75.61	0.0024	47.48	0.054	59.12

Note [1] S-Parameters – On-Wafer S-Parameters have been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge.

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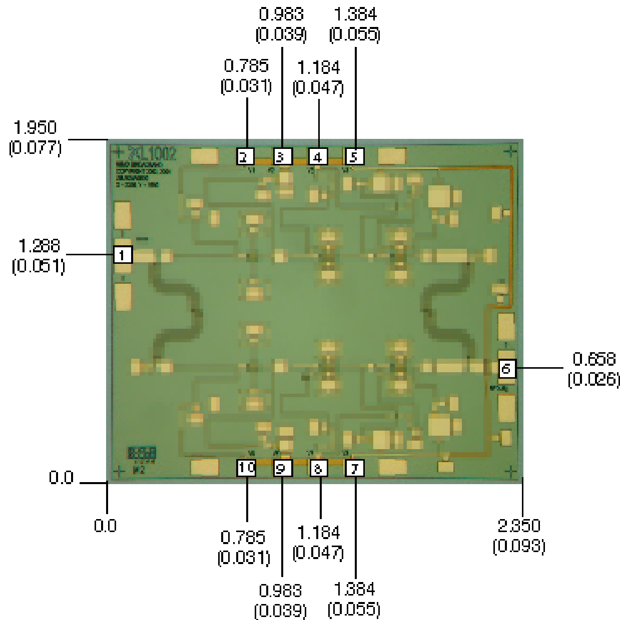
Mechanical Drawing

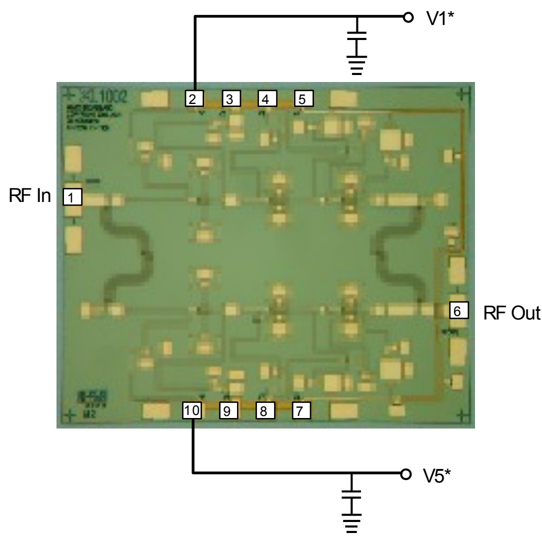


(Note: Engineering designator is 28LN3BA0050)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.115 +/- 0.010 (0.0045 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 2.838 mg.

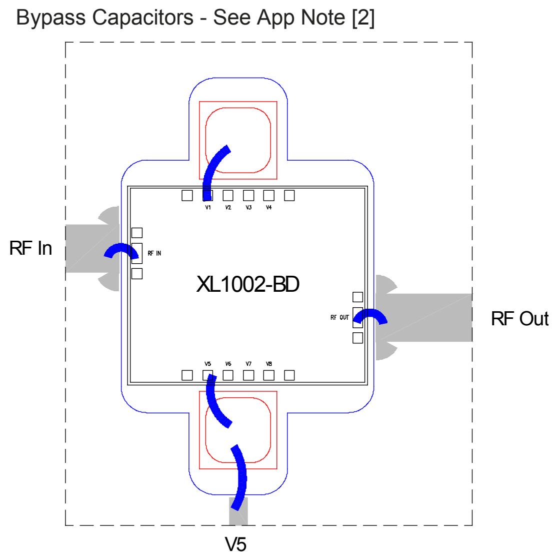
Bond Pad #1 (RF In)	Bond Pad #4 (V3)	Bond Pad #7 (V8)
Bond Pad #2 (V1)	Bond Pad #5 (V4)	Bond Pad #8 (V7)
Bond Pad #3 (V2)	Bond Pad #6 (RF Out)	Bond Pad #9 (V6)
		Bond Pad #10 (V5)

Bias Arrangement



*V1 or V5 may be used, but both are not required.

Bypass Capacitors - See App Note [2]



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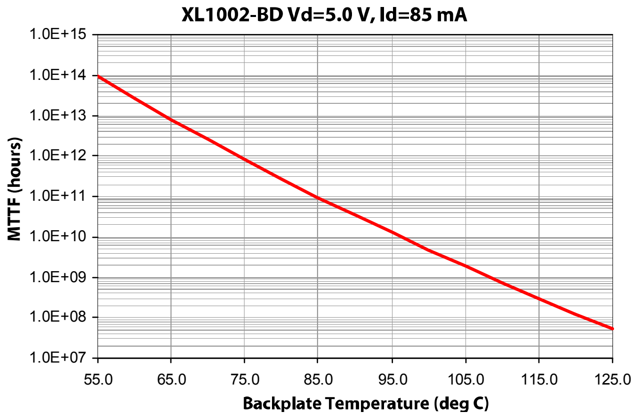
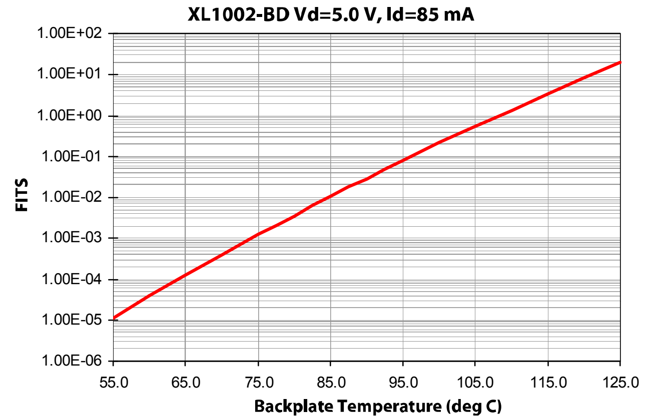
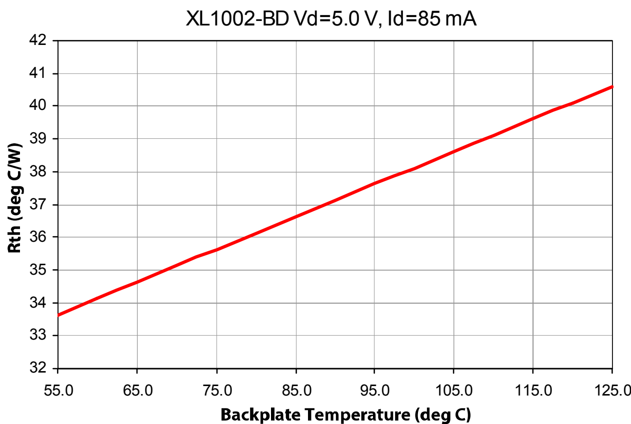
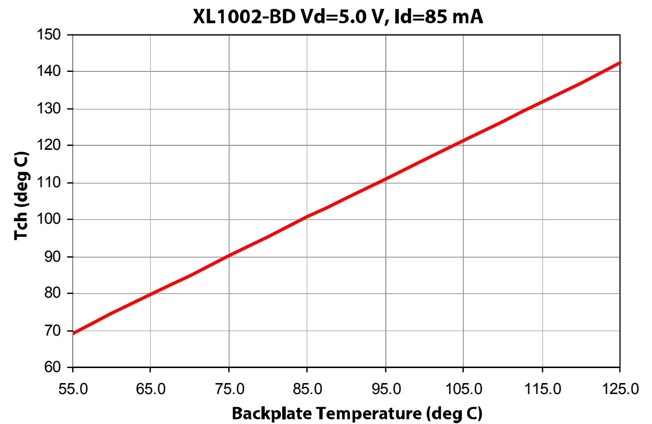
MTTF Graphs

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at M/A-COM Tech. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of device placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.









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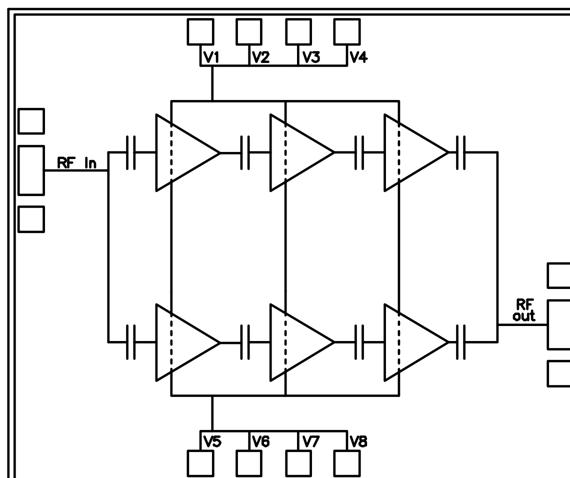
App Note [1] Biasing - As shown in the bonding diagram, this device operates using a self-biased architecture and only requires a single bias voltage. All DC pads (V1 through V8) are tied together on-chip, even though V1 or V5 are shown as main connections, any of the eight DC pads may be used to bias the device. Bias is nominally V1 or V5=5V, Id=85 mA.

App Note [2] Bias Arrangement - The DC pad at the top (V1) should be connected to one DC bypass capacitor (~100-200 pf) and the DC pad at the bottom (V5) should be connected using another DC bypass capacitor (~100-200 pf). Additional DC bypass capacitance (~0.01 pf) is also recommended. Capacitance should be as close to the device as possible.



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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

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