XP1026-BD

MACOM™

Power Amplifier
27.0-32.0 GHz

Rev. V1

Features

- Ka-Band 2W Power Amplifier
- 21.0 dB Small Signal Gain
- +33.0 dBm Saturated Output Power
- +40.0 dBm Output Third Order Intercept (OIP3)
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

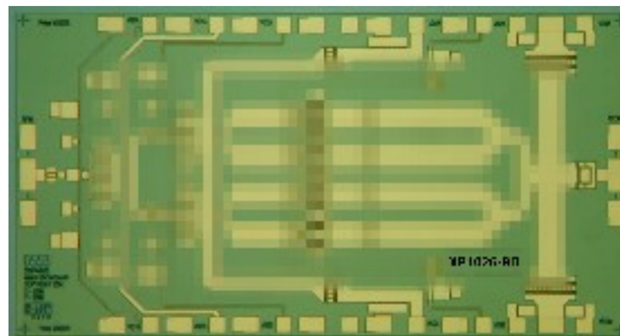
Description

M/A-COM Tech's three stage 27.0-32.0 GHz GaAs MMIC power amplifier has a small signal gain of 21.0 dB with +33 dBm saturated output power. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XP1026-BD-000V	"V" - vacuum release gel paks

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC[2]
Supply Current (Id1,2,3)	165,415,790 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (Pin)	+22 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +85 °C
Channel Temperature (Tch)[1]	175 °C

1. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
2. Under pulsed bias conditions, under CW Psat conditions further reduction in max supply voltage (~0.5V) is recommended.

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Electrical Specifications: 27-32 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	10.0	-
Output Return Loss (S22)	dB	-	15.0	-
Small Signal Gain (S21)[1]	dB	-	21.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.0	-
Reverse Isolation (S12)	dB	-	50.0	-
Output Power for 1 dB Compression (P1dB)	dBm	-	+32.0	-
Output Third Order Intercept Point (OIP3)	dBm	-	+40.0	-
Saturated Output Power (Psat)[1]	dBm	-	+33.0	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	+5.5	+5.8
Gate Bias Voltage (Vg1,2,3)	VDC	-1.2	-0.7	0.0
Supply Current (Id1) (Vd=5.5 V, Vg=-0.7 V Typical)	mA	-	100	150
Supply Current (Id2) (Vd=5.5 V, Vg=-0.7 V Typical)	mA	-	250	350
Supply Current (Id3) (Vd=5.5 V, Vg=-0.7 V Typical)	mA	-	550	750

1. Measured on wafer pulsed

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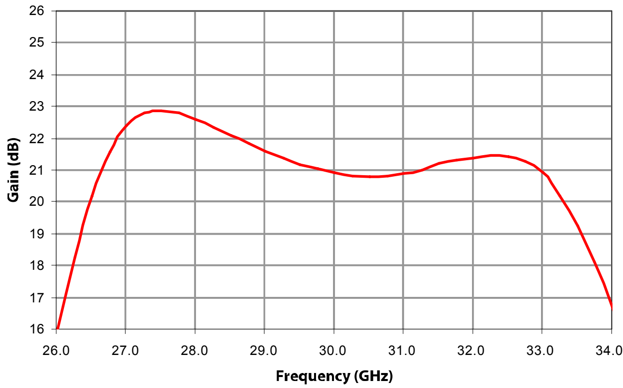
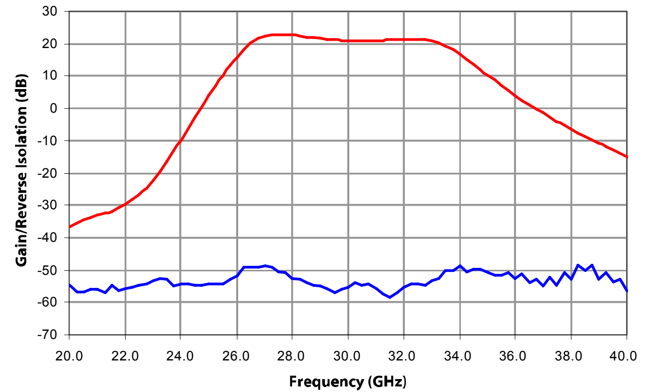
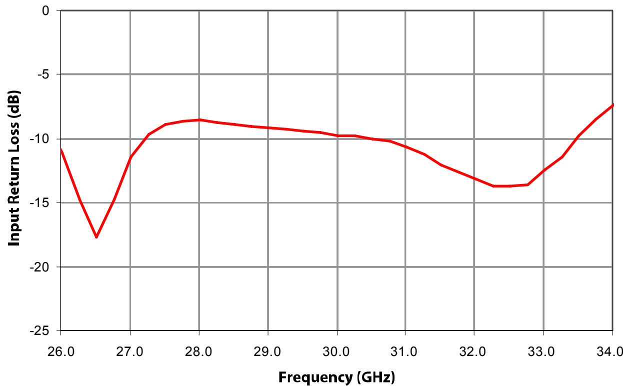
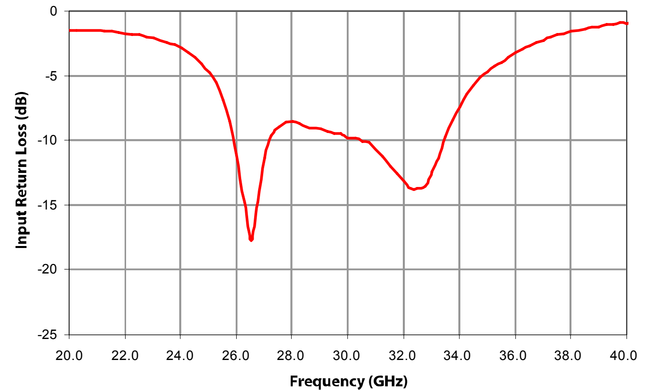
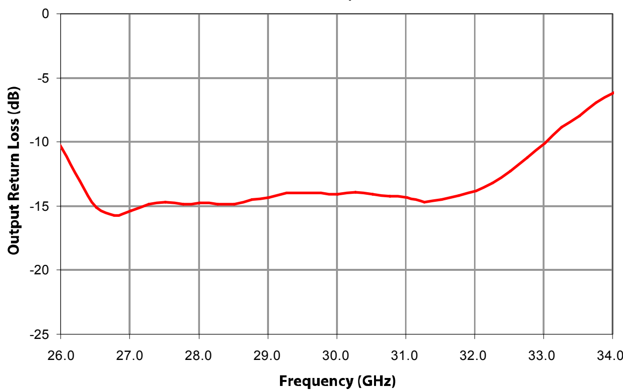
Typical Performance Curves (On-Wafer[1])

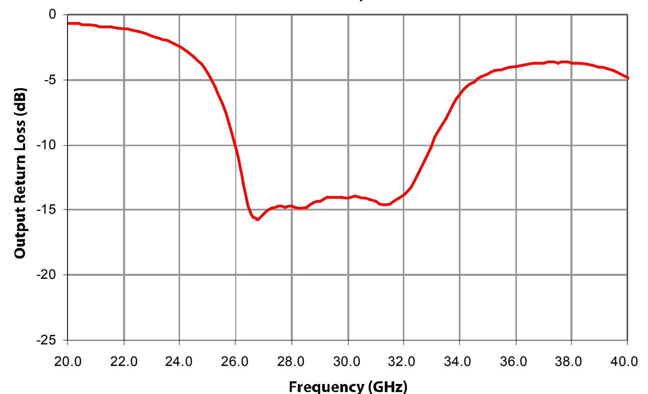












1. **Measurements –** On-Wafer S-Parameters have been taken using reduced bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition and tuned output matching network is recommended. For additional information see the M/A-COM Tech “T-Pad Transition” application note. Contact technical sales for output matching network information.

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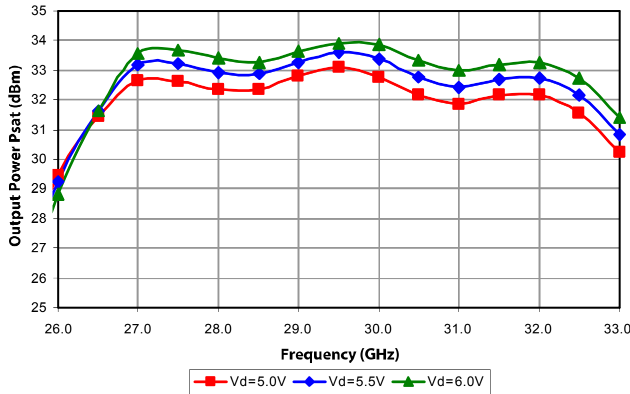
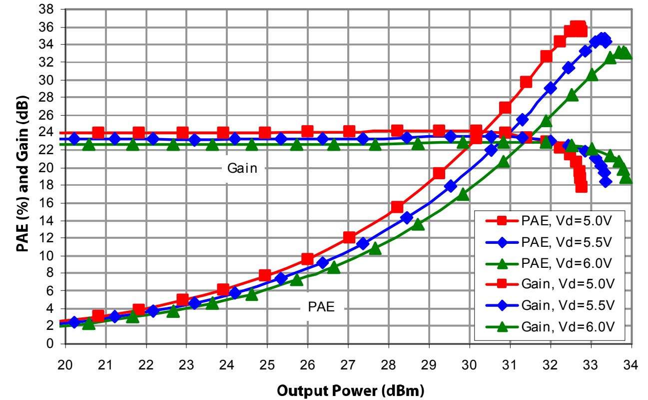
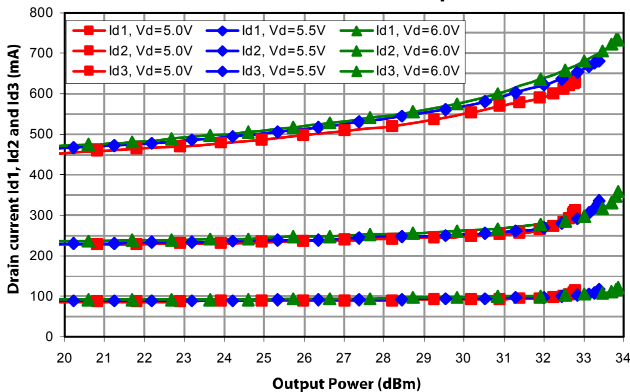
Typical Performance Curves (On-Wafer[1]) (cont.)







1. **Measurements –** On-Wafer Output Power data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition and tuned output matching network is recommended. For additional information see the M/A-COM Tech "T-Pad Transition" application note. Contact technical sales for output matching network information.

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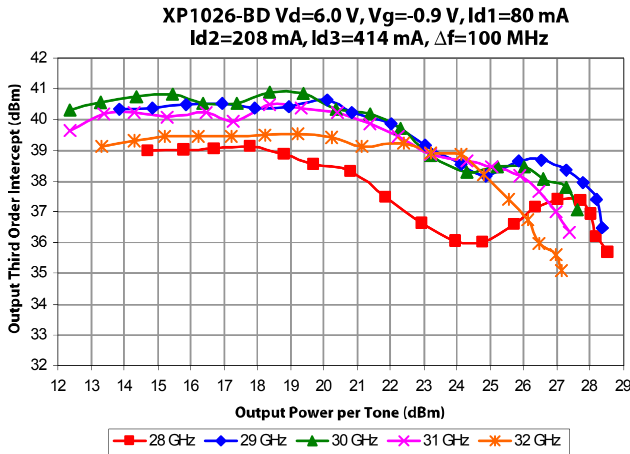

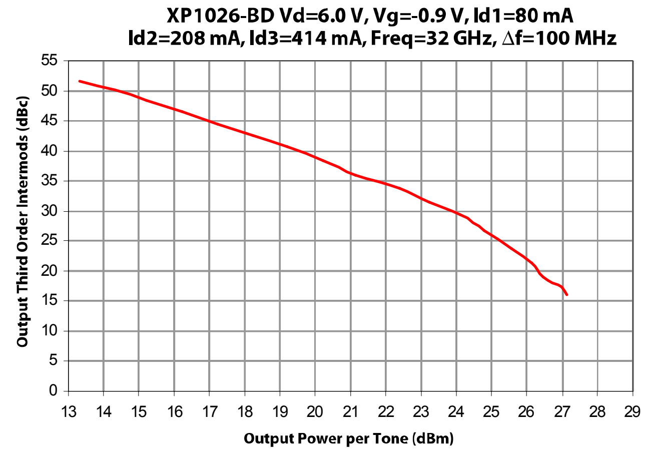

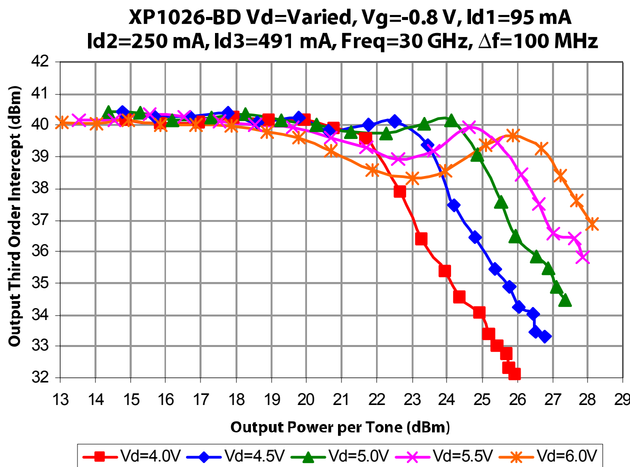

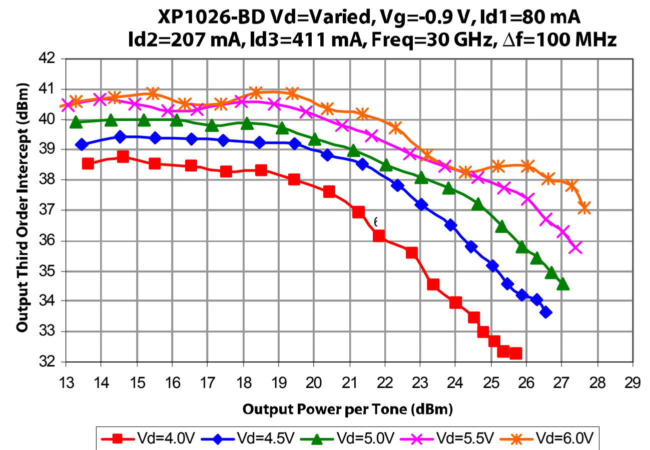

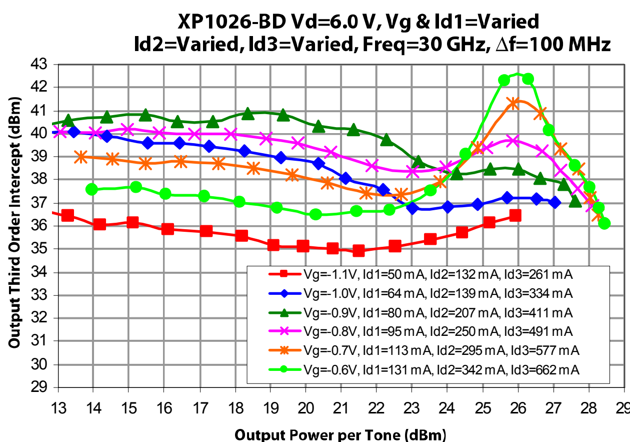

1. **Measurements –** On-Wafer Output Power data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition and tuned output matching network is recommended. For additional information see the M/A-COM Tech “T-Pad Transition” application note. Contact technical sales for output matching network information.

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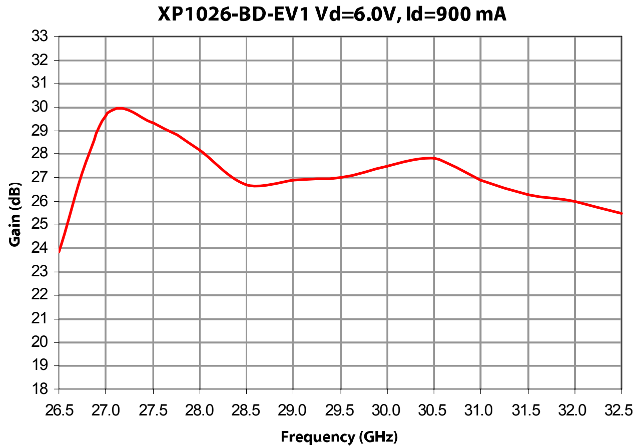
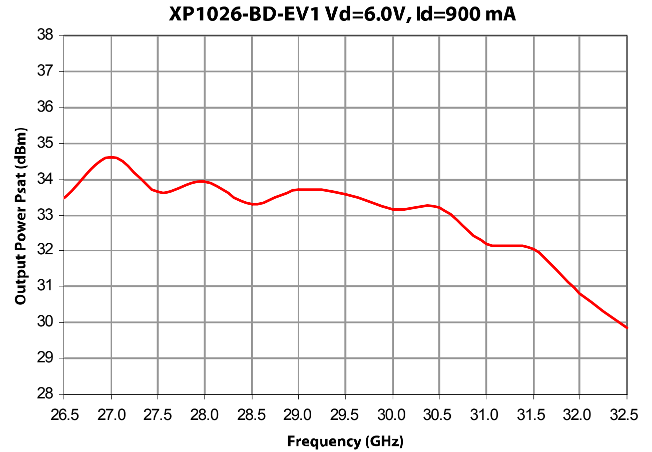
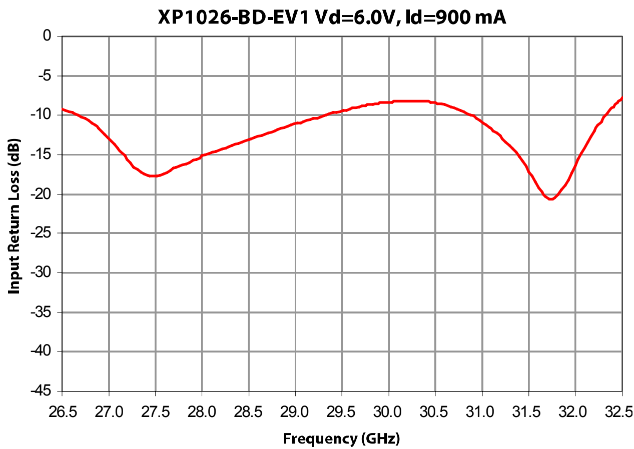
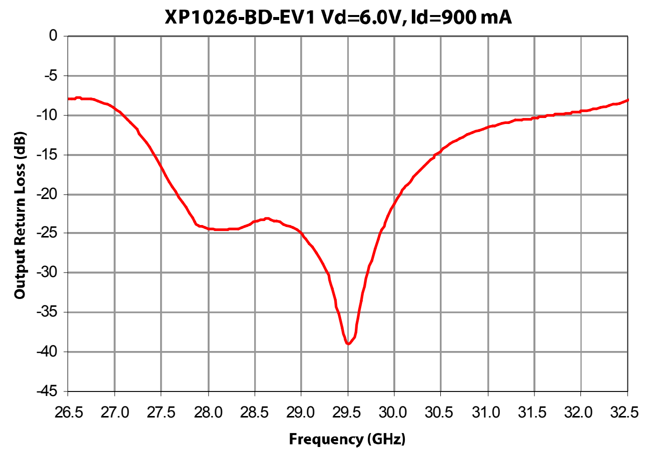
Typical Performance Curves (Text Fixture[1])









1. **Measurements –** Test Fixture data includes all bond wire parasitics, uncompensated RF In/Out M/A-COM Tech T-Pad transitions and RF ceramic circuit losses. For Gain and Output Power curves RF In/Out circuit losses have been removed.

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S-Parameters (On-Wafer[1])

Typcial S-Parameter Data for XP1026-BD
Vd=5.0 V, Id=752 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
20.0	0.847	171.50	0.015	-99.17	0.0018	40.23	0.923	140.91
21.0	0.841	166.55	0.022	-98.53	0.0016	46.62	0.907	133.10
22.0	0.822	160.39	0.033	-86.99	0.0016	54.34	0.879	123.51
23.0	0.787	152.73	0.076	-67.75	0.0022	42.02	0.831	110.21
24.0	0.720	142.08	0.320	-71.55	0.0019	28.90	0.749	91.92
25.0	0.579	127.16	1.554	-115.03	0.0019	22.54	0.591	60.58
26.0	0.280	111.47	6.221	165.52	0.0025	22.32	0.299	-0.74
27.0	0.270	-172.74	13.203	54.04	0.0037	-20.99	0.171	-140.68
28.0	0.374	169.06	13.466	-43.91	0.0023	-57.24	0.184	171.79
29.0	0.349	164.25	12.038	-120.22	0.0018	-62.39	0.192	165.70
30.0	0.324	157.94	11.121	173.96	0.0017	-60.58	0.197	156.08
31.0	0.293	141.14	11.071	110.20	0.0016	-104.46	0.191	137.21
32.0	0.220	105.44	11.725	40.04	0.0017	-99.98	0.204	95.72
33.0	0.239	12.75	11.119	-43.26	0.0021	-157.17	0.313	11.35
34.0	0.429	-44.62	6.839	-128.91	0.0036	91.59	0.493	-49.85
35.0	0.582	-74.93	3.254	163.30	0.0029	-11.61	0.592	-86.43
36.0	0.689	-91.39	1.577	111.44	0.0023	-88.63	0.631	-107.76
37.0	0.770	-102.86	0.840	67.95	0.0018	-165.75	0.651	-123.01
38.0	0.834	-112.17	0.477	27.51	0.0022	111.14	0.653	-135.32
39.0	0.872	-118.79	0.286	-10.00	0.0023	-1.66	0.629	-147.05
40.0	0.900	-124.20	0.178	-45.28	0.0015	-92.29	0.572	-158.59

1. **Measurements –** On-Wafer S-Parameters have been taken using reduced bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge.

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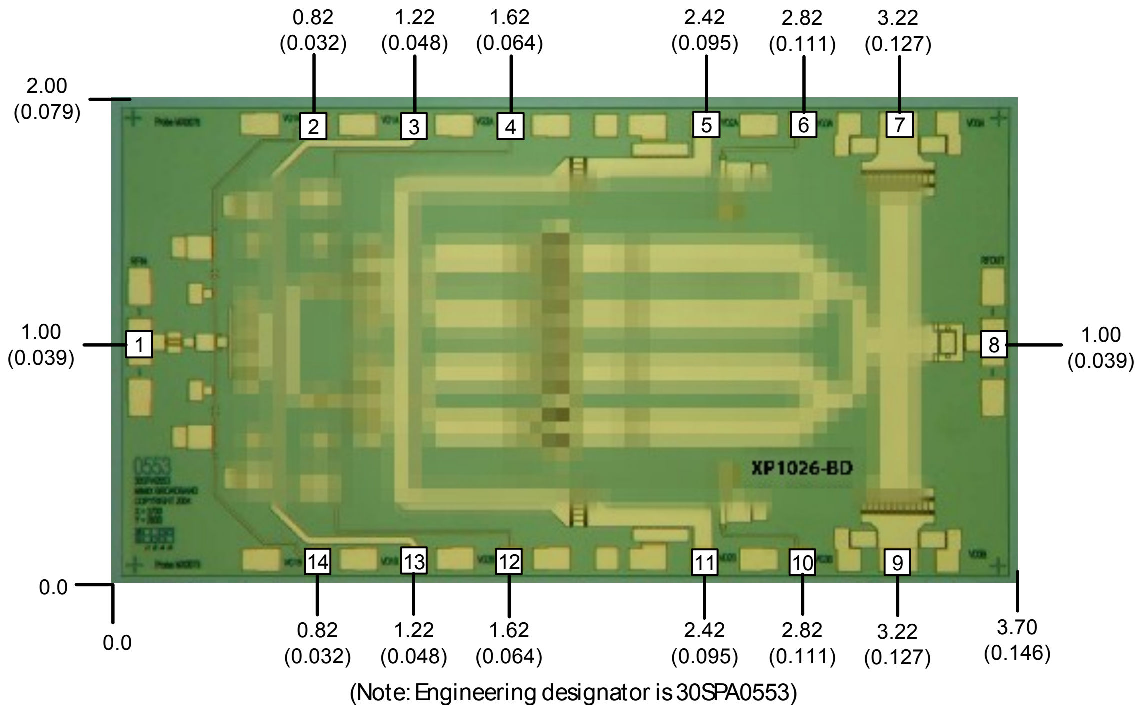
Mechanical Drawing

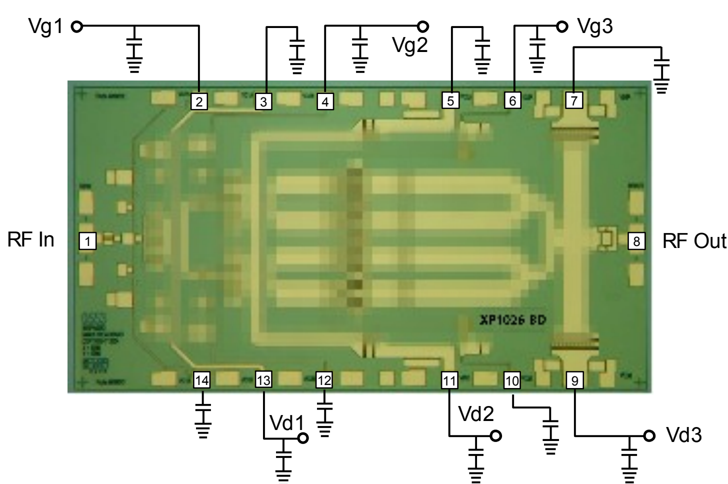


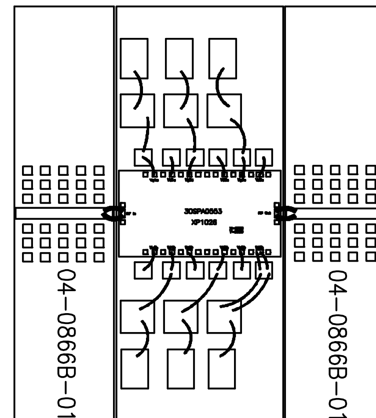
(Note: Engineering designator is 30SPA0553)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
Most DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF and Vd3 Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 4.588 mg.

Bond Pad #1 (RF In)
Bond Pad #2 (Vg1A)
Bond Pad #3 (Vd1A)
Bond Pad #4 (Vg2A)
Bond Pad #5 (Vd2A)
Bond Pad #6 (Vg3A)
Bond Pad #7 (Vd3A)
Bond Pad #8 (RF Out)
Bond Pad #9 (Vd3B)
Bond Pad #10 (Vg3B)
Bond Pad #11 Vd2B)
Bond Pad #12 (Vg2B)
Bond Pad #13 (Vd1B)
Bond Pad #14 (Vg1B)

Bias Arrangement (See App Notes [1], [2] and [3])





Layout for reference only – It is recommended to bias output stage from both sides.

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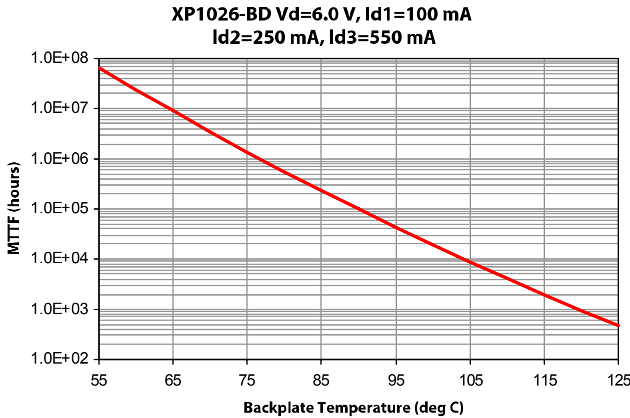
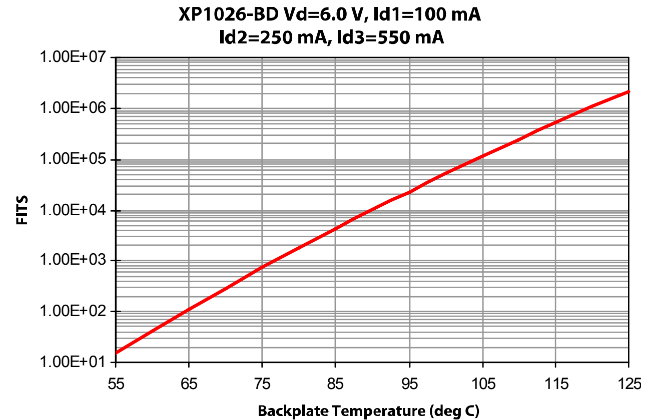
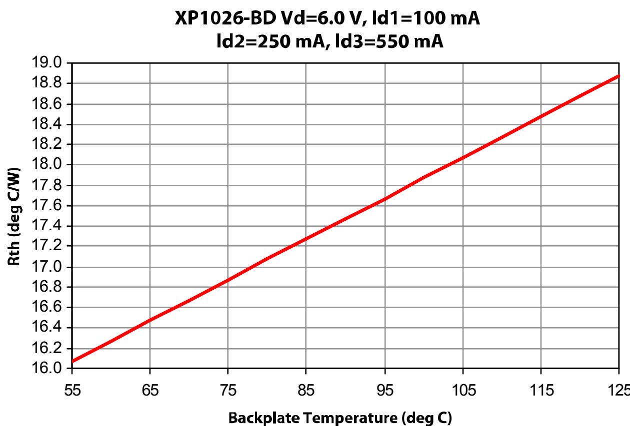
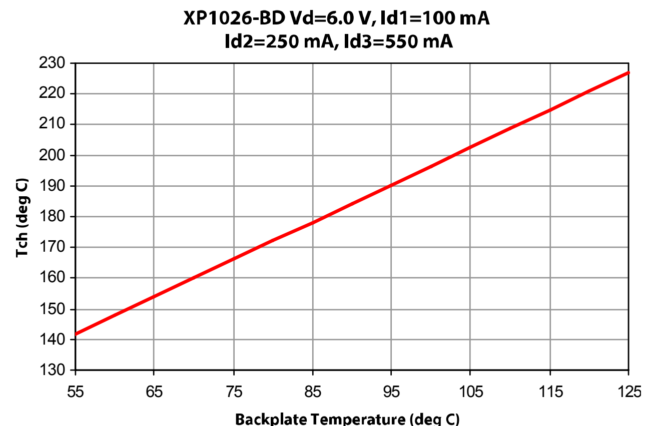
MTTF Graphs

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at M/A-COM Tech. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of die placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.









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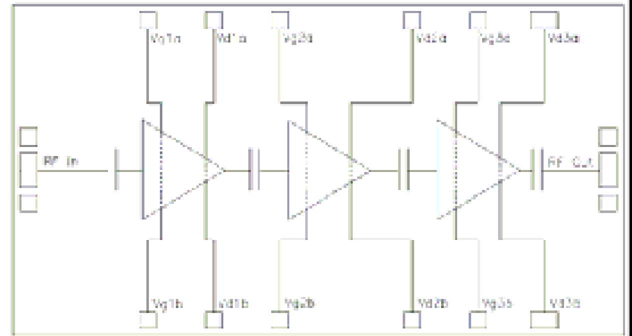

App Note [1] Biasing - It is recommended to separately bias each amplifier stage Vd1 through Vd3 at Vd(1,2,3) =5.5V with Id1=100mA, Id2=250mA and Id3=550mA. Separate biasing is recommended if the amplifier is to be used in a linear application or at high levels of saturation, where gate rectification will alter the effective gate control voltage. For non-critical applications it is possible to parallel all stages and adjust the common gate voltage for a total drain current Id(total)=900mA.

[Linear Applications] - For applications where the amplifier is being used in linear operation, where best IM3 (Third-Order Intermod) performance is required at more than 5dB below P1dB, it is also recommended to use active gate biasing to keep the drain currents constant as the RF power and temperature vary; this gives the best performance and most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate voltage of the pHEMT is controlled to maintain correct drain current compensating for changes over temperature.

[Saturated Applications] - For applications where the amplifier RF output power is saturated, the optimum drain current will vary with RF drive and each amplifier stage is best operated at a constant gate voltage. Significant gate currents will flow at saturation and bias circuitry must allow for drain current growth under this condition to achieve best RF output power and power added efficiency. Additionally, if the input RF power level will vary significantly, a more negative gate voltage will result in less die heating at lower RF input drive levels where the absence of RF cooling becomes significant. Note under this bias condition, gain will then vary with RF drive.

NOTE! - For any application it is highly recommended to bias the output amplifier stage from both sides for best RF and thermal performance.

CAUTION! - Also, make sure to properly sequence the applied voltages to ensure negative gate bias (Vg1,2,3) is available before applying the positive drain supply (Vd1,2,3). Additionally, it is recommended that the device gates are protected with Silicon diodes to limit the applied voltage.

App Note [2] Bias Arrangement -
[For Individual Stage Bias] (recommended for linear/saturated applications) - Each DC pad (Vd1,2,3 and Vg1,2,3) needs to have DC bypass capacitance (100-200 pF) as close to the device as possible. Additional DC bypass capacitance (1 nF and 3.3 uF) is also recommended. All DC pads have been tied together on chip and device can be biased from either side.

[For Parallel Stage Bias] (general applications) - The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors (100-200 pF) are tied together at one point after bypass capacitance. Additional DC bypass capacitance (1 nF and 3.3 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads. All DC pads have been tied together on chip and can be biased from either side.

NOTE! In either arrangement, for most stable performance all unused DC pads must also be bypassed with at least 100-200 pf capacitance.

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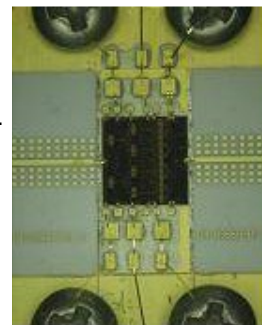
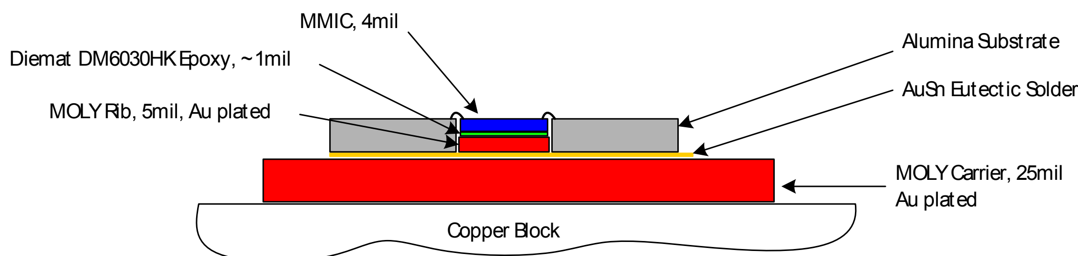


App Note [3] Material Stack-Up – In addition to the practical aspects of bias and bias arrangement, device base material stack-up also must be considered for best thermal performance. A well thought out thermal path solution will improve overall device reliability, RF performance and power added efficiency. The photo shows a typical high power amplifier carrier assembly. The material stack-up for this carrier is shown below. This stack-up is highly recommended for most reliable performance however, other materials (i.e. eutectic solder vs epoxy, copper tungsten/copper moly rib, etc.) can be considered/possibly used but only after careful review of material thermal properties, material availability and end application performance requirements.



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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

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