XP1027-BD

Power Amplifier
27 - 31 GHz

Rev. V2

Features

- Ka-Band 4 W Power Amplifier
- Balanced Design, Good Input / Output Match
- 25 dB Small Signal Gain
- 35 dBm Saturated Output Power
- 43 dBm Output Third Order Intercept (OIP3)
- 100% On-Wafer Testing
- 100% Visual Inspection
- RoHS* Compliant and 260°C Reflow Compatible

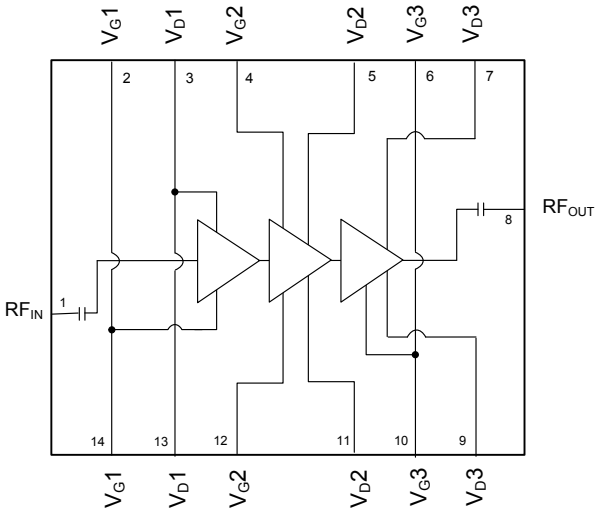
Description

The XP1027-BD is a three-stage 27 - 31 GHz GaAs MMIC power amplifier that provides 25 dB small signal gain and 35 dBm saturated output power. The device includes Lange couplers to achieve good input/output return loss.

Backside via holes and gold metallization to allow die attach with either conductive epoxy or eutectic solder. Passivation protects the die surface.

This power amplifier is well suited for millimeter-wave, point-to-point radio, SATCOM, LMDS and VSAT applications.

Functional Diagram



Pin Configuration[1]

Pad	Function	Description
1	RF_{IN}	RF Input
2,14	V_G1	Gate Voltage Stage 1
3,13	V_D1	Drain Voltage Stage 1
4,12	V_G2	Gate Voltage Stage 2
5,11	V_D3	Drain Voltage Stage 3
6,10	V_G3	Gate Voltage Stage 4
7,9	V_D3	Drain Voltage Stage 4
8	RF_{OUT}	RF Output

1. Backside metal is RF, DC and thermal ground.

Ordering Information

Part Number	Package
XP1027-BD-000V	"V" - vacuum release gel packs

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications: 27 - 31 GHz, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	22	25	-
Gain Flatness	dB	-	+/-1	-
Input Return Loss	dB	-	20	-
Output Return Loss	dB	-	20	-
Reverse Isolation	dB	-	50	-
P1dB	dBm	-	34	-
Output IP3	dBm	-	43	-
Saturated P_{OUT}, Pulsed P_{IN}	dBm	33	35	-
Drain Bias Voltage	VDC	-	5.0	5.8
Gate Bias Voltage	VDC	-1.0	-0.7	0.0
Supply Current, V_D = 5 V, V_G = -0.7 V I_D1 I_D2 I_D3	mA	-	 240 630 1240	 300 750 1435

Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage[2]	+6 VDC
Supply Current I_D1 I_D2 I_D3	 325 mA 825 mA 1575 mA
Gate Bias Voltage	-1.5 < Vg < 0 V
Input Power	+25 dBm
Storage Temperature	-65°C to +165°C
Operating Temperature	-55°C to +85°C
Channel Temperature[3]	175°C

2. Under pulsed bias conditions, under CW P_{SAT} conditions further reduction in max supply voltage (~0.5 V) is recommended.
3. Channel temperature should be kept as low as possible to maximize lifetime.

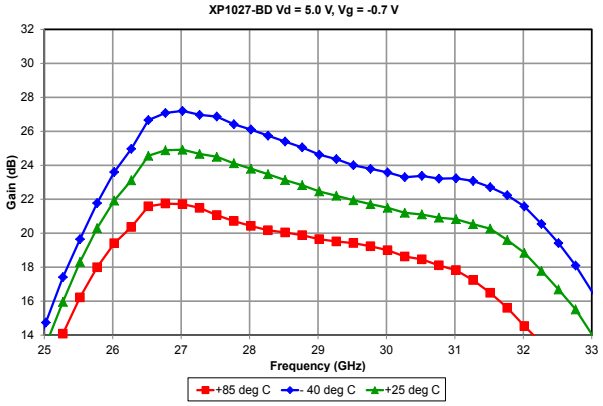
Handling Procedures

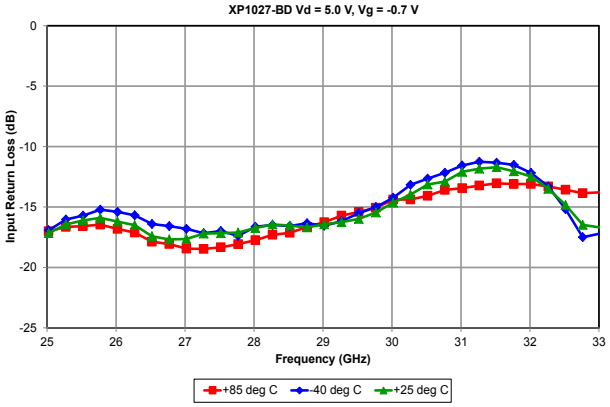
Please observe the following precautions to avoid damage:

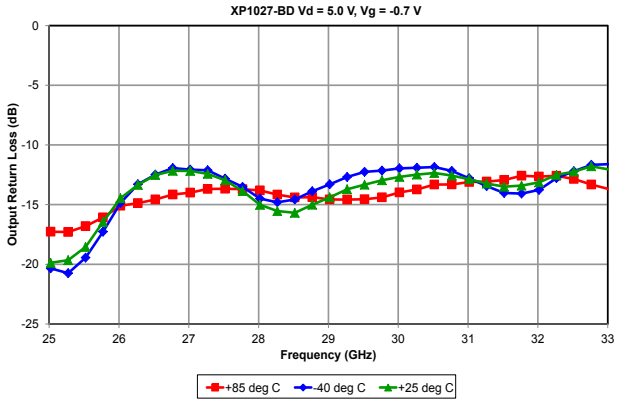
Static Sensitivity

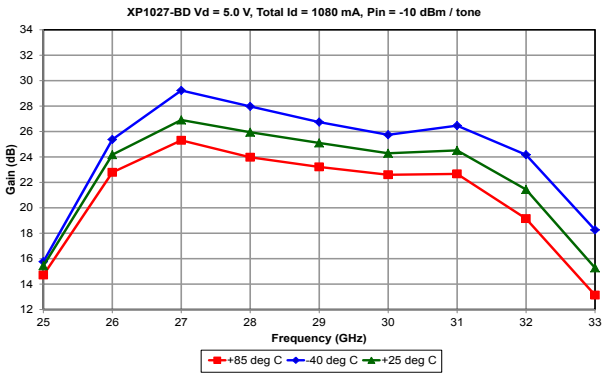
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 2 devices.

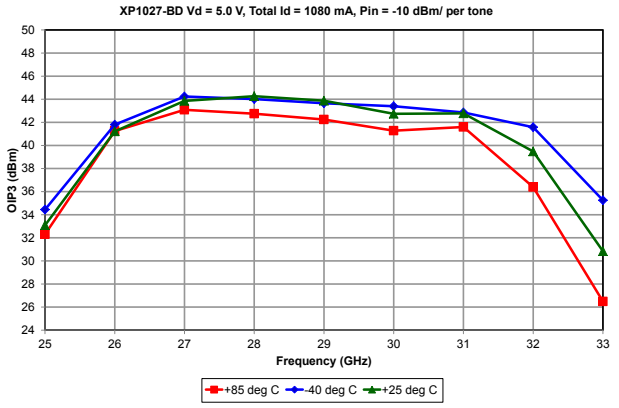
Typical Performance Curves (Test Fixture[4])





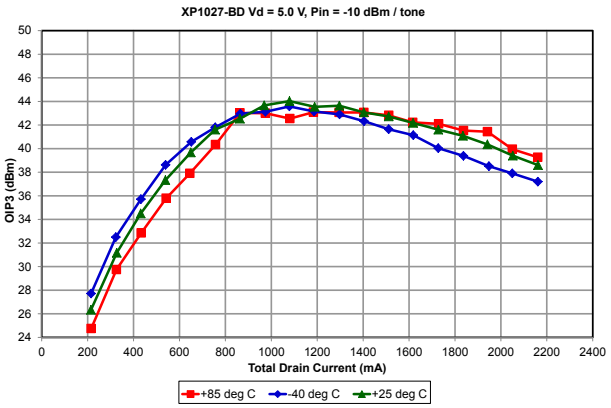


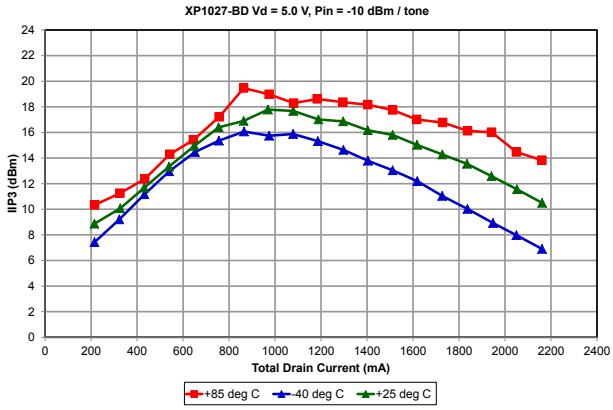


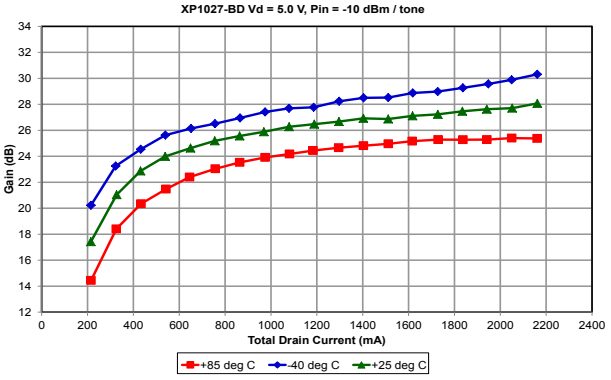


4. Measurements – Test Fixture data includes all bond wire parasitics, uncompensated RF In/Out MACOM T-Pad transitions and RF ceramic circuit losses. For Gain and Output Power curves RF In/Out circuit losses have been removed.

Typical Performance Curves (Test Fixture[5])



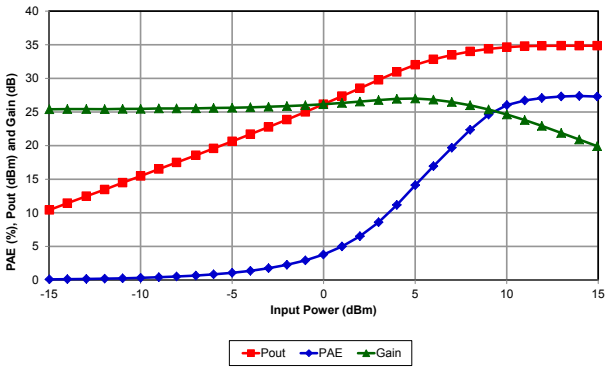




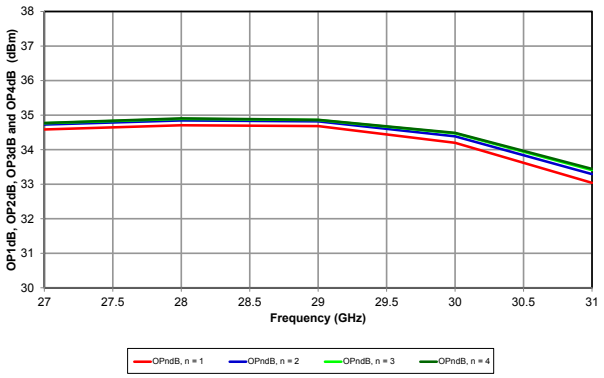
5. Measurements – Test Fixture data includes all bond wire parasitics, uncompensated RF In/Out MACOM T-Pad transitions and RF ceramic circuit losses. For Gain and Output Power curves RF In/Out circuit losses have been removed.

Typical Performance Curves

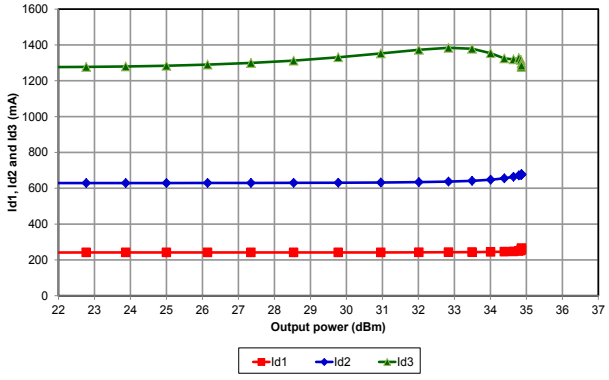
XP1027-BD Vd = 5.0 V, Vg = -0.7 V, Frequency = 29 GHz, CW



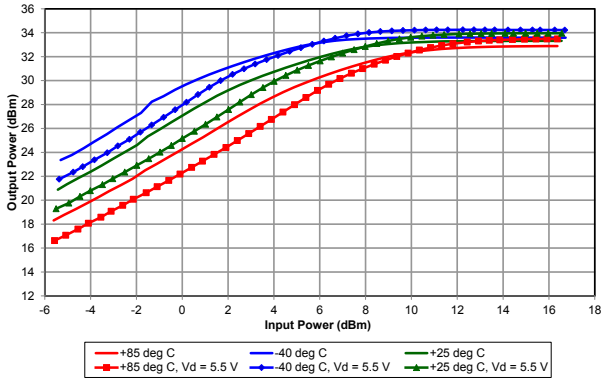
XP1027-BD, Vd = 5.0 V, VG = -0.7 V, CW



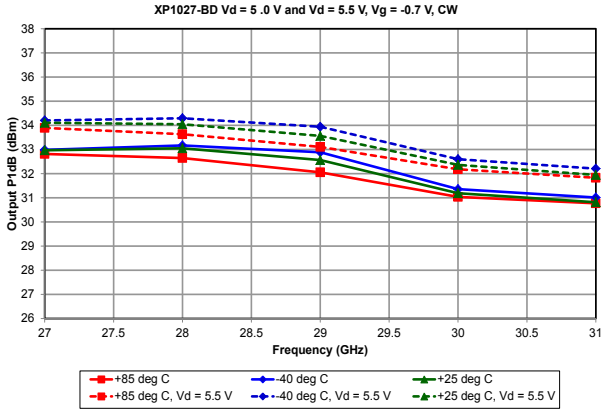
XP1027-BD Vd = 5.0 V, Vg = -0.7 V, CW



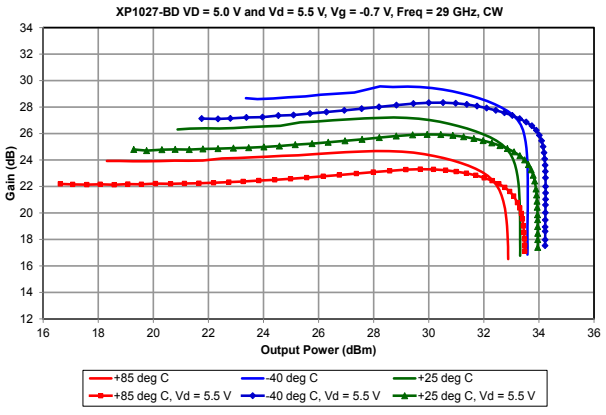
XP1027-BD VD = 5.0 V and Vd = 5.5 V, Vg = -0.7 V, Freq = 29 GHz, CW



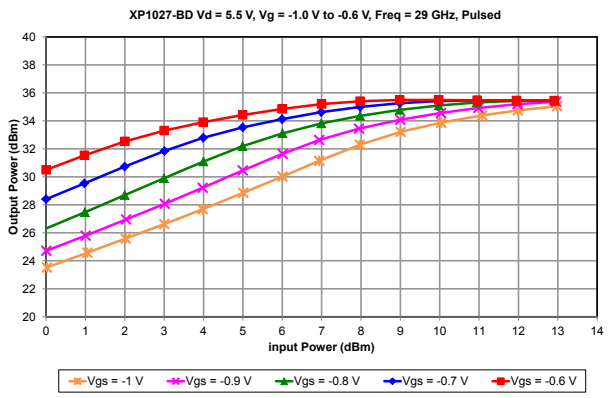
XP1027-BD Vd = 5 .0 V and Vd = 5.5 V, Vg = -0.7 V, CW

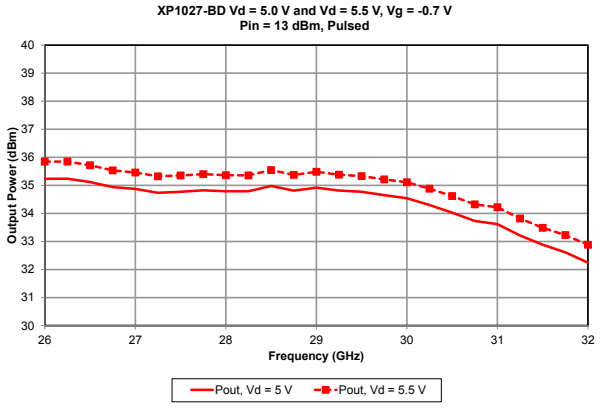


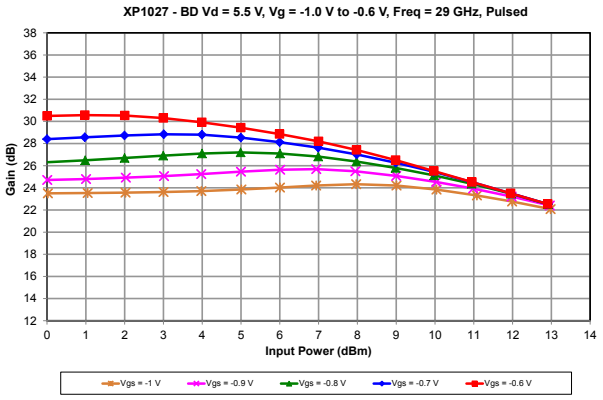
XP1027-BD VD = 5.0 V and Vd = 5.5 V, Vg = -0.7 V, Freq = 29 GHz, CW

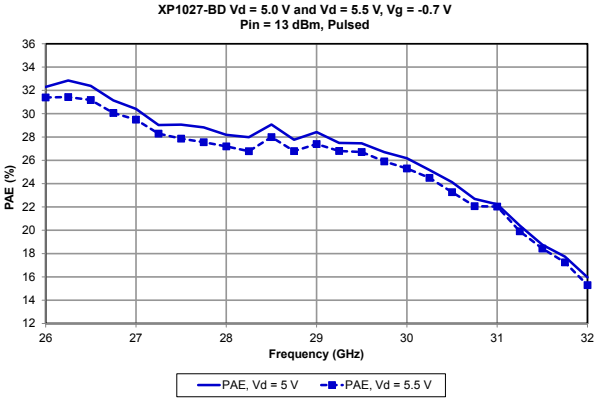


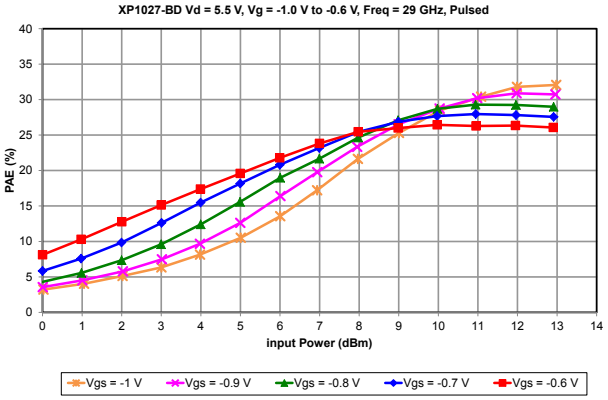
Typical Performance Curves[6]

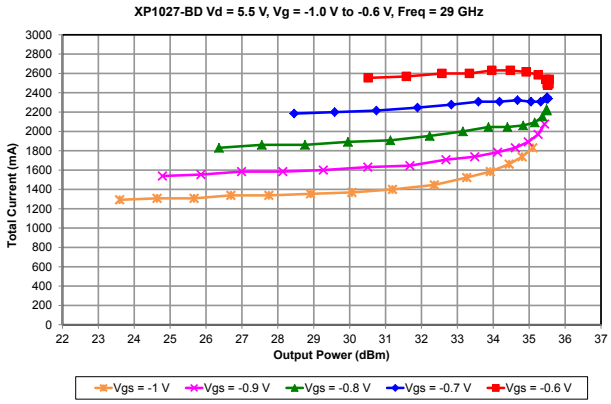






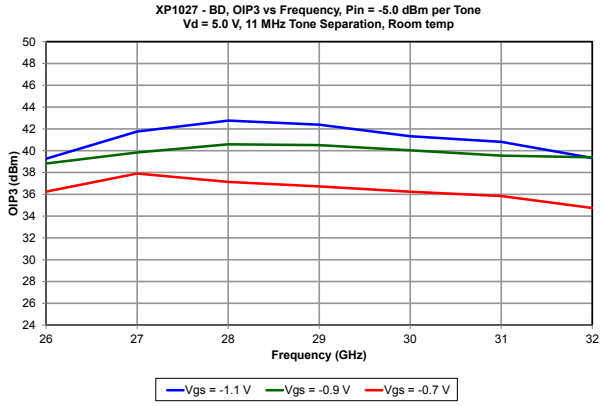


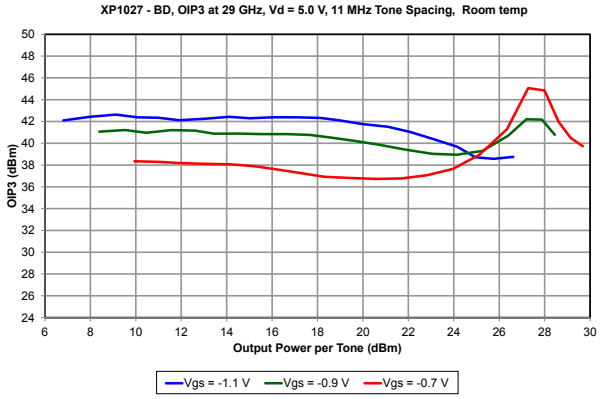


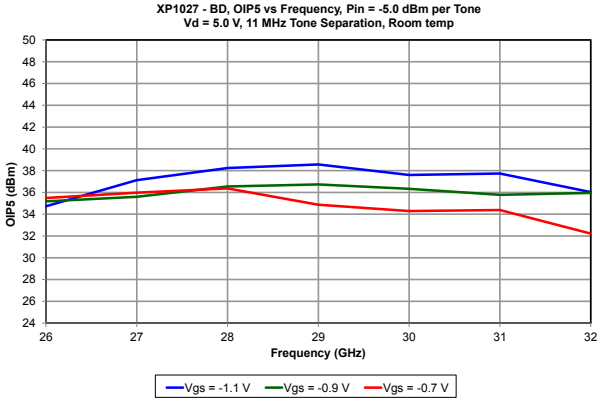


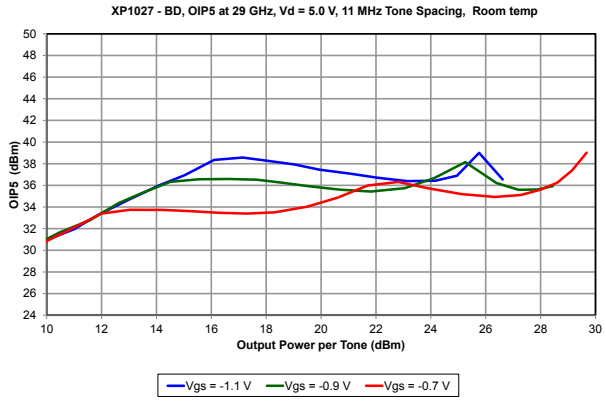
6. Test conditions – Measurements are referenced 150 µm in from RF In/Out pad edge. For optimum performance MACOM T-pad transition and tuned output matching network is recommended. For additional information see the MACOM "T-Pad Transition" application note. Contact technical sales for output matching network information.

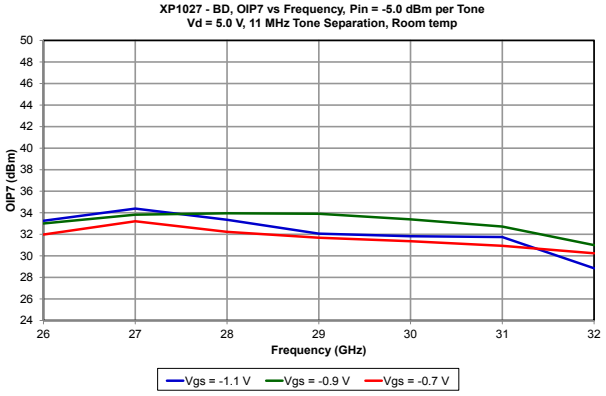
Typical Performance Curves[7,8]

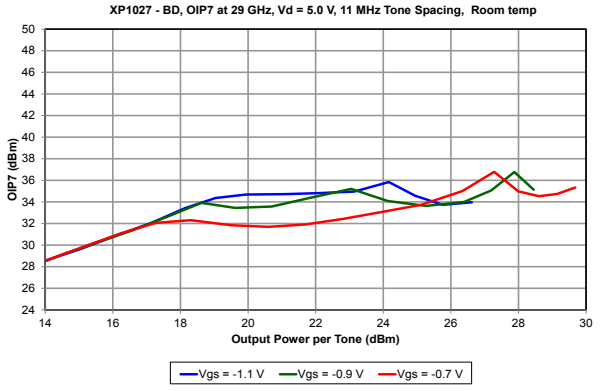






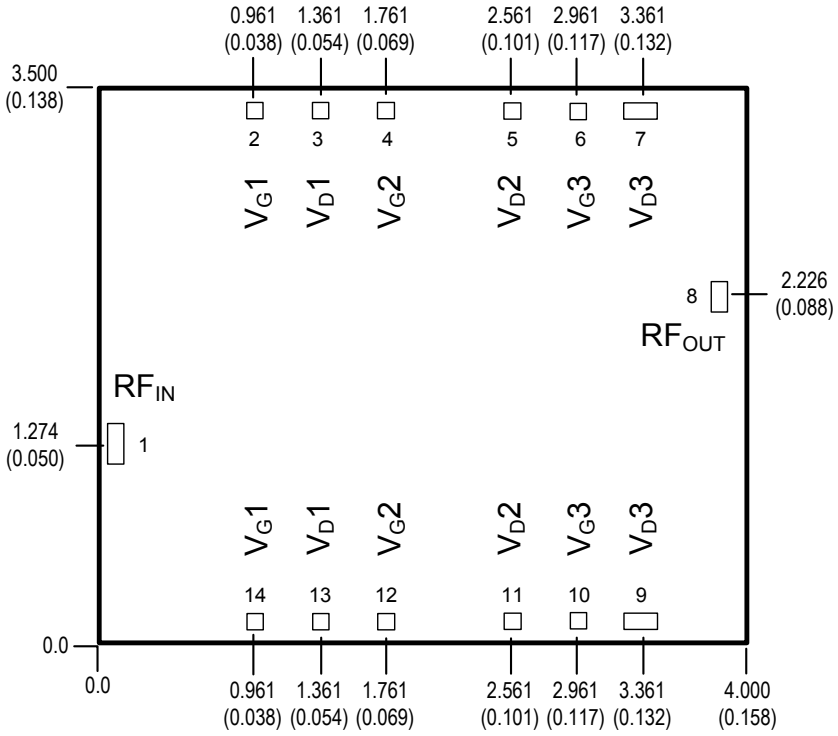






7. Test conditions – Measurements are referenced 150 µm in from RF In/Out pad edge. For optimum performance MACOM T-pad transition and tuned output matching network is recommended. For additional information see the MACOM “T-Pad Transition” application note. Contact technical sales for output matching network information.
8. Additional Data – The XP1027 device consists of a balanced XP1026 pair. See the XP1026 data sheet for additional data concerning OIP3 control and optimization.

Die Outline



NOTES:
All Dimensions shown as mm/inches.
Bond pad dimensions are shown to center of bond pad.
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Thickness is 0.110 ±0.010 (0.0046 ±0.0004).
Backside is ground. Bond pad and backside metallization are gold.
Most DC bond pads are 0.100 x 0.100 (0.004 x 0.004).
All RF and V_D3 bond pads are 0.100 x 0.200 (0.004 x 0.008)
Dicing tolerance is ±0.005 (±0.0002). Approximate weight is 8.68 mg.

App Note [1] Biasing -
It is recommended to separately bias each amplifier stage V_D1 through V_D3 at V_D (1,2,3) = 5 V with I_D1 = 240 mA, I_D2 = 630 mA and I_D3 = 1240 mA. Separate biasing is recommended if the amplifier is to be used in a linear application or at high levels of saturation, where gate rectification will alter the effective gate control voltage. For non-critical applications it is possible to parallel all stages and adjust the common gate voltage for a total drain current I_D (total) = 2110 mA.

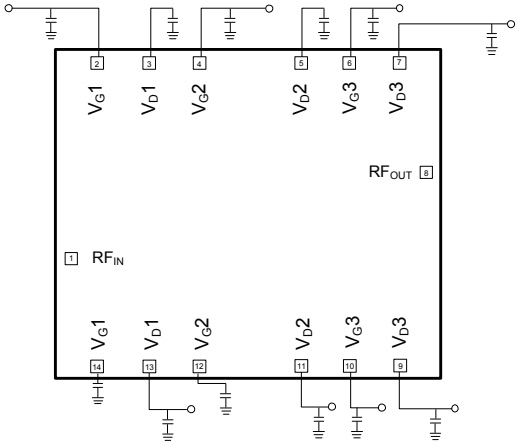
Linear Applications -
For applications where the amplifier is being used in linear operation, where best IM3 (Third-Order Intermod) performance is required at more than 5 dB below P1dB, it is recommended to use active gate biasing to keep the drain currents constant as the RF power and temperature vary; this gives the best performance and most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate voltage of the pHEMT is controlled to maintain correct drain current compensating for changes over temperature.

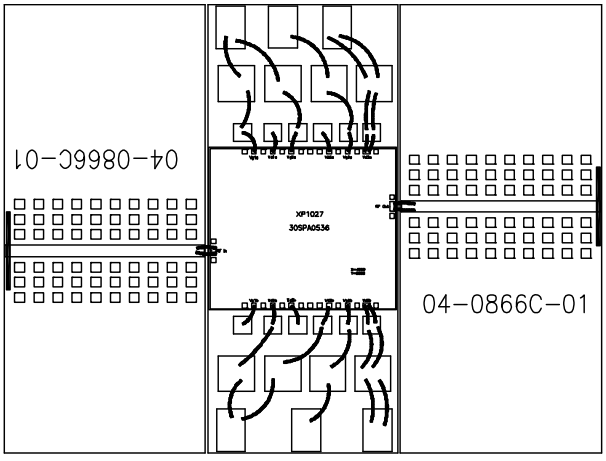
Saturated Applications -
For applications where the amplifier RF output power is saturated, the optimum drain current will vary with RF drive and each amplifier stage is best operated at a constant gate voltage. Significant gate currents will flow at saturation and bias circuitry must allow for drain current growth under this condition to achieve best RF output power and power added efficiency. If the input RF power level will vary significantly, a more negative gate voltage will result in less die heating at lower RF input drive levels where the absence of RF cooling becomes significant. Under this bias condition, gain will then vary with RF drive

NOTE -
For any application it is highly recommended to bias the output amplifier stage from both sides for best RF and thermal performance.

CAUTION -
Make sure to properly sequence the applied voltages to ensure negative gate bias (V_G1,2,3) is available before applying the positive drain supply (V_D1,2,3). It is recommended that the device gates are protected with silicon diodes to limit the applied voltage.

Bias Arrangement





Layout for reference only – It is recommended to bias output stage from both sides.