

XP10TN135H

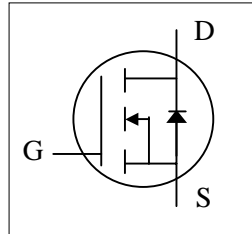
Halogen-Free Product



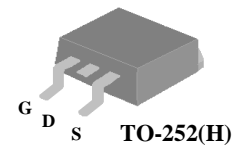
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	100V
R _{DS(ON)}	135mΩ
I _D	8.1A



Description

XP10TN135 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V	8.1	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	5.1	A
I _{DM}	Pulsed Drain Current ¹	28	A
P _D @T _C =25°C	Total Power Dissipation	20.8	W
P _D @T _A =25°C	Total Power Dissipation ³	2	W
E _{AS}	Single Pulse Avalanche Energy ⁴	8	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	6	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	62.5	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	-	-	135	m Ω
		$V_{GS}=4.5V, I_D=3A$	-	-	145	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=5A$	-	17	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=5A$ $V_{DS}=80V$ $V_{GS}=10V$	-	11	17.6	nC
Q_{gs}	Gate-Source Charge		-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	2	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=50V$	-	6	-	ns
t_r	Rise Time	$I_D=5A$	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	14	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	3	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	580	928	pF
C_{oss}	Output Capacitance	$V_{DS}=50V$	-	27	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	19	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	2	4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=5A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_S=5A, V_{GS}=0V,$ $di/dt=100A/\mu s$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge		-	18	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=50V$, $L=1\text{mH}$, $R_G=25\Omega$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT

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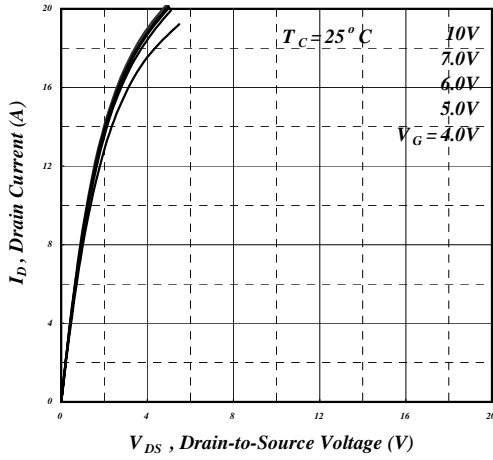


Fig 1. Typical Output Characteristics

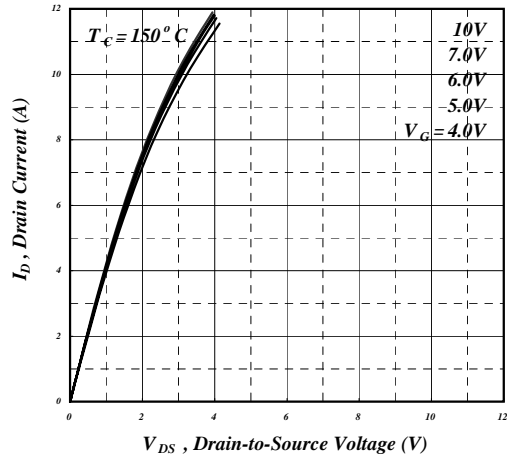


Fig 2. Typical Output Characteristics

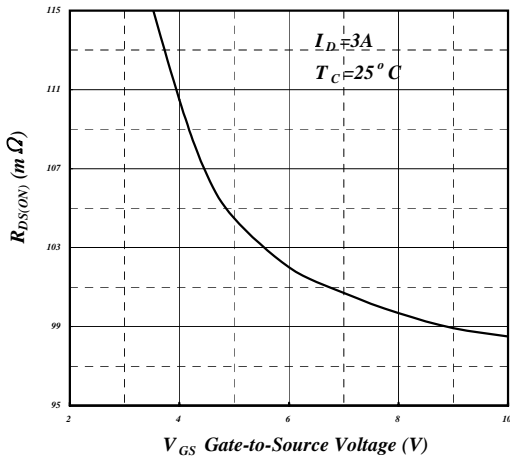


Fig 3. On-Resistance v.s. Gate Voltage

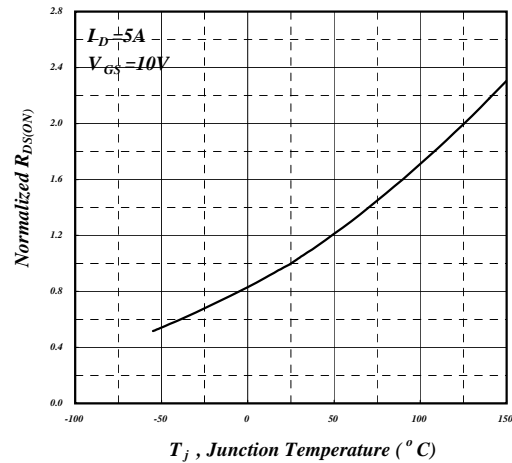


Fig 4. Normalized On-Resistance v.s. Junction Temperature

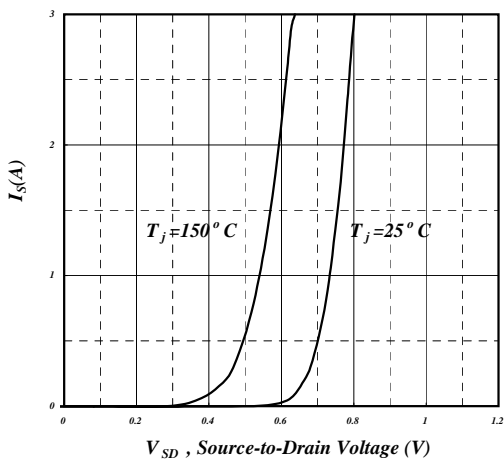


Fig 5. Forward Characteristic of Reverse Diode

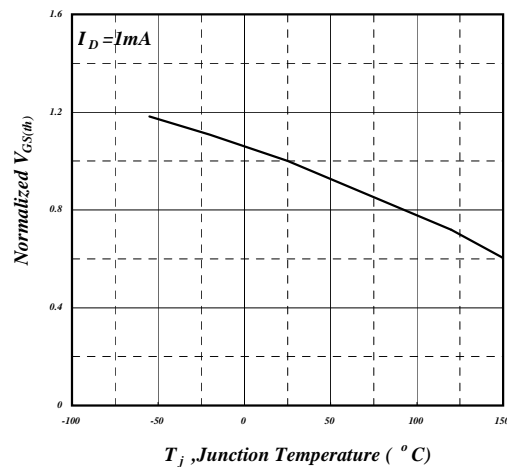


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

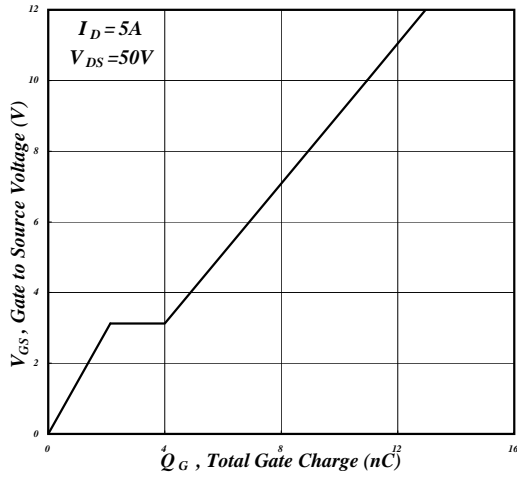


Fig 7. Gate Charge Characteristics

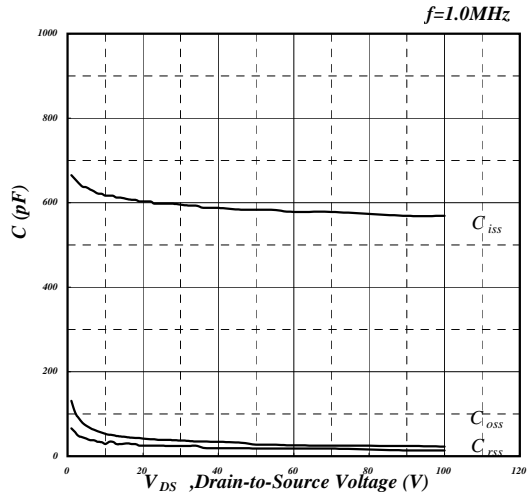


Fig 8. Typical Capacitance Characteristics

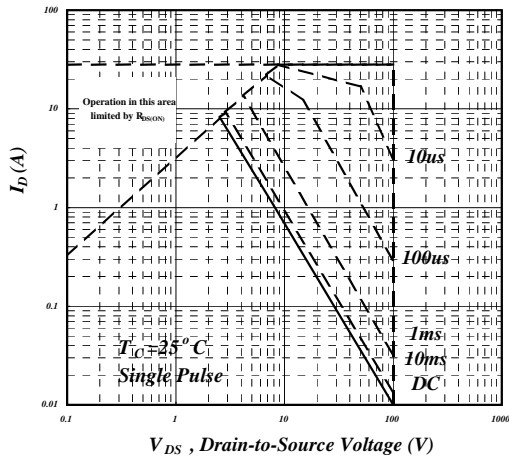


Fig 9. Maximum Safe Operating Area

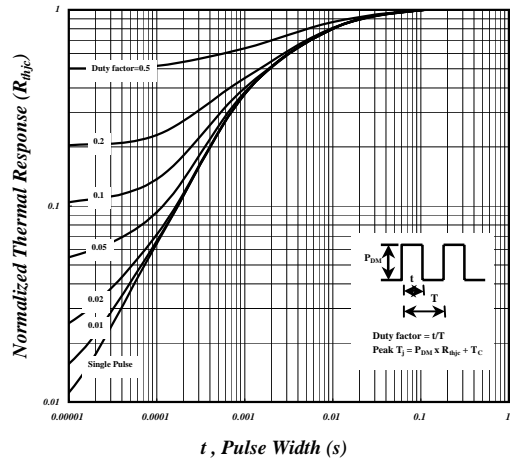


Fig 10. Effective Transient Thermal Impedance

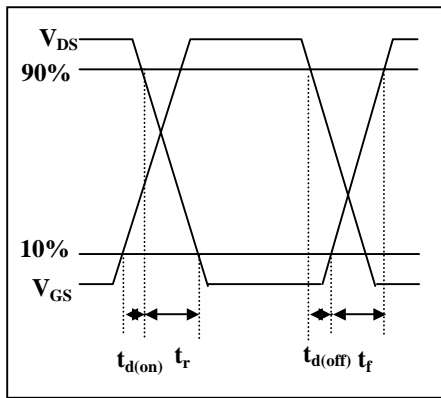


Fig 11. Switching Time Waveform

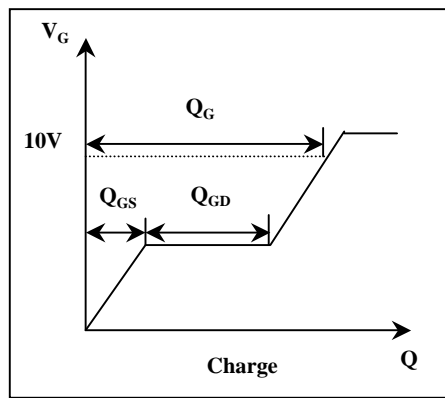


Fig 12. Gate Charge Waveform

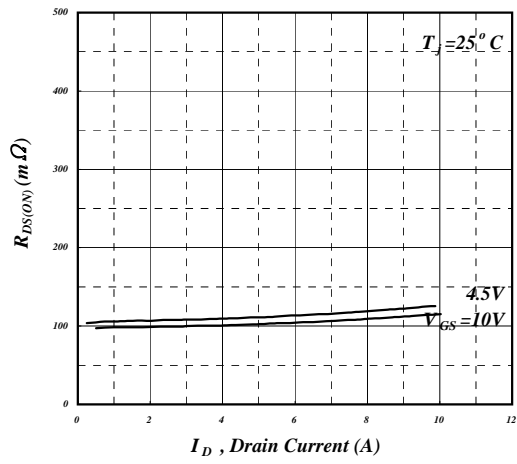


Fig 13. Typ. Drain-Source on State Resistance

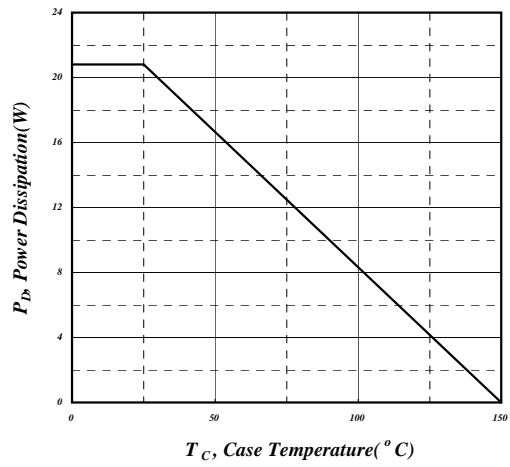


Fig 14. Total Power Dissipation

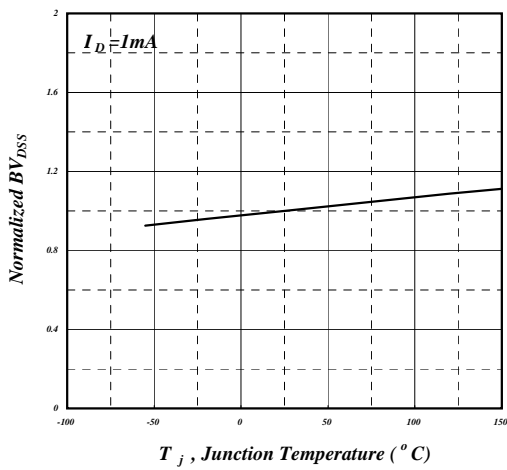


Fig 15. Normalized BV_{DSS} v.s. Junction