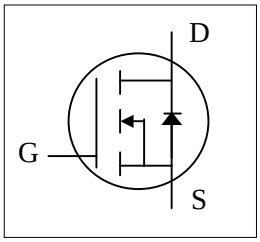
XP10TN135K

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- **Simple Drive Requirement**
- **Lower Gate Charge**
- **Fast Switching Characteristic**
- **Halogen Free & RoHS Compliant Product**

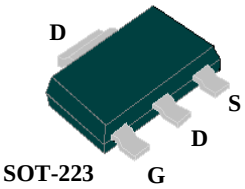


BV_{DSS}	100V
$R_{DS(ON)}$	135mΩ
I_D	3A

Description

XP10TN135 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SOT-223 package is designed for suface mount application, larger heatsink than SO-8 and SOT package.



SOT-223

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current[3], V_{GS} @ 10V	3	A
I_D@T_A=70℃	Drain Current[3], V_{GS} @ 10V	2.4	A
I_{DM}	Pulsed Drain Current[1]	12	A
P_D@T_A=25℃	Total Power Dissipation	2.78	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	45	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=3A	-	115	135	mΩ
		V_{GS}=4.5V, I_D=2A	-	122	145	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	1.7	3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=3A	-	11	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=3A	-	12	20	nC
Q_{gs}	Gate-Source Charge	V_{DS}=80V	-	2.2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	2.5	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V	-	7	-	ns
t_r	Rise Time	I_D=1A	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	16	-	ns
t_f	Fall Time	V_{GS}=10V	-	6	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	610	980	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	40	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	25	-	pF
R_g	Gate Resistance	f=1.0MHz	-	2.2	4.4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=2A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_S=3A, V_{GS}=0V,	-	22	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	23	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 120 ℃/W when mounted on Min. copper pad.

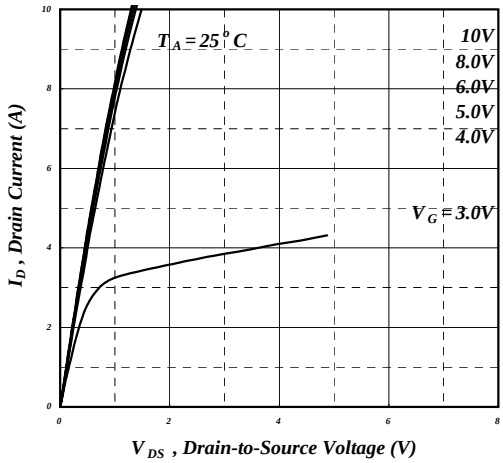


Fig 1. Typical Output Characteristics

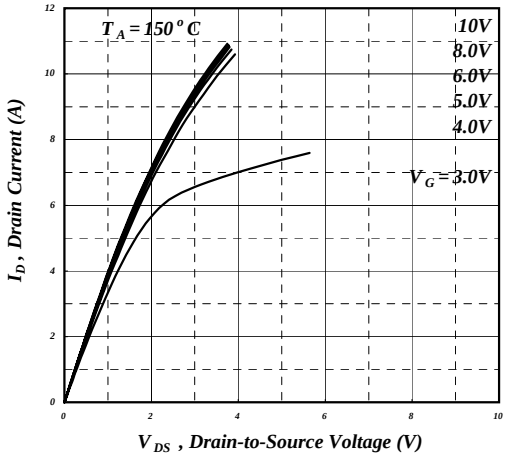


Fig 2. Typical Output Characteristics

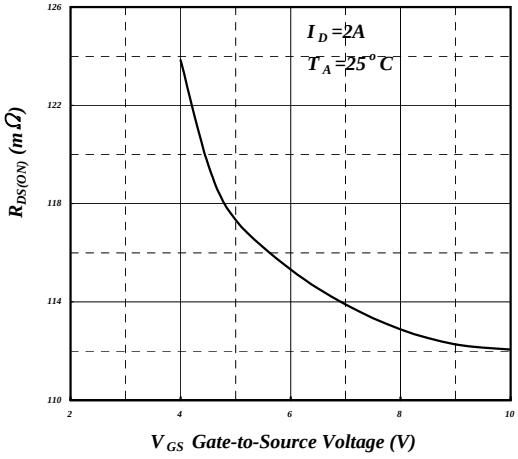


Fig 3. On-Resistance v.s. Gate Voltage

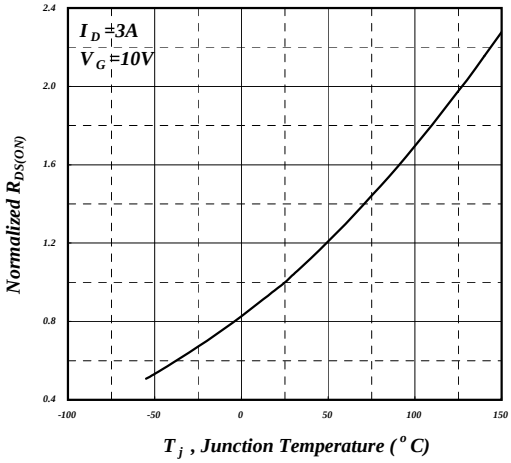


Fig 4. Normalized On-Resistance v.s. Junction Temperature

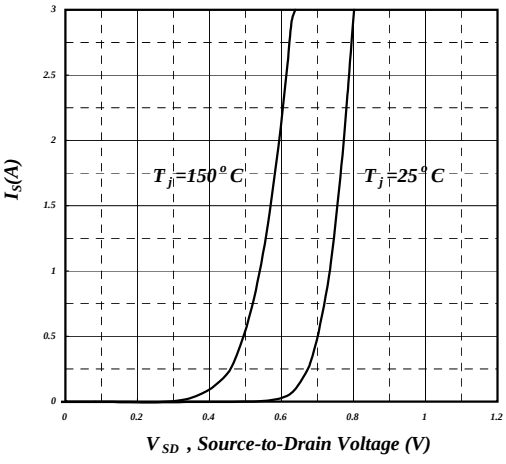


Fig 5. Forward Characteristic of Reverse Diode

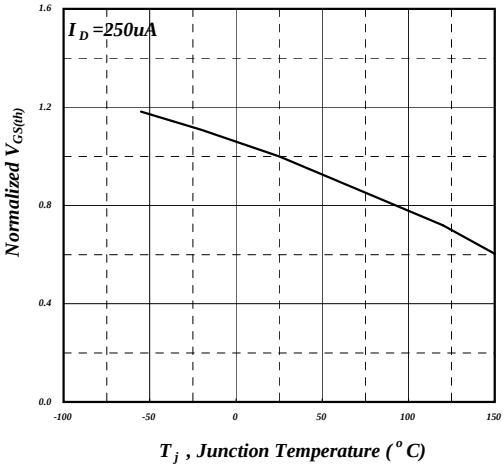


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

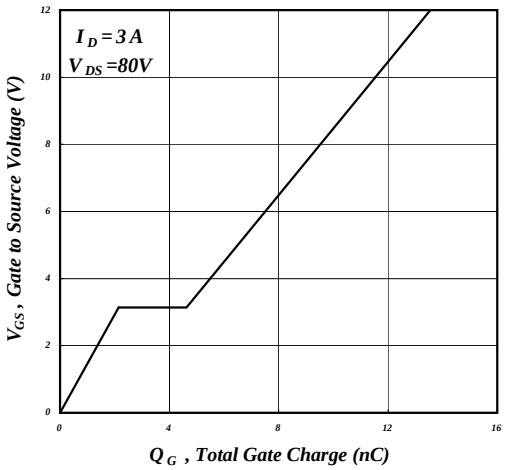


Fig 7. Gate Charge Characteristics

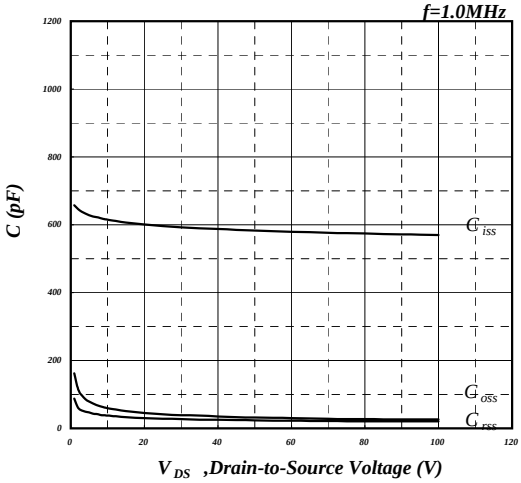


Fig 8. Typical Capacitance Characteristics

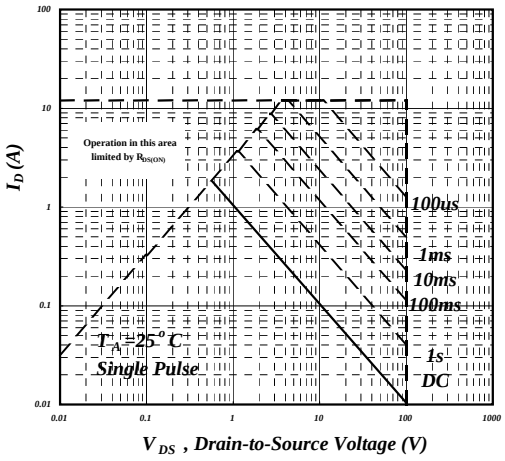


Fig 9. Maximum Safe Operating Area

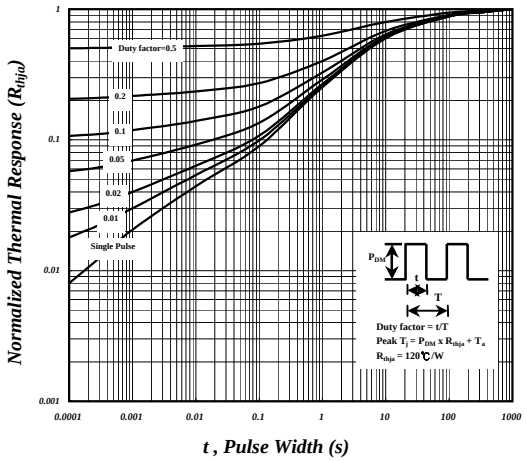


Fig 10. Effective Transient Thermal Impedance

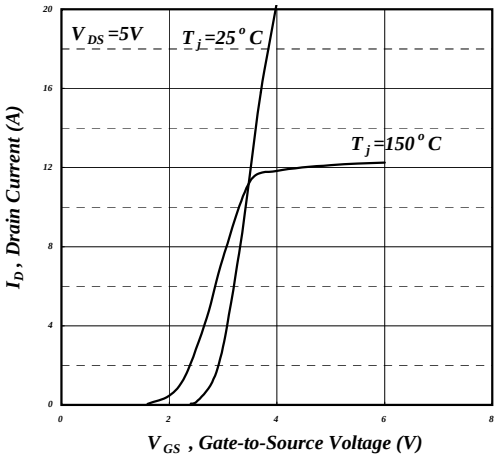


Fig 11. Transfer Characteristics

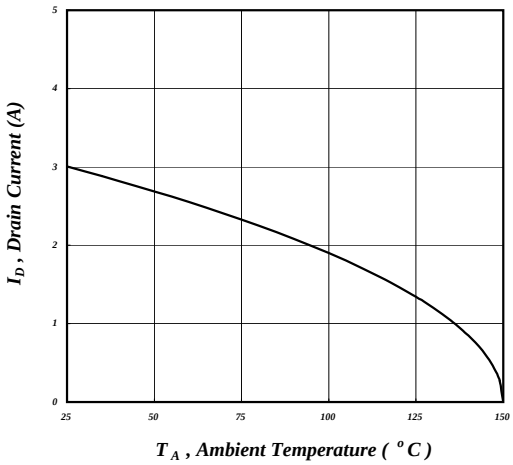


Fig 12. Drain Current v.s. Ambient Temperature

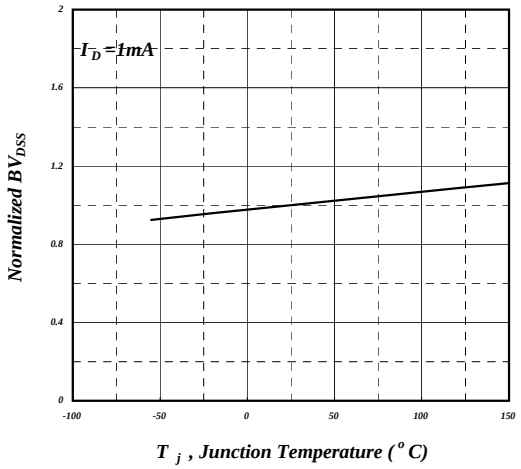


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

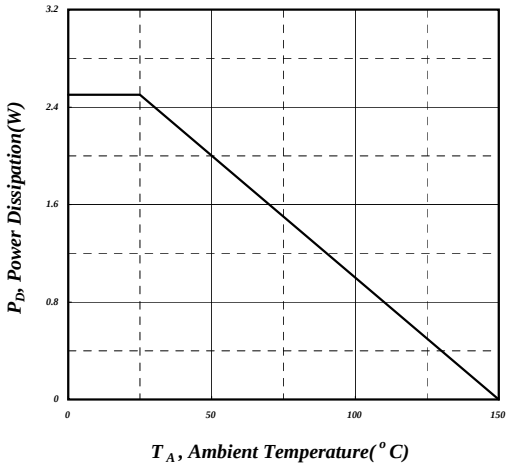


Fig 14. Total Power Dissipation

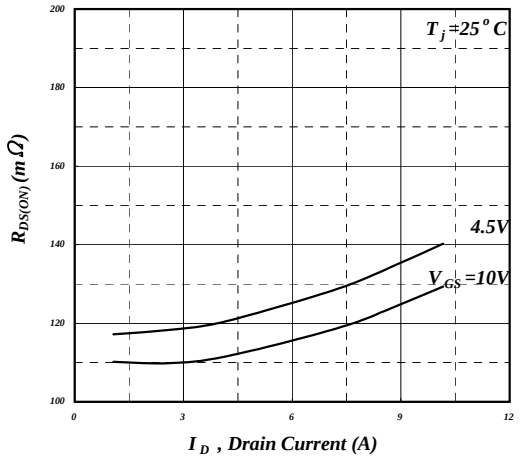


Fig 15. Typ. Drain-Source on State Resistance