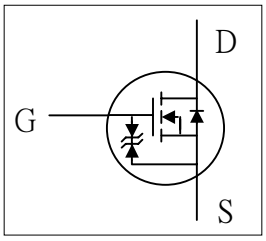
# XP2N1K2EN1

**Halogen-Free Product**

*N-CHANNEL ENHANCEMENT MODE*

*POWER MOSFET*

- **Capable of 1.2V Low Gate Drive**
- **Lower Gate Charge**
- **Fast Switching Performance**
- **RoHS Compliant & Halogen-Free**

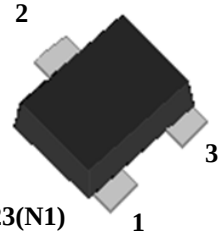



| | |
|---|---|
| $BV_{DSS}$ | 20V |
| $R_{DS(ON)}$ | 1.2Ω |
| $I_D$ | 200mA |
| HBM ESD | 2KV |

## Description

XP2N1K2E series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SOT-723 Package with very small footprint is suitable for all commercial-industrial surface mount application.




**SOT-723(N1)**

**1 : Gate**
**2 : Drain**
**3 : Source**

## Absolute Maximum Ratings@$T_j$=25°C(unless otherwise specified)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 20 | V |
| $V_{GS}$ | Gate-Source Voltage | ±8 | V |
| $I_D$@$T_A$=25℃ | Drain Current[3], $V_{GS}$ @ 2.5V | 200 | mA |
| $I_{DM}$ | Pulsed Drain Current[1] | 400 | mA |
| $I_S$@$T_A$=25℃ | Source Current (Body Diode) | 125 | mA |
| $I_{SM}$ | Pulsed Source Current[1](Body Diode) | 800 | mA |
| $P_D$@$T_A$=25℃ | Total Power Dissipation | 0.15 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |

## Thermal Data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Rthj-a | Maximum Thermal Resistance, Junction-ambient[3] | 833 | ℃/W |

## Electrical Characteristics@$T_j$=25°C(unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250uA | 20 | - | - | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=2.5V, $I_D$=200mA | - | - | 1.2 | Ω |
| | | $V_{GS}$=1.8V, $I_D$=200mA | - | - | 1.4 | Ω |
| | | $V_{GS}$=1.5V, $I_D$=40mA | - | - | 2.4 | Ω |
| | | $V_{GS}$=1.2V, $I_D$=20mA | - | - | 4.8 | Ω |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=1mA | 0.3 | - | 1 | V |
| $g_{fs}$ | Forward Transconductance | $V_{DS}$=10V, $I_D$=200mA | - | 1.8 | - | S |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=16V, $V_{GS}$=0V | - | - | 10 | uA |
| $I_{GSS}$ | Gate-Source Leakage | $V_{GS}$=±8V, $V_{DS}$=0V | - | - | ±30 | uA |
| $Q_g$ | Total Gate Charge | $I_D$=200mA | - | 0.7 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{DS}$=10V | - | 0.2 | - | nC |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | $V_{GS}$=2.5V | - | 0.2 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=10V | - | 2 | - | ns |
| $t_r$ | Rise Time | $I_D$=150mA | - | 10 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G$=10Ω | - | 30 | - | ns |
| $t_f$ | Fall Time | $V_{GS}$=5V | - | 16 | - | ns |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V | - | 44 | - | pF |
| $C_{oss}$ | Output Capacitance | $V_{DS}$=10V | - | 14 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | f=1.0MHz | - | 10 | - | pF |

## Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Forward On Voltage[2] | $I_S$=0.13A, $V_{GS}$=0V | - | - | 1.2 | V |

### Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on min. copper pad of FR4 board

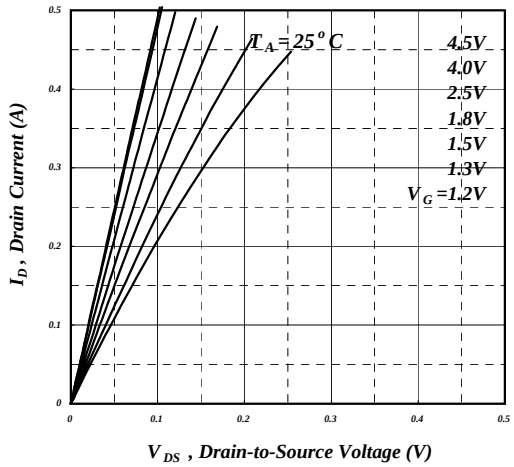



**Fig 1. Typical Output Characteristics**

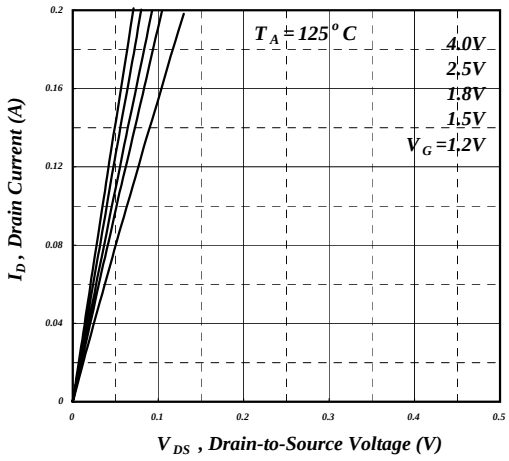



**Fig 2. Typical Output Characteristics**

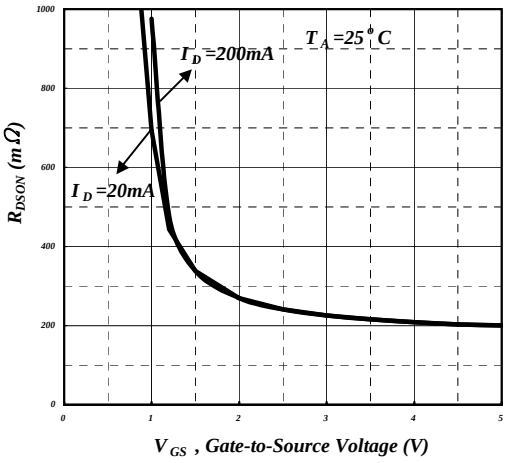



**Fig 3. On-Resistance v.s. Gate Voltage**

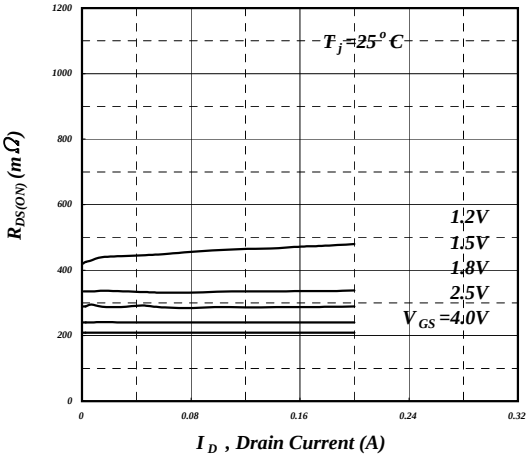



**Fig 4. Typ. Drain-Source on State Resistance**

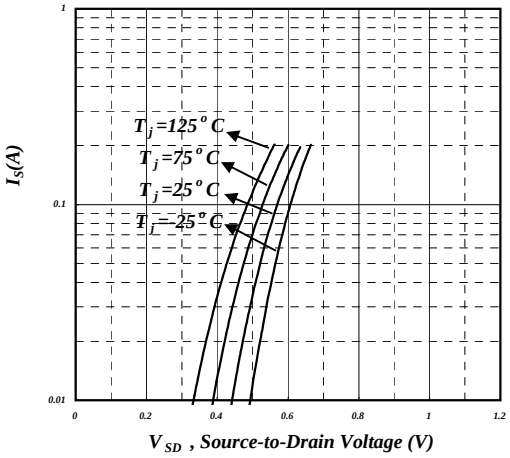



**Fig 5. Forward Characteristic of Reverse Diode**

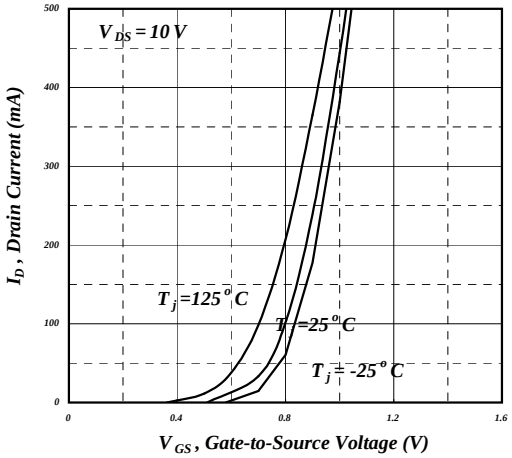



**Fig 6. Transfer Characteristics**

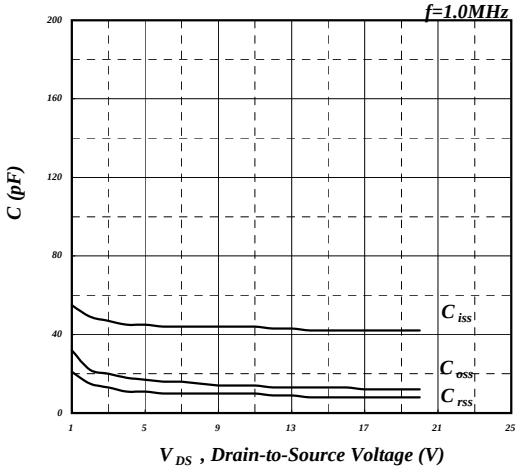



**Fig 7. Typical Capacitance Characteristics**

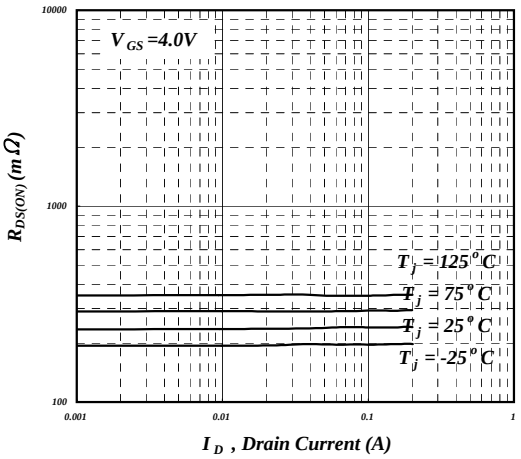



**Fig 8. Static Drain-Source On-State Resistance vs. Drain Current**

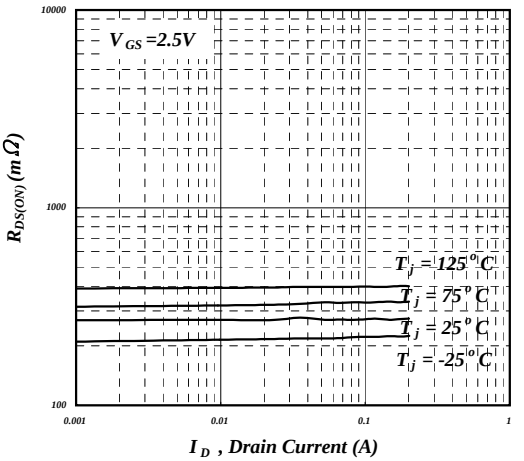



**Fig 9. Static Drain-Source On-State Resistance vs. Drain Current**

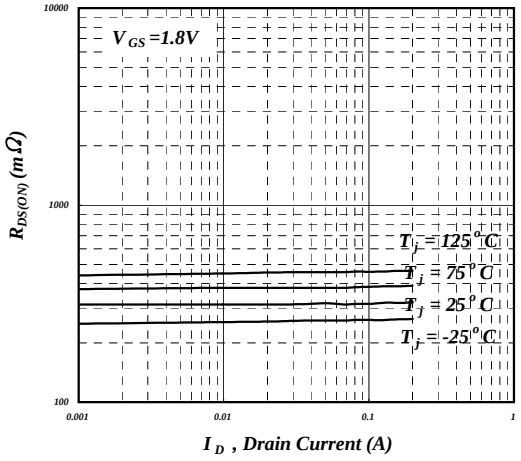



**Fig 10. Static Drain-Source On-State Resistance vs. Drain Current**

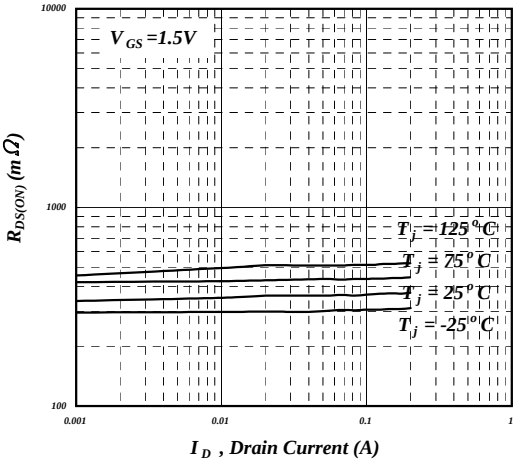



**Fig 11. Static Drain-Source On-State Resistance vs. Drain Current**

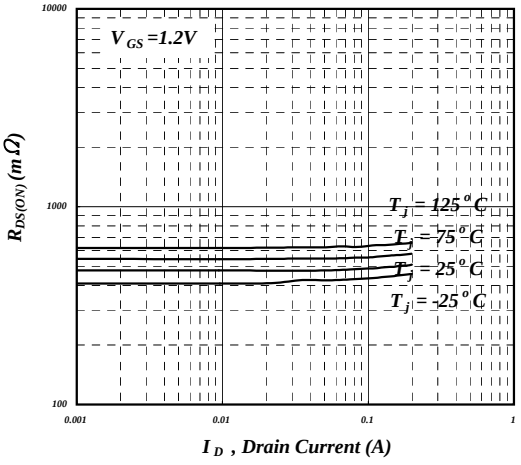



**Fig 12. Static Drain-Source On-State Resistance vs. Drain Current**