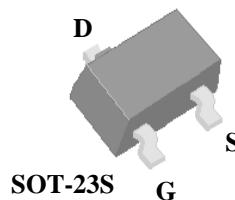
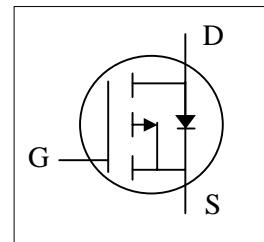




- ▼ Capable of 2.5V Gate Drive
- ▼ Small Package Outline
- ▼ Surface Mount Device
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	-20V
$R_{DS(ON)}$	65mΩ
I_D^3	-4.2A



Description

XP2P053 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SOT-23S package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_A = 25^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 4.5\text{V}$	-4.2	A
$I_D @ T_A = 70^\circ\text{C}$	Drain Current ³ , $V_{GS} @ 4.5\text{V}$	-3.4	A
I_{DM}	Pulsed Drain Current ¹	-16	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation ³	1.25	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	100	°C/W

Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=-250\mu\text{A}$	-20	-	-	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=-10\text{V}$, $I_{\text{D}}=-4.5\text{A}$	-	-	53	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}$, $I_{\text{D}}=-4\text{A}$	-	-	65	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}$, $I_{\text{D}}=-2\text{A}$	-	-	100	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=-250\mu\text{A}$	-0.5	-	-1.2	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=-5\text{V}$, $I_{\text{D}}=-3\text{A}$	-	9	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=-16\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}= \pm 12\text{V}$, $V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Q_{g}	Total Gate Charge	$I_{\text{D}}=-3\text{A}$	-	10	16	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=-10\text{V}$	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=-4.5\text{V}$	-	2	-	nC
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DS}}=-10\text{V}$	-	8	-	ns
t_{r}	Rise Time	$I_{\text{D}}=-1\text{A}$	-	12	-	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	$R_{\text{G}}=3.3\Omega$	-	24	-	ns
t_{f}	Fall Time	$V_{\text{GS}}=-5\text{V}$	-	38	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	1000	1600	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=-10\text{V}$	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=-1\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	$I_{\text{S}}=-3\text{A}$, $V_{\text{GS}}=0\text{V}$, $dI/dt=100\text{A}/\mu\text{s}$	-	12	-	ns
Q_{rr}	Reverse Recovery Charge		-	4	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{s}$; $300^\circ\text{C}/\text{W}$ when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT

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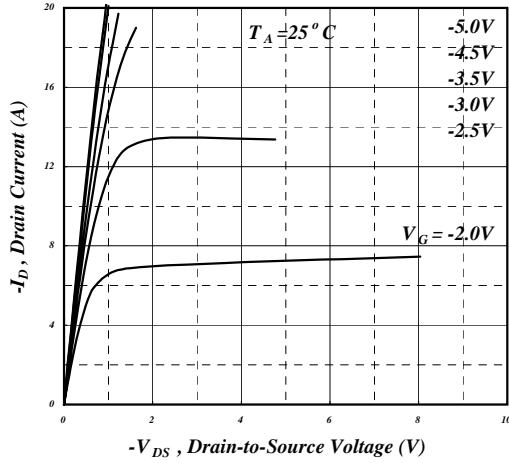


Fig 1. Typical Output Characteristics

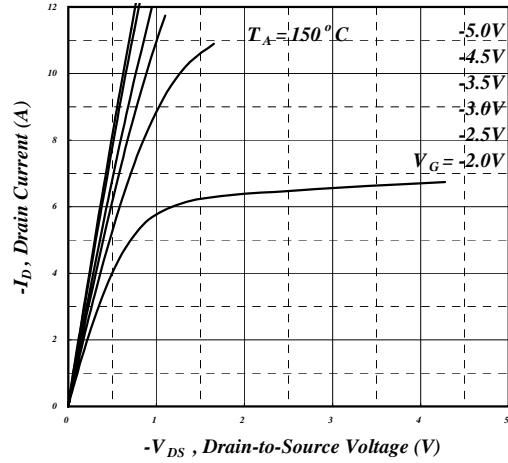


Fig 2. Typical Output Characteristics

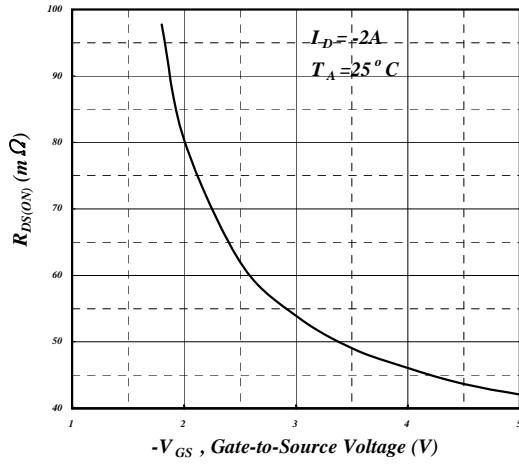


Fig 3. On-Resistance v.s. Gate Voltage

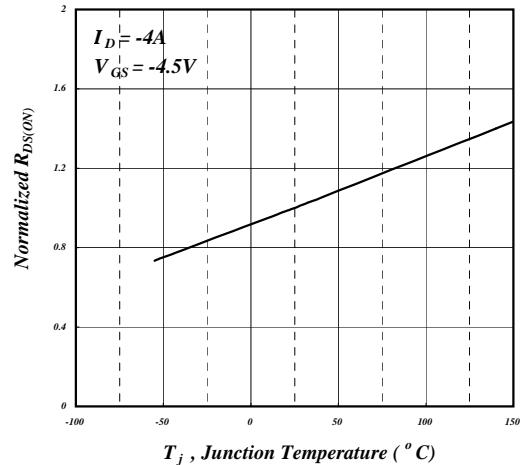


Fig 4. Normalized On-Resistance v.s. Junction Temperature

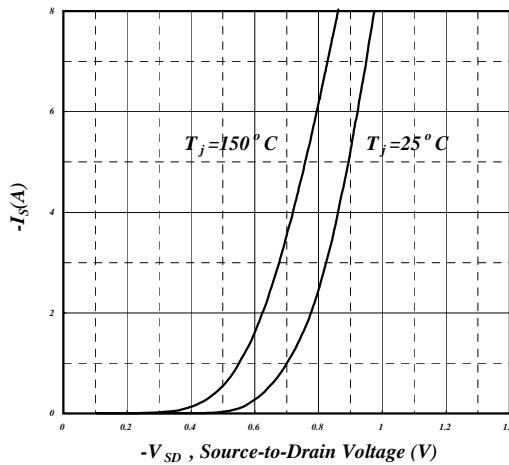


Fig 5. Forward Characteristic of Reverse Diode

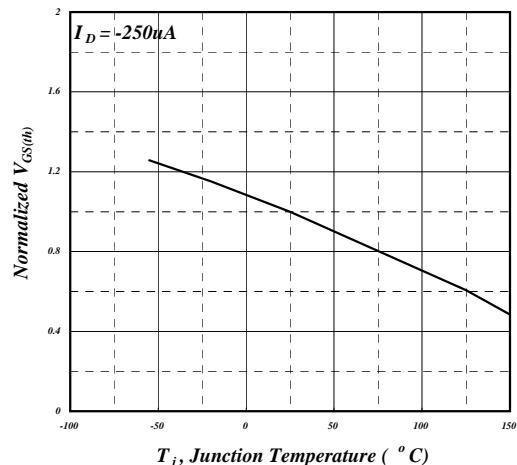
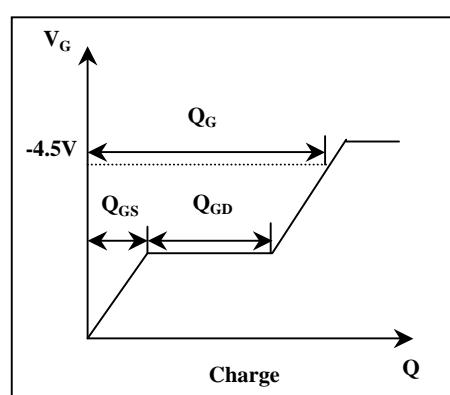
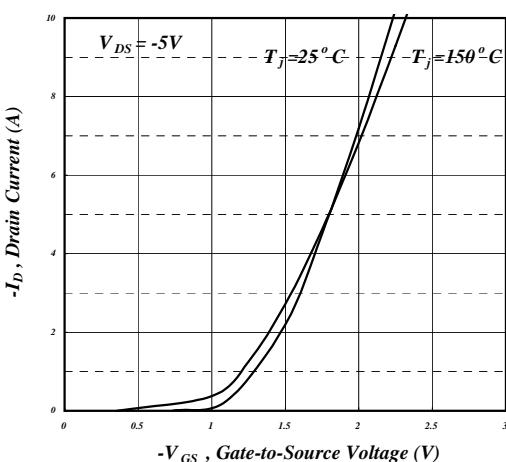
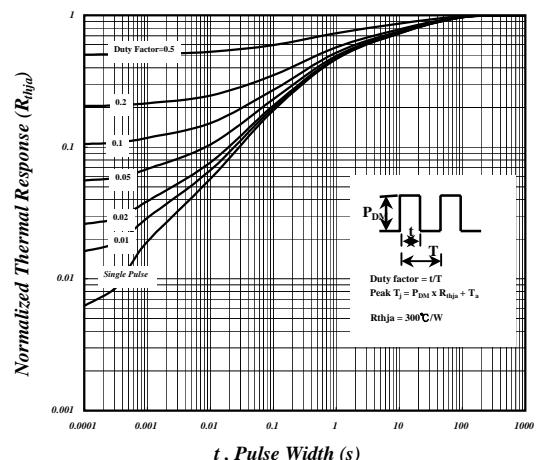
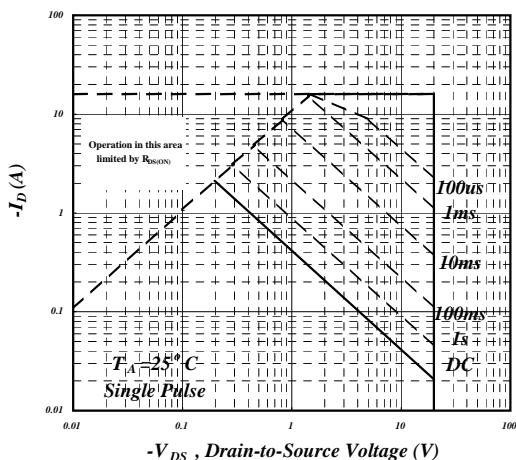
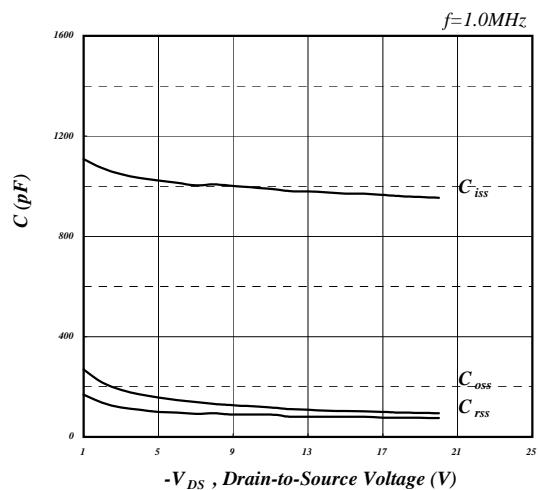
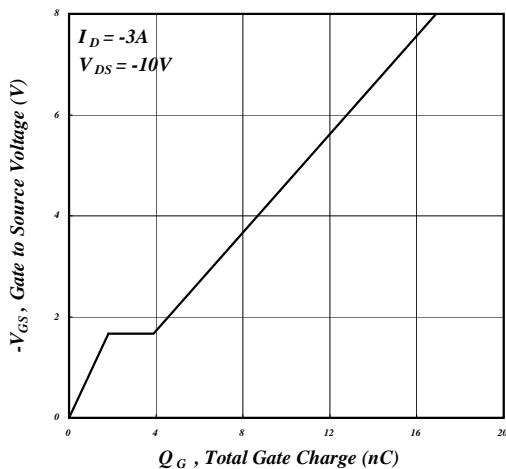


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



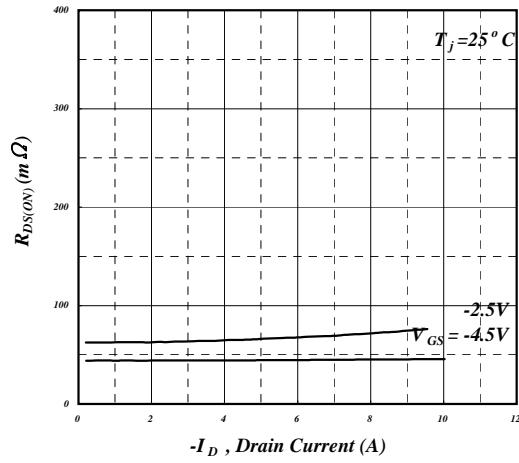


Fig 13. Typ. Drain-Source on State Resistance

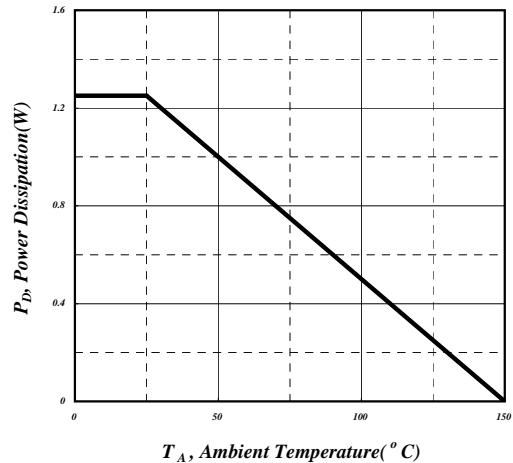


Fig 14. Total Power Dissipation