

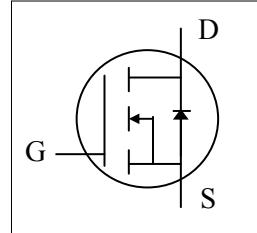


XP3N5R0AYT

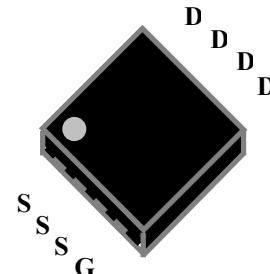
Halogen-Free Product

**N-CHANNEL ENHANCEMENT MODE
POWER MOSFET**

- ▼ Simple Drive Requirement
- ▼ Small Size & Ultra_Low $R_{DS(ON)}$
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	30V
$R_{DS(ON)}$	5mΩ



PM^{PAK}® 3 x 3

Description

XP3N5R0A series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK® 3 x 3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	<u>+20</u>	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^4$	63.5	A
$I_D @ T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	20	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	16	A
I_{DM}	Pulsed Drain Current ¹	120	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	3.12	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-c}	Maximum Thermal Resistance, Junction-case	4	°C/W
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	40	°C/W

Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=19\text{A}$	-	-	5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=12\text{A}$	-	-	9	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.3	-	2.3	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=19\text{A}$	-	58	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	10	uA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	+0.1	uA
$Q_g(10\text{V})$	Total Gate Charge	$I_{\text{D}}=19\text{A}$	-	40	64	nC
$Q_g(4.5\text{V})$	Total Gate Charge		-	21	33.6	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=15\text{V}$	-	7	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	10	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time		-	11	-	ns
t_r	Rise Time	$I_{\text{D}}=19\text{A}$	-	56	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	28	-	ns
t_f	Fall Time	$V_{\text{GS}}=10\text{V}$	-	8	-	ns
C_{iss}	Input Capacitance		-	1750	2800	pF
C_{oss}	Output Capacitance		-	300	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	250	-	pF
R_g	Gate Resistance		-	1.6	3.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_{\text{S}}=19\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V},$ $dI/dt=100\text{A}/\mu\text{s}$	-	12	-	ns
Q_{rr}	Reverse Recovery Charge		-	4	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² 2oz copper pad of FR4 board, t \leq 10sec; 135°C/W when mounted on min. copper pad.
- 4.Maximum current limited by package.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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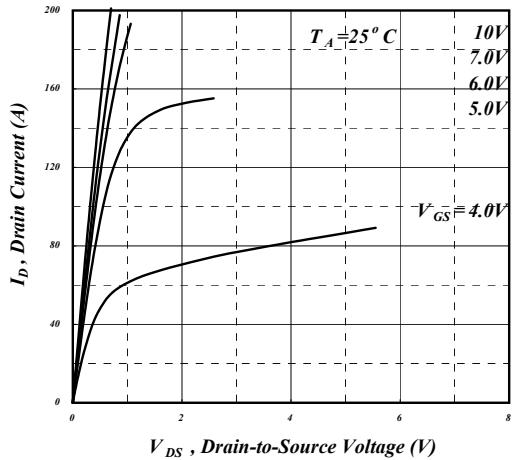


Fig 1. Typical Output Characteristics

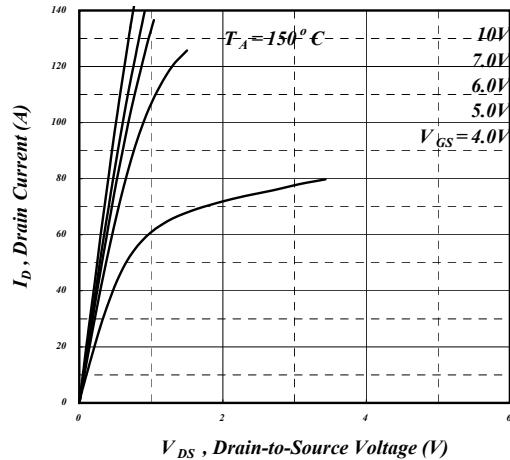


Fig 2. Typical Output Characteristics

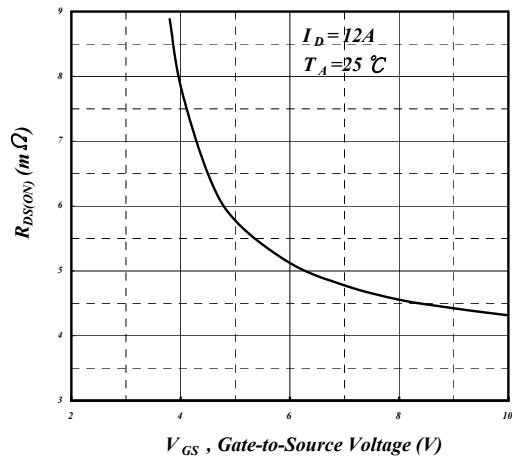


Fig 3. On-Resistance v.s. Gate Voltage

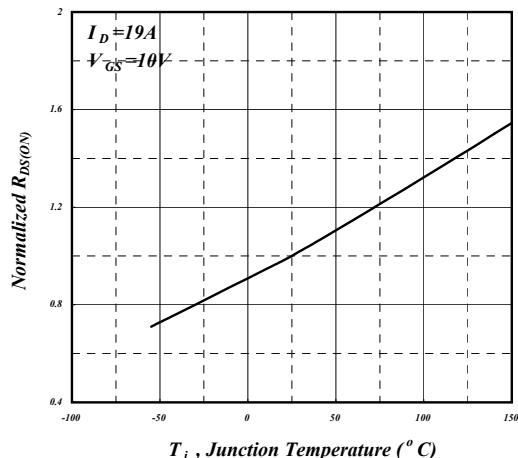


Fig 4. Normalized On-Resistance v.s. Junction Temperature

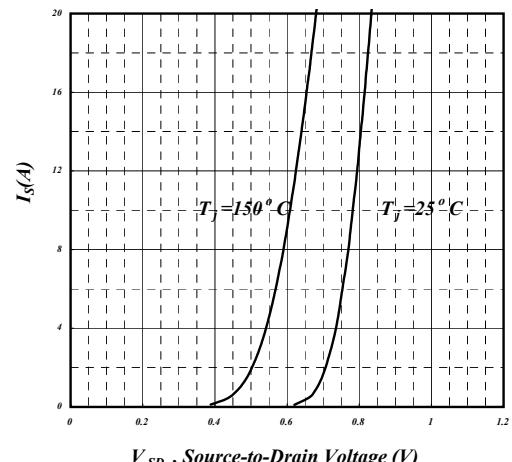


Fig 5. Forward Characteristic of Reverse Diode

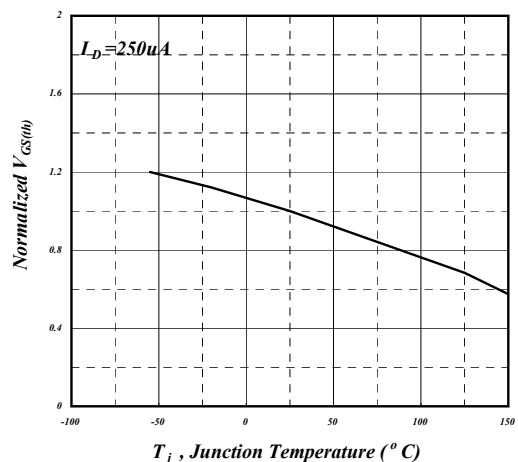
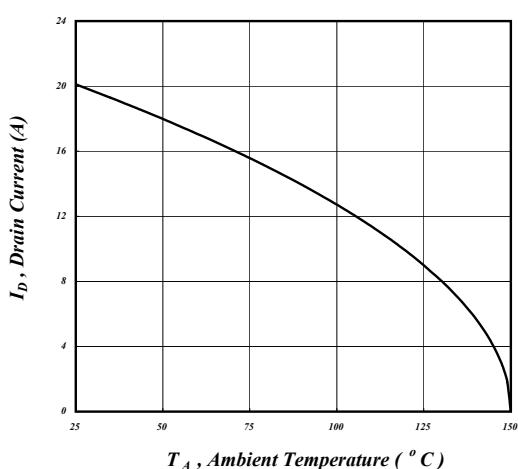
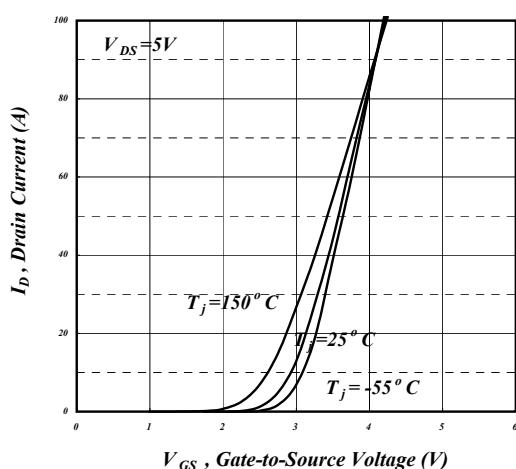
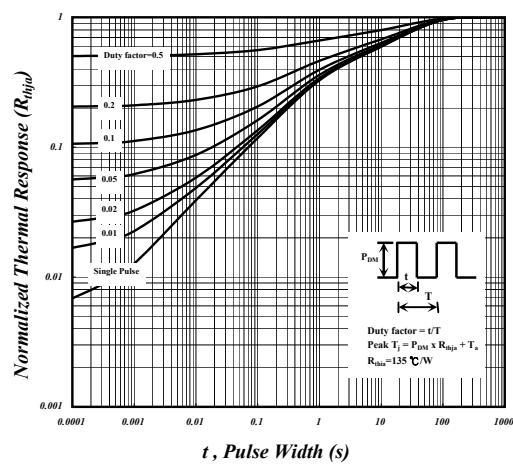
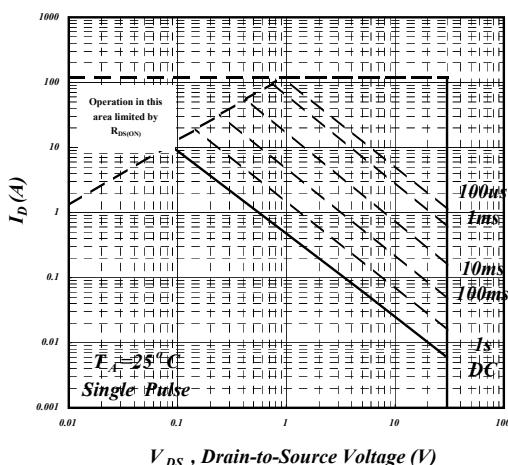
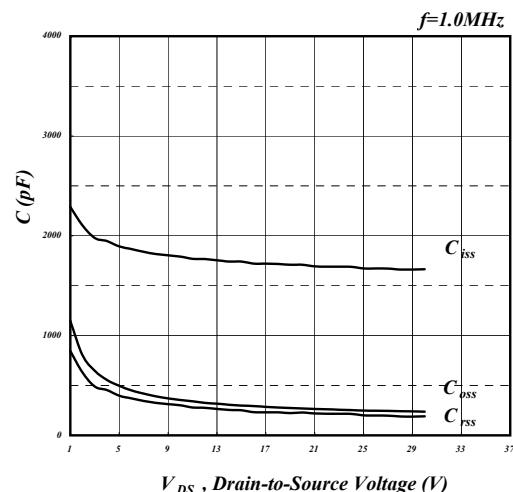
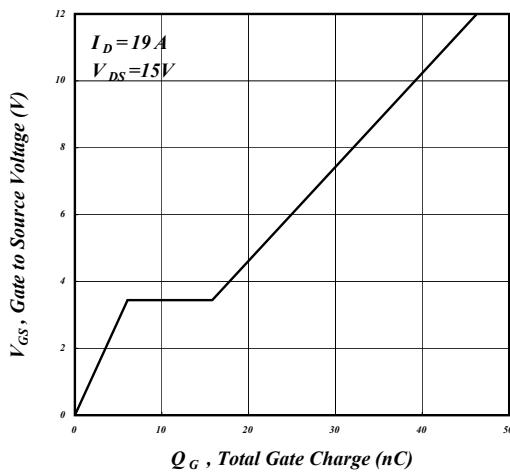


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



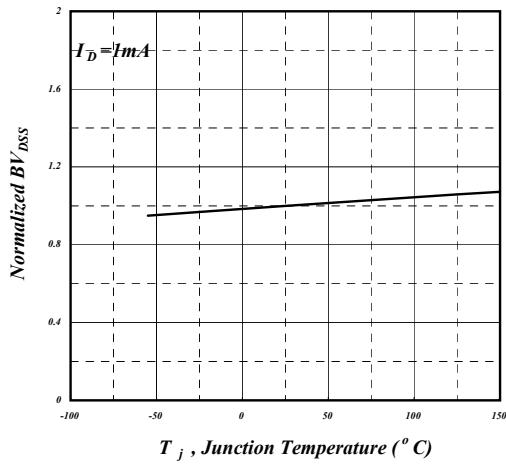


Fig 13. Normalized BV_{DSS} v.s. Junction

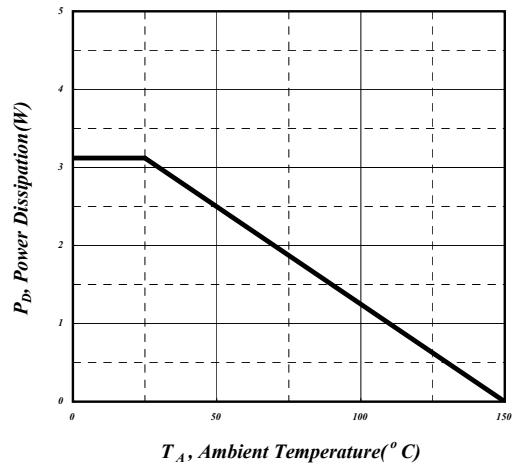


Fig 14. Total Power Dissipation

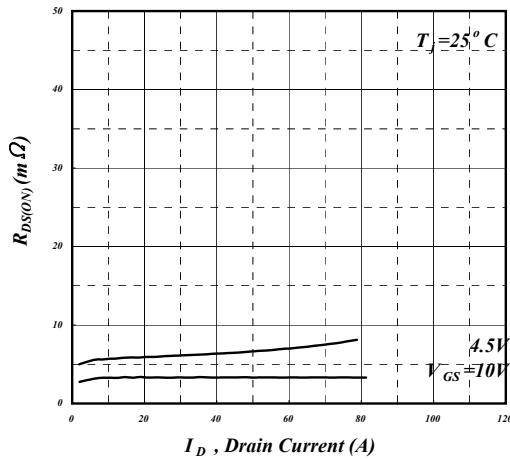


Fig 15. Typ. Drain-Source on State Resistance