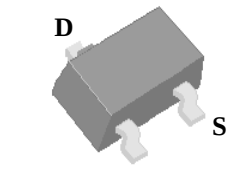
XP60PN72REN

Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Small Package Outline**
- ▼ **ESD Diode Protected**
- ▼ **RoHS Compliant & Halogen-Free**



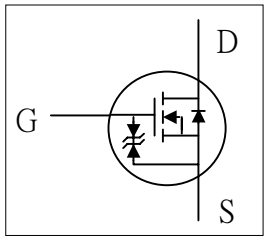
SOT-23

BV_{DSS}	600V
$R_{DS(ON)}$	72Ω
I_D	53mA
HBM ESD	2KV

Description

XP60PN72 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The special design SOT-23 package with good thermal performance is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for voltage conversion or switch applications.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current[3], V_{GS} @ 10V	53	mA
I_D@T_A=70℃	Drain Current[3], V_{GS} @ 10V	43	mA
I_{DM}	Pulsed Drain Current[1]	300	mA
P_D@T_A=25℃	Total Power Dissipation	0.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	250	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	600	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=50mA	-	-	72	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	5	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=50mA	-	200	-	mS
I_{DSS}	Drain-Source Leakage Current	V_{DS}=480V, V_{GS}=0V	-	-	100	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±30	uA
Q_g	Total Gate Charge[2]	I_D=0.1A	-	2.5	4	nC
Q_{gs}	Gate-Source Charge	V_{DS}=200V	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	0.3	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=300V	-	10	-	ns
t_r	Rise Time	I_D=50mA	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	14	-	ns
t_f	Fall Time	V_{GS}=10V	-	77	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	50	80	pF
C_{oss}	Output Capacitance	V_{DS}=100V	-	9	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=0.05A, V_{GS}=0V	-	-	1.5	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Mounted on min. copper pad FR4 board

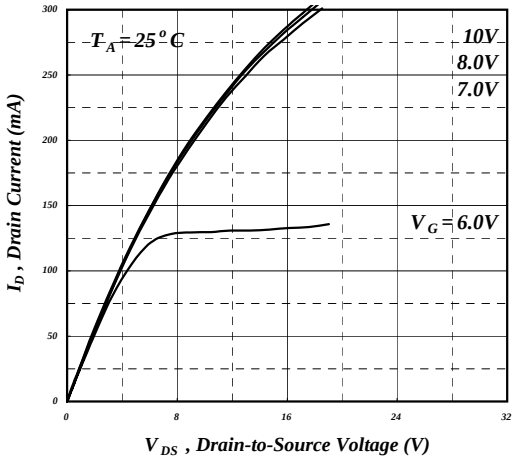


Fig 1. Typical Output Characteristics

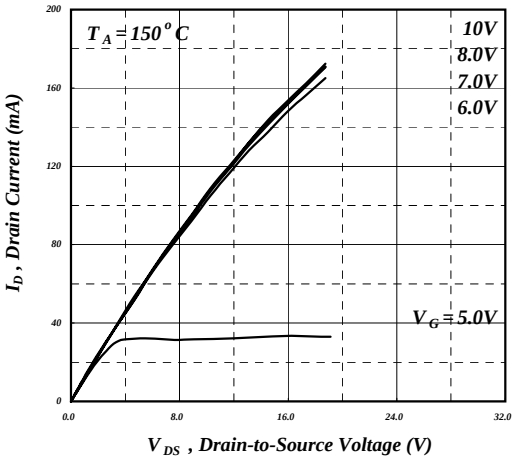


Fig 2. Typical Output Characteristics

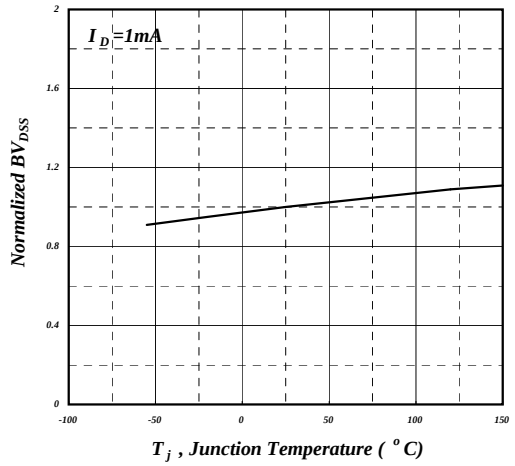


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

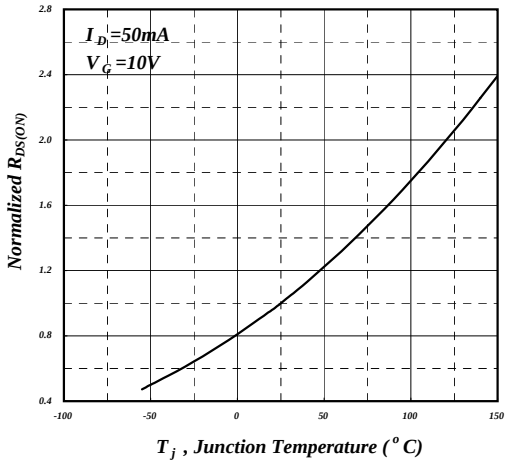


Fig 4. Normalized On-Resistance v.s. Junction Temperature

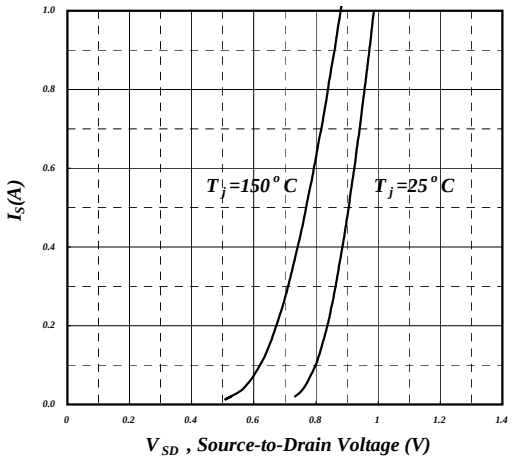


Fig 5. Forward Characteristic of Reverse Diode

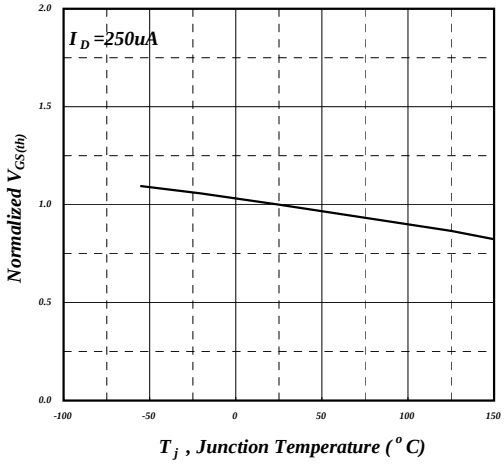


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

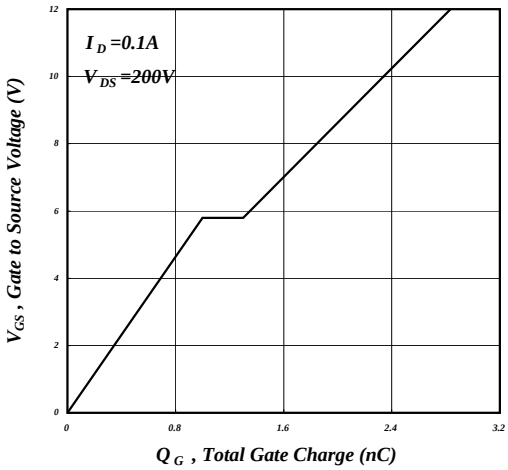


Fig 7. Gate Charge Characteristics

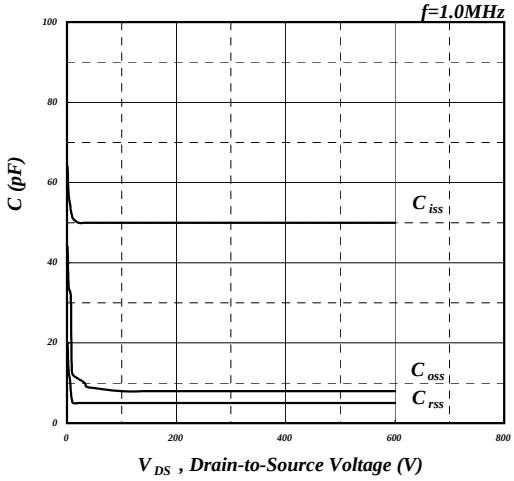


Fig 8. Typical Capacitance Characteristics

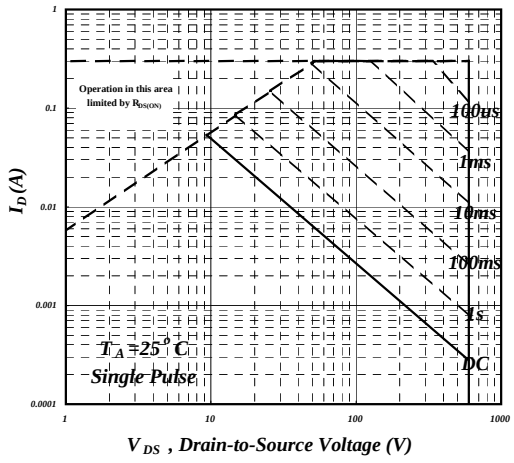


Fig 9. Maximum Safe Operating Area

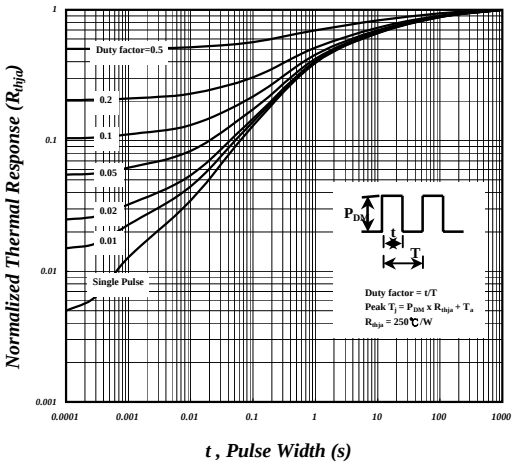


Fig 10. Effective Transient Thermal Impedance

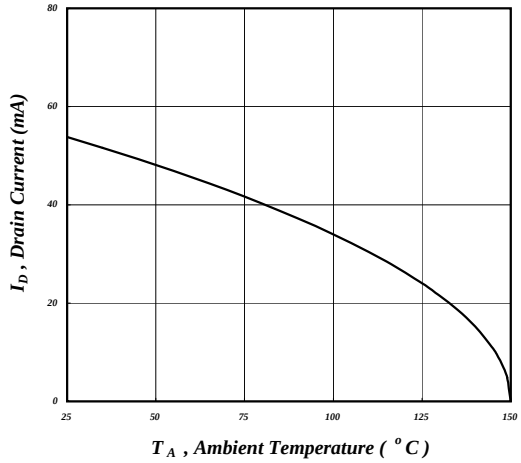


Fig 11. Drain Current v.s. Ambient Temperature

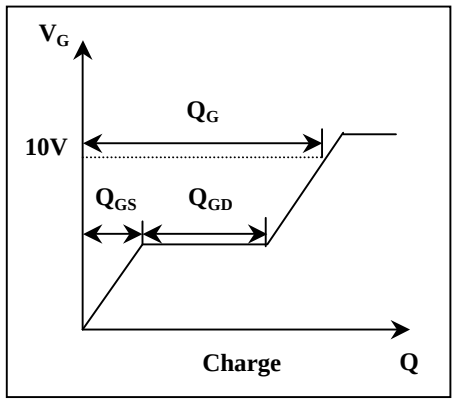


Fig 12. Gate Charge Circuit