

# XP60PN72RLEN

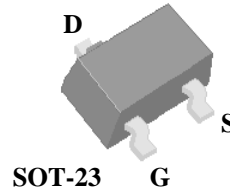
**Halogen-Free Product**



N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Simple Drive Requirement
- ▼ Small Package Outline
- ▼ ESD Diode Protected
- ▼ RoHS Compliant & Halogen-Free

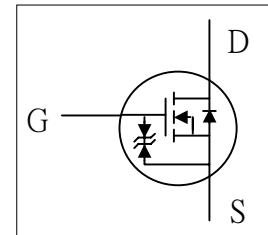


$BV_{DSS}$	600V
$R_{DS(ON)}$	72 $\Omega$
$I_D$	53mA
HBM ESD	2KV

## Description

XP60PN72 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The special design SOT-23 package with good thermal performance is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for voltage conversion or switch applications.



## Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	600	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	53	mA
$I_D @ T_A=70^\circ\text{C}$	Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	43	mA
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	300	mA
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	0.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	250	$^\circ\text{C}/\text{W}$

**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =1mA	600	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =50mA	-	-	72	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =16mA	-	-	150	Ω
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.4	-	2.6	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =20V, I <sub>D</sub> =50mA	-	240	-	mS
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =480V, V <sub>GS</sub> =0V	-	-	100	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±30	uA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =0.1A V <sub>DS</sub> =200V V <sub>GS</sub> =10V	-	2.3	3.7	nC
Q <sub>gs</sub>	Gate-Source Charge		-	0.5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge		-	0.5	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =300V I <sub>D</sub> =50mA	-	7	-	ns
t <sub>r</sub>	Rise Time		-	9	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω	-	17	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	78	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V V <sub>DS</sub> =100V f=1.0MHz	-	40	64	pF
C <sub>oss</sub>	Output Capacitance		-	9	-	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		-	5	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =0.05A, V <sub>GS</sub> =0V	-	-	1.5	V

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Mounted on min. copper pad FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT

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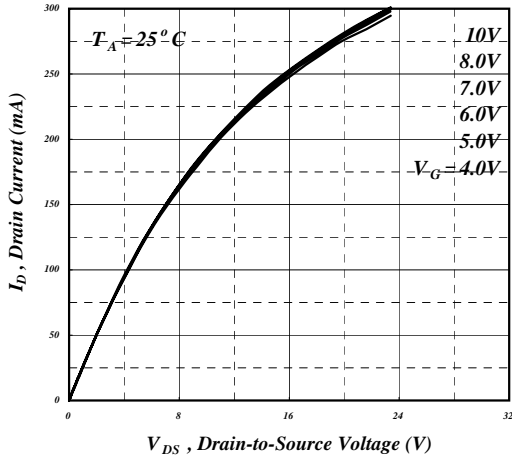


Fig 1. Typical Output Characteristics

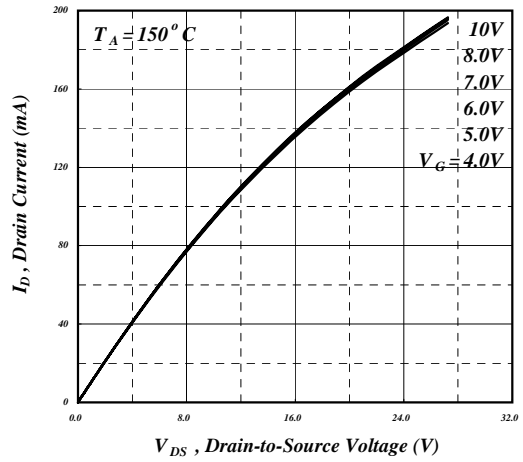


Fig 2. Typical Output Characteristics

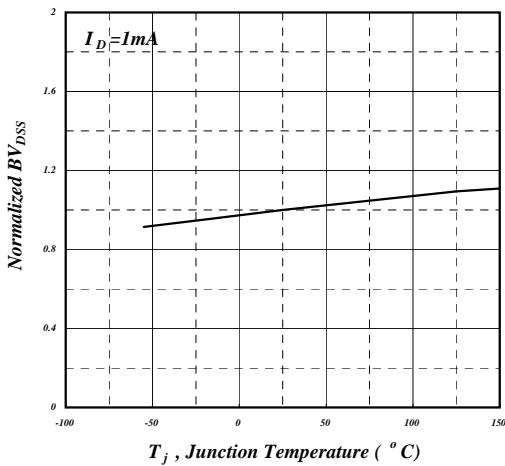


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

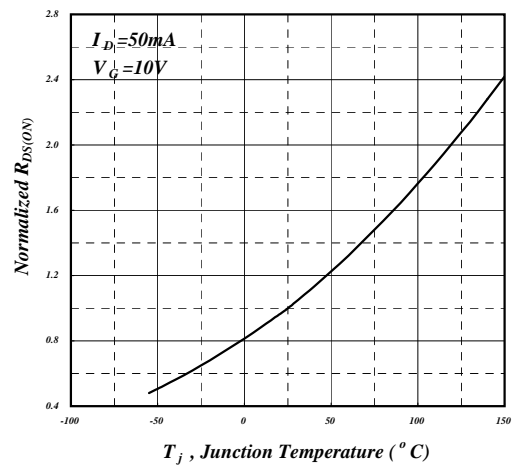


Fig 4. Normalized On-Resistance v.s. Junction Temperature

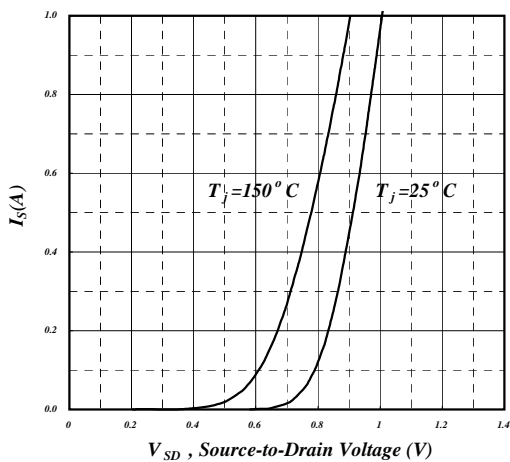


Fig 5. Forward Characteristic of Reverse Diode

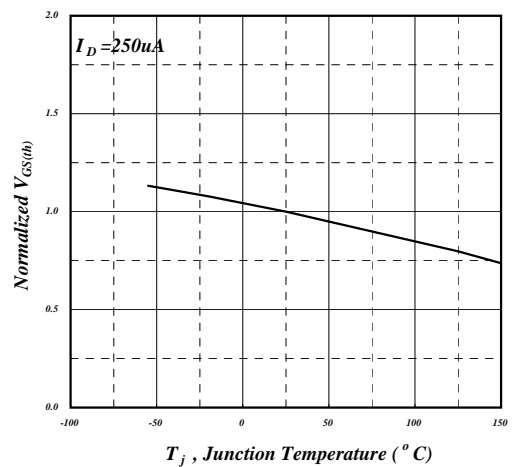
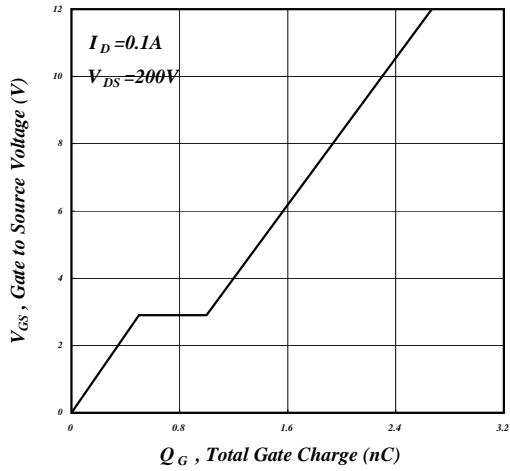
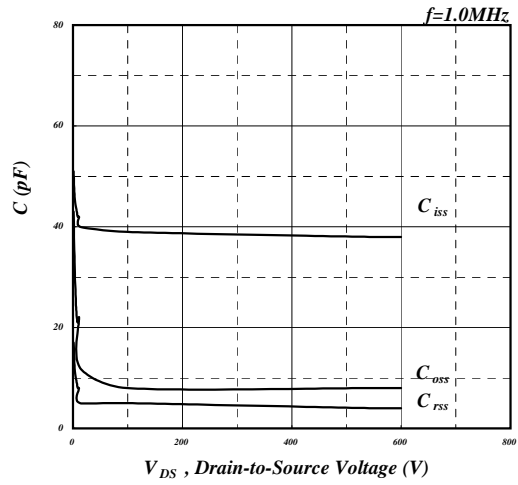


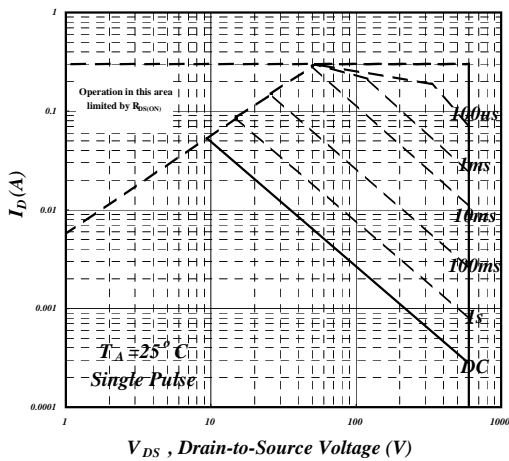
Fig 6. Gate Threshold Voltage v.s. Junction Temperature



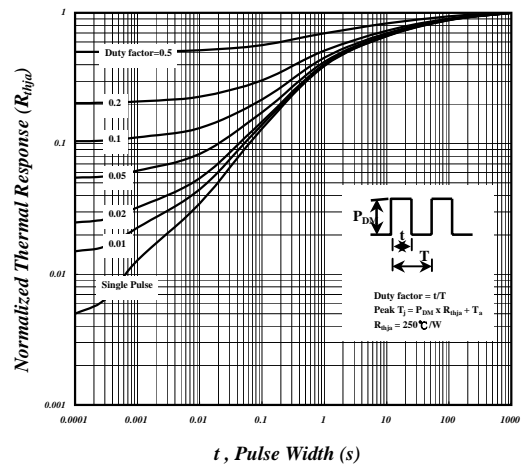
**Fig 7. Gate Charge Characteristics**



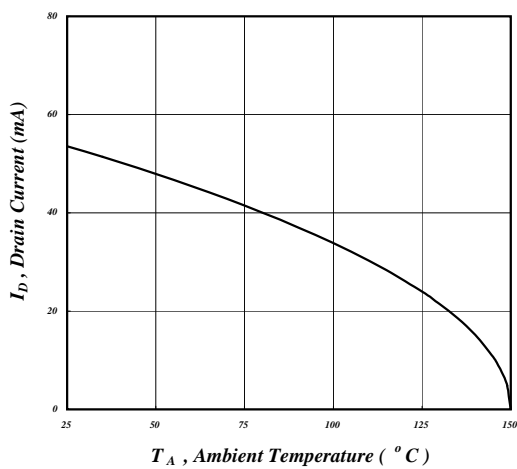
**Fig 8. Typical Capacitance Characteristics**



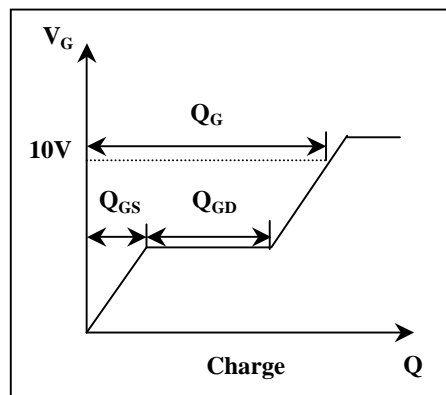
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Drain Current v.s. Ambient Temperature**



**Fig 12. Gate Charge Circuit**