

XP6NA3R0H

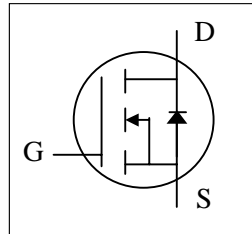
Halogen-Free Product

N-CHANNEL ENHANCEMENT MODE

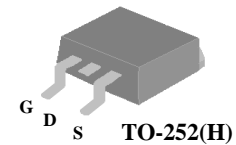
POWER MOSFET



- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	60V
R _{DS(ON)}	3mΩ



Description

XP6NA3R0 series are innovative design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	126	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Package Limited)	75	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ⁴ (Package Limited)	75	A
I _{DM}	Pulsed Drain Current ¹	400	A
P _D @T _C =25°C	Total Power Dissipation	83.3	W
P _D @T _A =25°C	Total Power Dissipation ³	2	W
E _{AS}	Single Pulse Avalanche Energy ⁶	173	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.5	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	62.5	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=40A$	-	-	3	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=40A$	-	100	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 0.1	μA
Q_g	Total Gate Charge ⁵	$I_D=40A$	-	70	112	nC
Q_{gs}	Gate-Source Charge ⁵	$V_{DS}=30V$	-	22	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁵	$V_{GS}=10V$	-	18	-	nC
$t_{d(on)}$	Turn-on Delay Time ⁵	$V_{DS}=30V$	-	22	-	ns
t_r	Rise Time ⁵	$I_D=40A$	-	75	-	ns
$t_{d(off)}$	Turn-off Delay Time ⁵	$R_G=7.5\Omega$	-	52	-	ns
t_f	Fall Time ⁵	$V_{GS}=10V$	-	88	-	ns
C_{iss}	Input Capacitance ⁵	$V_{GS}=0V$	-	4075	6520	pF
C_{oss}	Output Capacitance ⁵	$V_{DS}=50V$	-	650	-	pF
C_{rss}	Reverse Transfer Capacitance ⁵	$f=1.0\text{MHz}$	-	20	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	0.8	1.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=40A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time ⁵	$I_S=40A, V_{GS}=0V$	-	45	-	ns
Q_{rr}	Reverse Recovery Charge ⁵	$di/dt=100A/\mu s$	-	45	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board
4. Package limitation current is 75A .
5. Guaranteed by design.
6. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=0.3\text{mH}$, $R_G=25\Omega$, $V_{GS}=10V$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

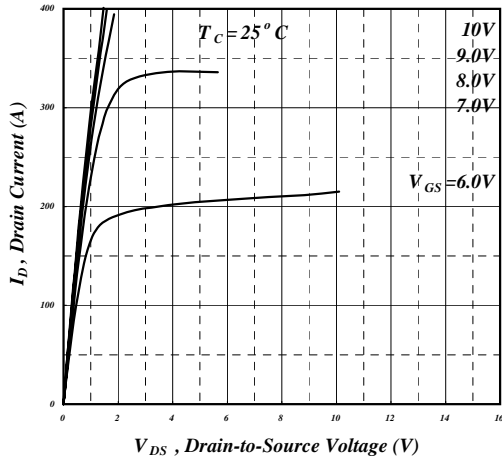


Fig 1. Typical Output Characteristics

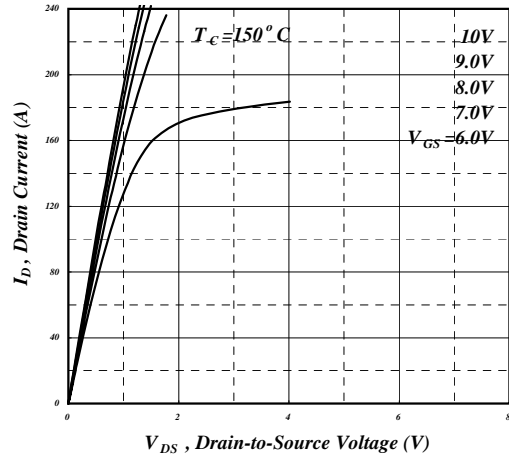


Fig 2. Typical Output Characteristics

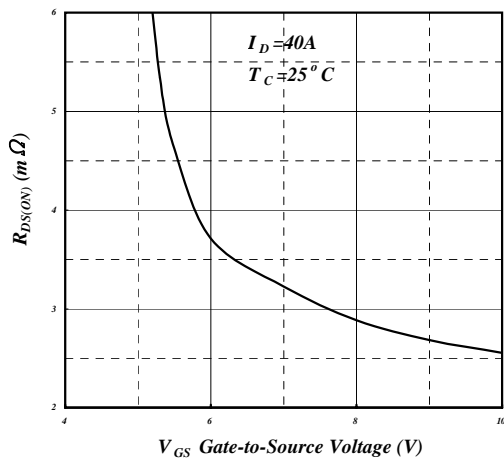


Fig 3. On-Resistance v.s. Gate Voltage

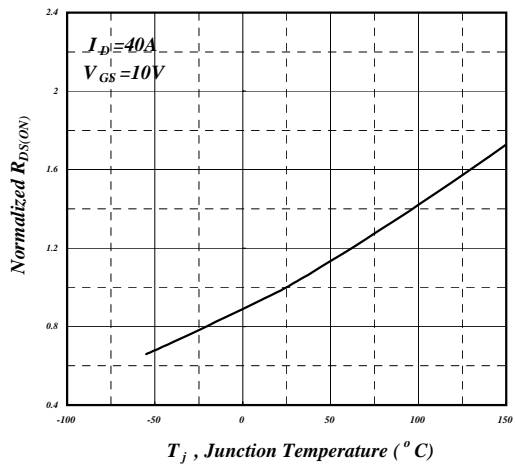


Fig 4. Normalized On-Resistance v.s. Junction Temperature

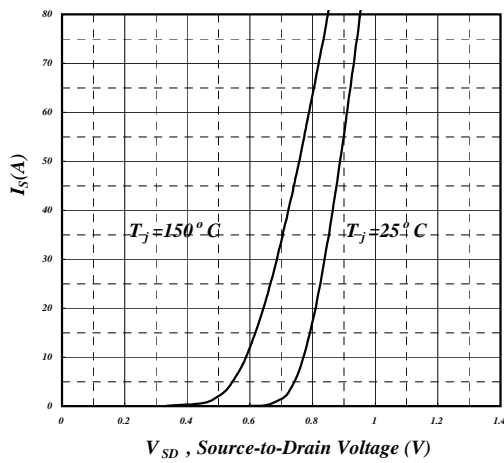


Fig 5. Forward Characteristic of Reverse Diode

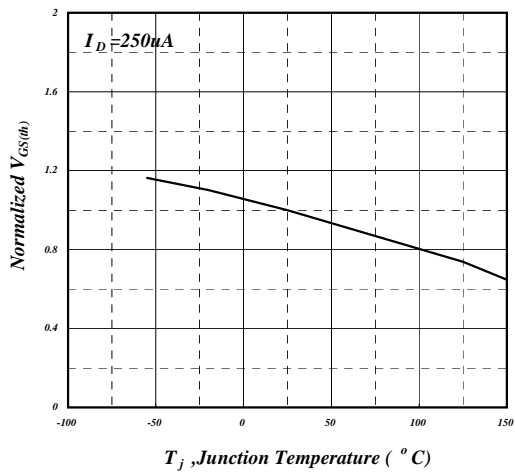


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

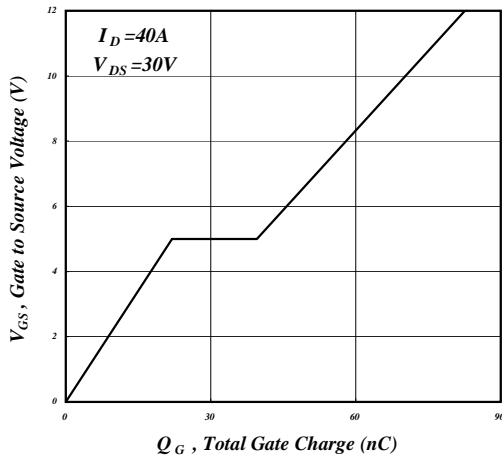


Fig 7. Gate Charge Characteristics

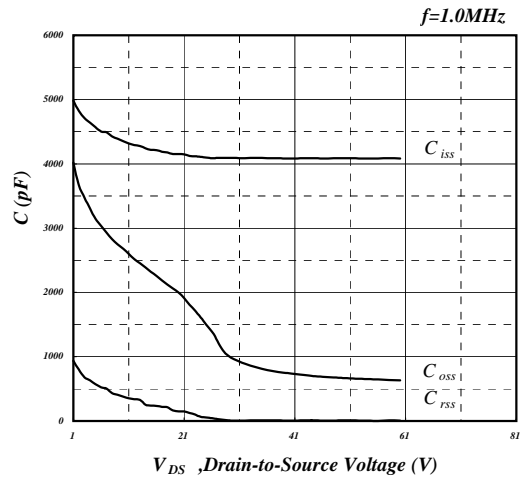


Fig 8. Typical Capacitance Characteristics

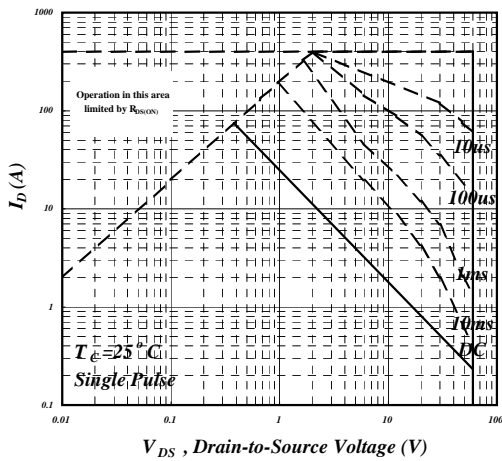


Fig 9. Maximum Safe Operating Area

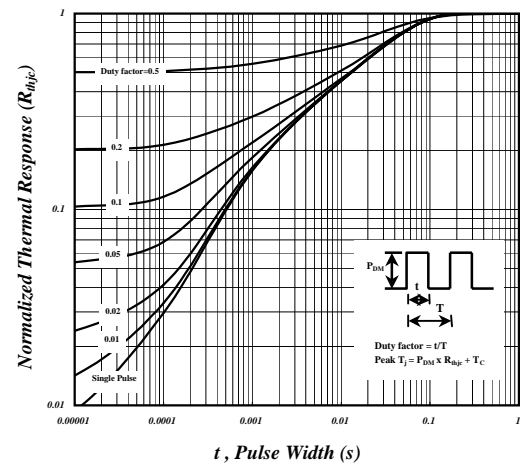


Fig 10. Effective Transient Thermal Impedance

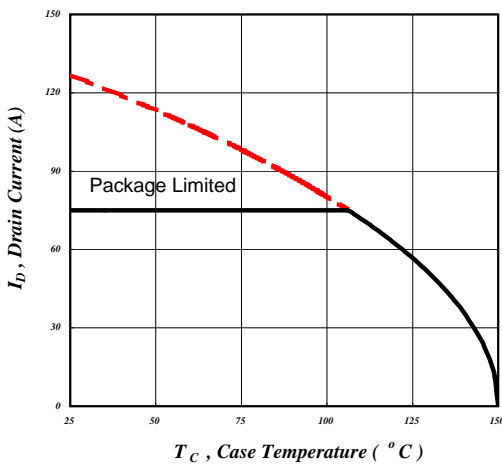


Fig 11. Drain Current v.s. Case Temperature

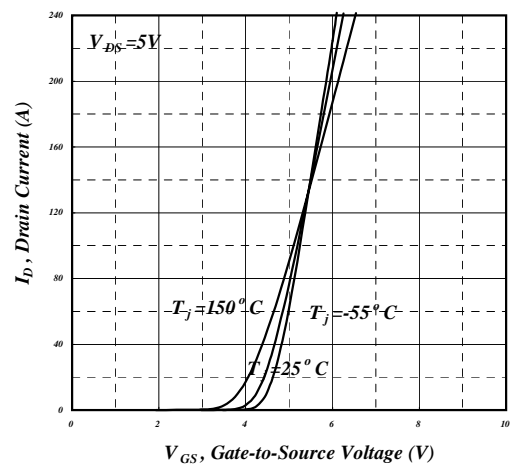


Fig 12. Transfer Characteristics

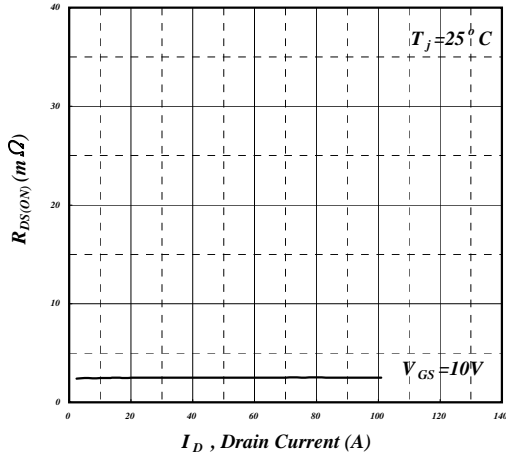


Fig 13. Typ. Drain-Source on State Resistance

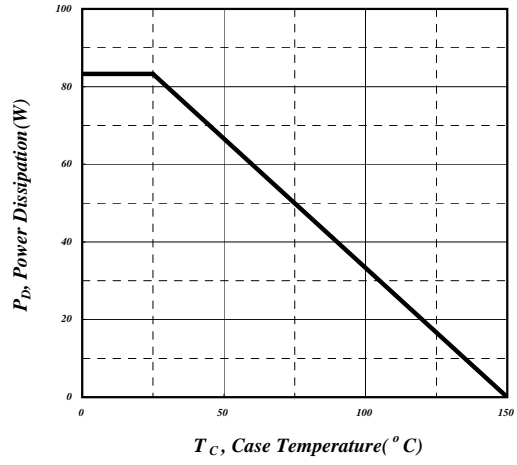


Fig 14. Total Power Dissipation

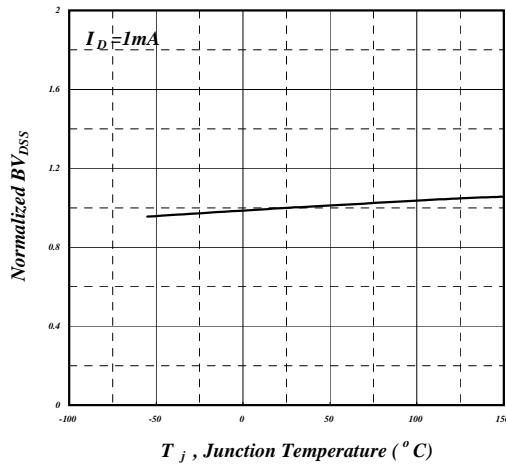


Fig 15. Normalized BV_{DS} v.s. Junction Temperature