5 GHz to 11 GHz GaAs, pHEMT, MMIC, Low Noise Amplifier

Data Sheet **HMC902LP3E**

FEATURES

- Low noise figure: 1.8 dB typical
- High gain: 19.5 dB
- High P1dB output power: 16 dBm typical
- Single supply: 3.5 V at 80 mA
- Output IP3: 28 dBm
- 50 Ω matched input/output
- Self biased with optional bias control for quiescent drain control (I_{DQ}) reduction.
- 3 mm × 3 mm, 16-lead LFCSP: 9 mm^2

APPLICATIONS

- Point to point radios
- Point to multi point radios
- Military and space
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

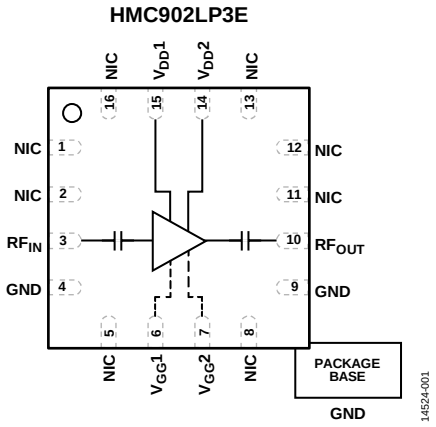

Figure 1.

GENERAL DESCRIPTION

The HMC902LP3E is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC) low noise amplifier (LNA), which is self biased with optional bias control for IDQ reduction. The HMC902LP3E is housed in a leadless 3 mm × 3 mm plastic surface mount package. The amplifier operates between 5 GHz and 11 GHz, providing 19.5 dB of small signal gain, 1.8 dB noise figure, and 28 dBm of output IP3, while requiring only 80 mA from a 3.5 V supply.

The P1dB output power of 16 dBm enables the LNA to function as a local oscillator (LO) driver for balanced, I/Q, or image reject mixers. The HMC902LP3E also features inputs/outputs that are dc blocked and internally matched to 50 Ω, making it ideal for high capacity microwave radios and C band, very small aperture terminal (VSAT) applications.

Rev. E
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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2/2018—Rev. D to Rev. E

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10/2017—Rev. C to Rev. D

Changes to Table 2 4

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

7/2017—Rev. 03.0816 to Rev. C

Updated Format ..... Universal
Changed HMC902 to HMC902LP3E ..... Throughout
Changes to Features Section, Applications Section, General Description Section, and Figure 1 1
Changes to Table 1 3
Changes to Figure 2 and Table 3 5
Changes to Typical Performance Characteristics Section 7
Added Theory of Operation Section and Figure 21; Renumbered Sequentially 10
Added Applications Information Section 11
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Added Application Circuit Section, Figure 23, and Figure 24 13
Updated Outline Dimensions 14
Changes to Ordering Guide 14

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, $V_{DD}1 = V_{DD}2$ = 3.5 V, I_{DQ} = 80 mA. $V_{GG}1 = V_{GG}2$ = open for normal, self biased operation.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		5		11	GHz	
GAIN[1]		17	19.5		dB	
Gain Variation over Temperature			0.01		dB/°C	
NOISE FIGURE[1]	NF		1.8	2.2	dB	
RETURN LOSS						
Input			12		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression[1]	P1dB		16		dBm	
Saturated Output Power[1]	P_{SAT}		17.5		dBm	
Output Third-Order Intercept	IP3		28		dBm	
SUPPLY CURRENT	I_{DQ}		80	110	mA	V_{DD} = 3.5 V, set $V_{GG}2$ = 0 V, $V_{GG}1$ = 0 V typical

[1] Board loss removed from gain, power, and noise figure measurement.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	4.5 V
Radio Frequency (RF) Input Power	10 dBm
Gate Bias Voltages	
$V_{GG}1$	−2 V to +0.2 V
$V_{GG}2$	−2 V to +0.2 V
Channel Temperature	150°C
Continuous Power Dissipation, P_{DISS} (T = 85°C, Derate 7 mW/°C Above 85°C)	0.45 W
Thermal Resistance (Channel to Ground Pad)	143.8°C/W
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1A, Passed 250 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

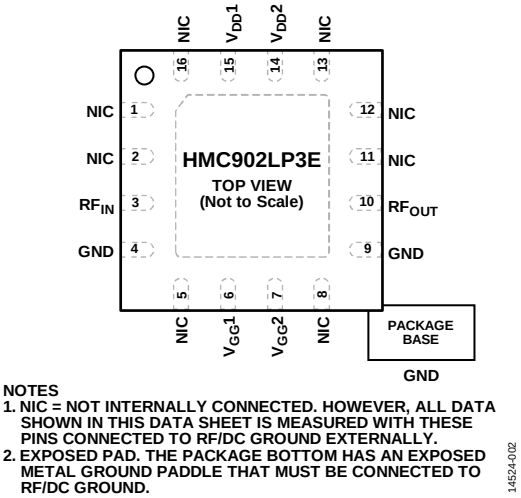

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 8, 11 to 13, 16	NIC	Not Internally Connected. However, all data shown in this data sheet is measured with these pins connected to RF/dc ground externally.
3	RF_{IN}	RF Input. This pin is ac-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
4, 9	GND	Ground. Connect these pins to RF/dc ground. See Figure 4 for the interface schematic.
6, 7	$V_{GG}1$, $V_{GG}2$	Optional Gate Control for Amplifier. If left open, the amplifier runs self biased at the standard current. Applying a negative voltage reduces drain current. External capacitors are required (see Figure 24). See Figure 5 for the interface schematic.
10	RF_{OUT}	RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
14, 15	$V_{DD}2$, $V_{DD}1$	Power Supply Voltage for the Amplifier. See Figure 23 and Figure 24 for the application circuits. See Figure 7 for the interface schematic.
	EPAD	Exposed Pad. The package bottom has an exposed metal ground paddle that must be connected to RF/dc ground.

INTERFACE SCHEMATICS

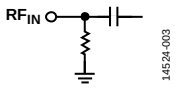

Figure 3. RF_{IN} Interface Schematic

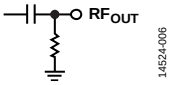

Figure 6. RF_{OUT} Interface Schematic

Figure 4. GND Interface Schematic

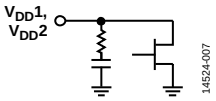

Figure 7. $V_{DD}1$ and $V_{DD}2$ Interface Schematic

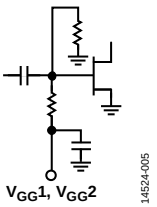

Figure 5. $V_{GG}1$ and $V_{GG}2$ Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

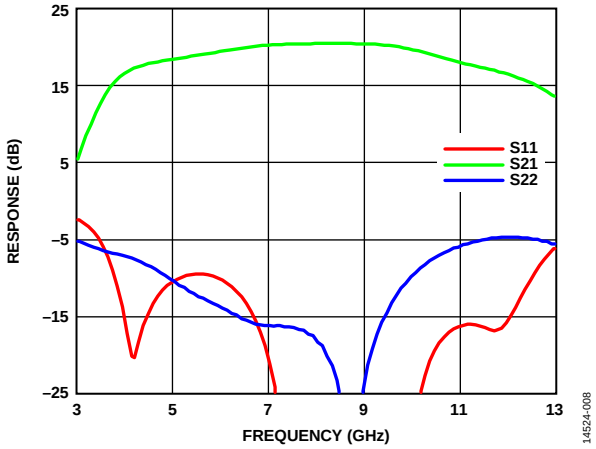

Figure 8. Broadband Gain and Return Loss vs. Frequency (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

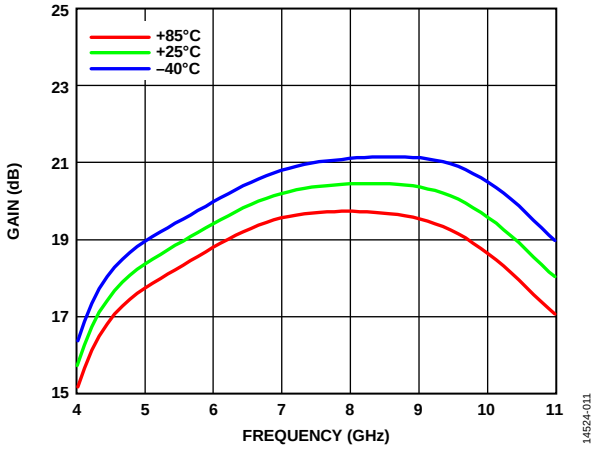

Figure 11. Gain vs. Frequency at Various Temperature (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

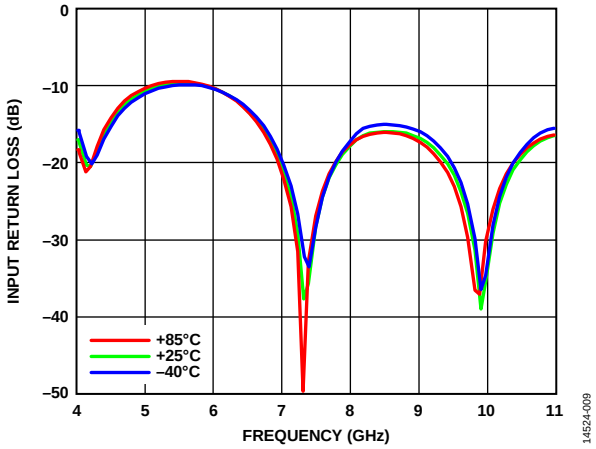

Figure 9. Input Return Loss vs. Frequency

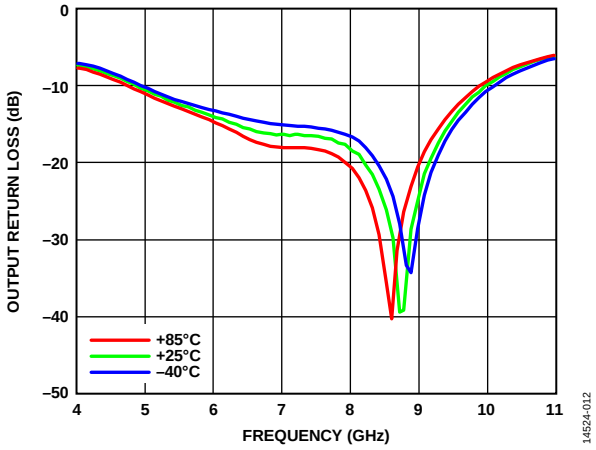

Figure 12. Output Return Loss vs. Frequency at Various Temperatures

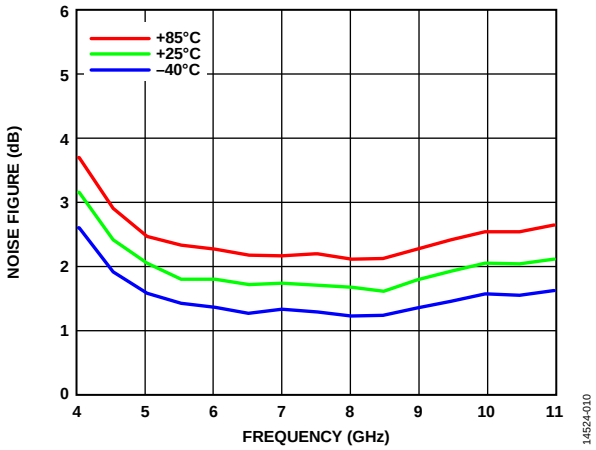

Figure 10. Noise Figure vs. Frequency at Various Temperature (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

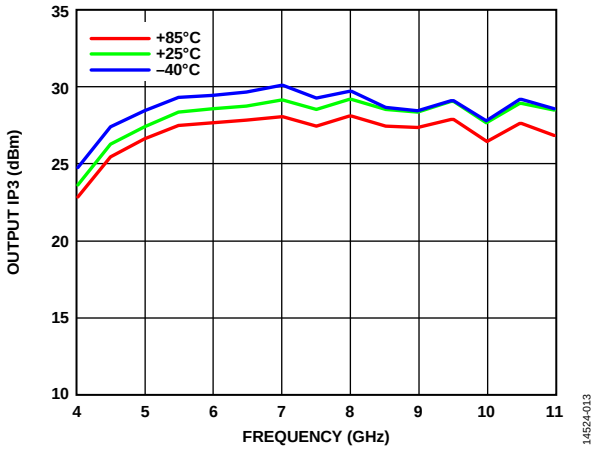

Figure 13. Output IP3 vs. Frequency at Various Temperatures

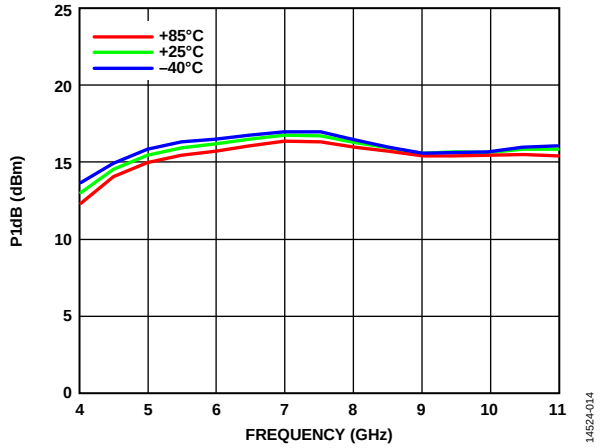

Figure 14. Output P1dB vs. Frequency at Various Temperatures (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

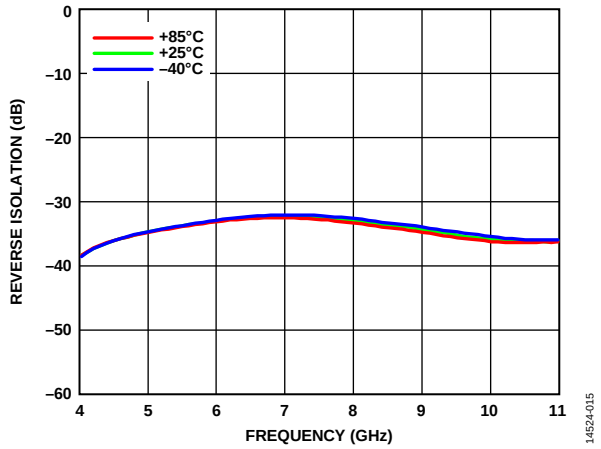

Figure 15. Reverse Isolation vs. Frequency at Various Temperatures

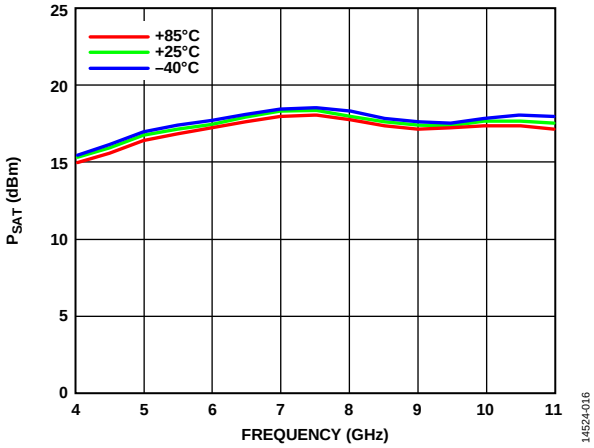

Figure 16. P_{SAT} vs Frequency at Various. Temperatures (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

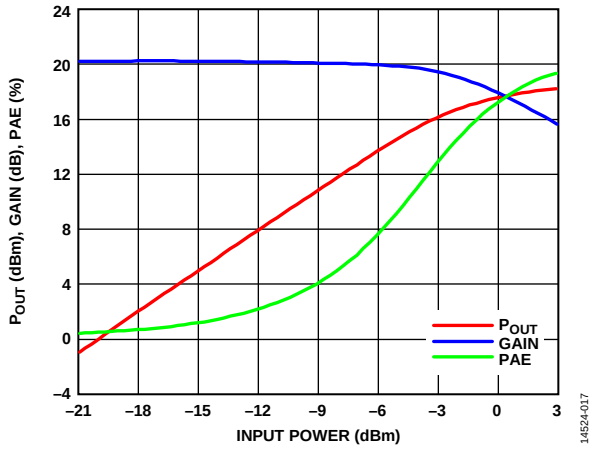

Figure 17. Output Power (P_{OUT}), Gain, and Power Added Efficiency (PAE) vs. Input Power (Board Loss Removed from Gain, Power, and Noise Figure Measurements)

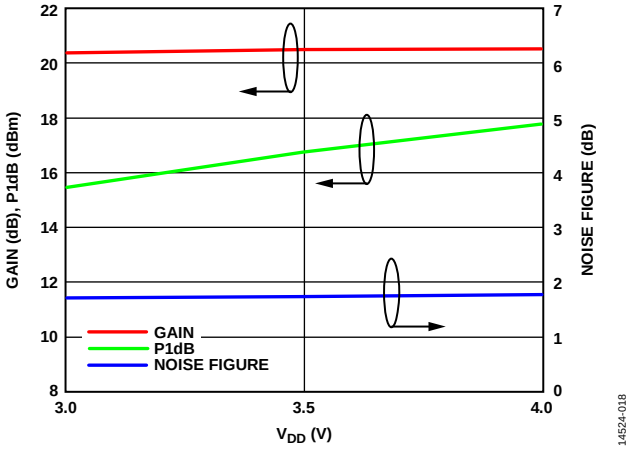

Figure 18. Gain, P1dB, and Noise Figure vs. Supply Voltage (V_{DD}) at 7 GHz (Board Loss Removed from Gain, Power and Noise Figure Measurement)

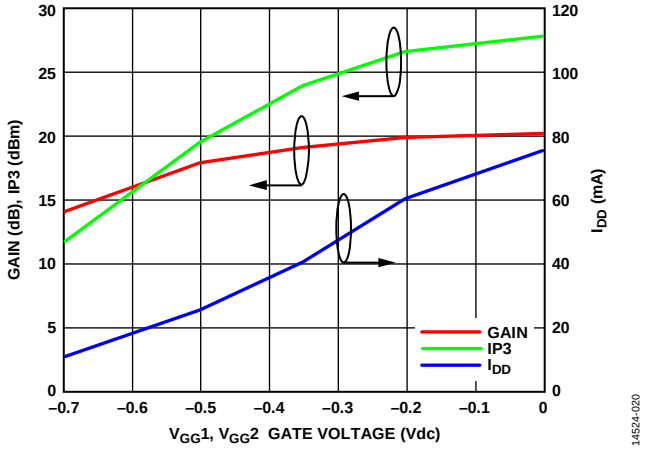

Figure 20. Gain, IP3, and I_{DD} vs. $V_{GG}1$, $V_{GG}2$ Gate Voltage at 7 GHz (Board Loss Removed from Gain Measurement, Data Taken at $V_{DD}1 = V_{DD}2 = 3$ V)

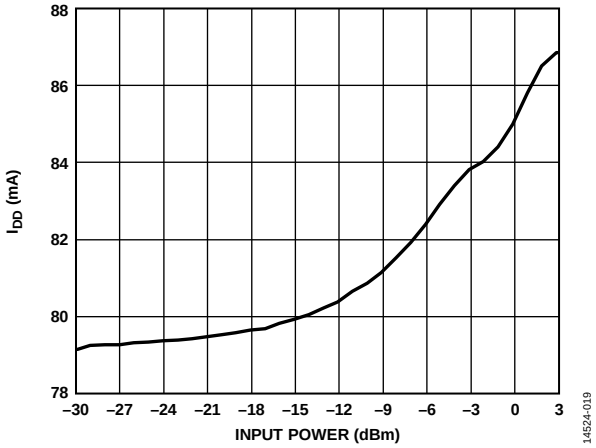

Figure 19. Supply Current (I_{DD}) vs. Input Power at 7 GHz

THEORY OF OPERATION

The HMC902LP3E is a GaAs, MMIC, pHEMT, LNA. The HMC902LP3E amplifier uses two gain stages in series. The basic schematic for the amplifier is shown in Figure 21, which forms a LNA operating from 5 GHz to 11 GHz with excellent noise figure performance.

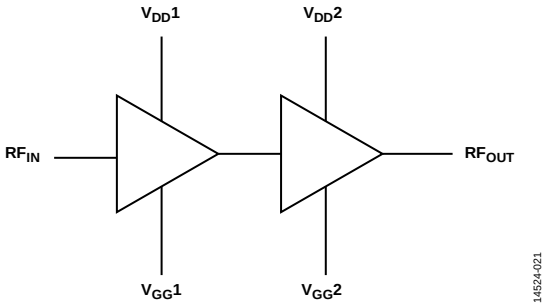

Figure 21. Basic Schematic for HMC902LP3E

The HMC902LP3E has single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 5 GHz to 11 GHz frequency range. Consequently, the device can be directly inserted into a 50 Ω system with no required impedance matching circuitry, which also means multiple HMC902LP3E amplifiers can be cascaded back to back without the need for external matching circuitry.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the package ground pad to ensure stable operation. To achieve optimal performance from the HMC902LP3E and to prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

The HMC902LP3E has $V_{GG}1$ and $V_{GG}2$ optional gate bias pins. When these pads are left open, the amplifier runs in self biased operation with typical I_{DQ} = 80 mA. Figure 23 shows the basic connections for operating the HMC902LP3E in self biased operation mode. Both RF_{IN} and RF_{OUT} ports of HMC902LP3E have on-chip dc block capacitors, eliminating the need for external ac coupling capacitors.

When using the optional $V_{GG}1$ and $V_{GG}2$ gate bias pins, use the recommended bias sequencing to prevent damage to the amplifier.

The recommended bias sequence during power-up is as follows:

1. Connect to GND.
2. Set $V_{GG}1$ and $V_{GG}2$ to −2.0 V.
3. Set $V_{DD}1$ and $V_{DD}2$ to 3.5 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to achieve typical I_{DQ} = 80 mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ and $V_{GG}2$ to −2.0 V to achieve typical I_{DQ} = 0 mA.
3. Decrease $V_{DD}1$ and $V_{DD}2$ to 0 V.
4. Increase $V_{GG}1$ and $V_{GG}2$ to 0 V.

The bias conditions previously listed (V_{DD} = 3.5 V and I_{DQ} = 80 mA) are the recommended operating points to achieve optimum performance. The data used in this data sheet was taken with the recommended bias conditions.

When using the HMC902LP3E with different bias conditions, different performance than what is shown in the Typical Performance Characteristics section can result. Decreasing the V_{DD} level has negligible effect on gain and NF performance, but reduces the P1dB, see Figure 18. For applications where the P1dB requirement is not stringent, the HMC902LP3E can be down biased to reduce power consumption.

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The evaluation PCB of the HMC902LP3E uses RF circuit design techniques. Signal lines must have 50 Ω impedance whereas the package ground leads and exposed paddle must be connected directly to the ground plane similar to that shown in Figure 22.

Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation board must be mounted to an appropriate heat sink. The evaluation PCB shown is available from Analog Devices, Inc., upon request.

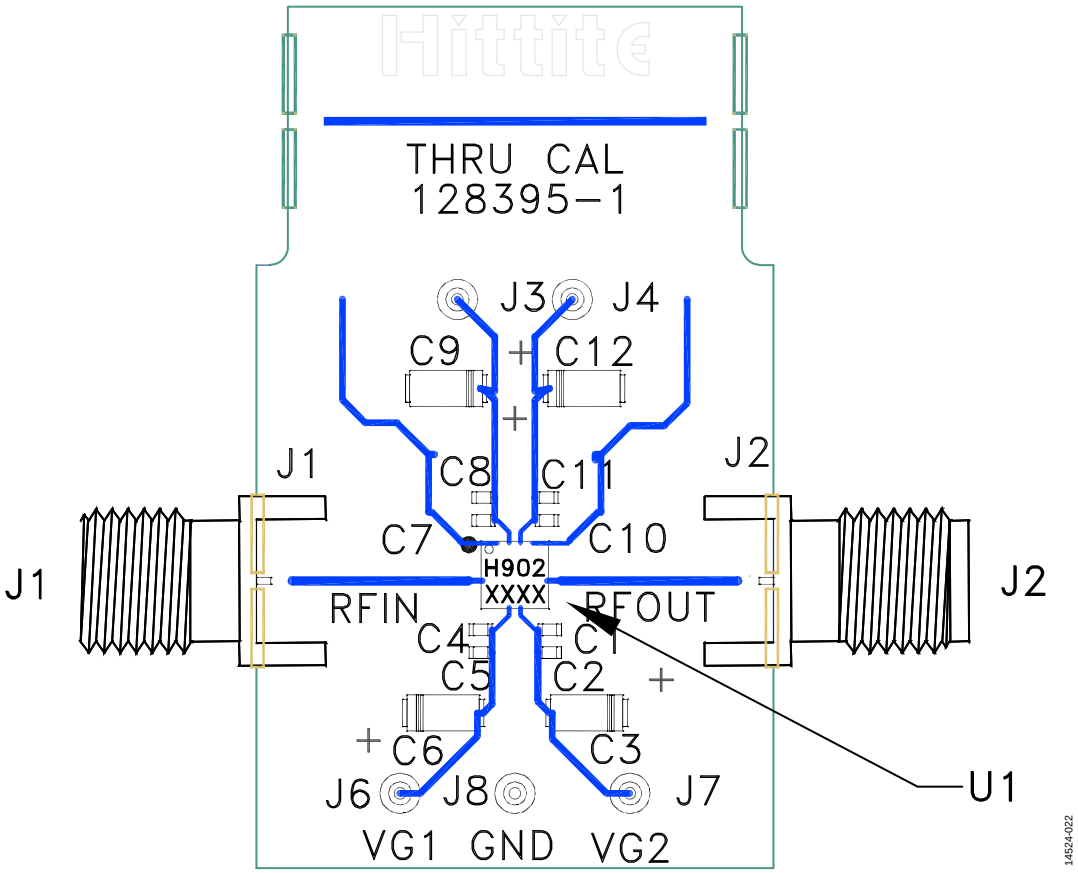

Figure 22. Evaluation PCB (128395-1)

Table 4. Bill of Materials for the Evaluation PCB

Item	Description
J1, J2	Subminiature Version A (SMA) connectors
J3, J4, J6 to J8	DC pins
C1, C4, C7, C10	100 pF capacitors, 0402 package
C2, C5, C8, C11	0.01 µF capacitors, 0402 package
C3, C6, C9, C12	4.7 µF tantalum capacitors
U1	HMC902LP3E amplifier
PCB	128395-1 evaluation PCB; circuit board material: Rogers 4350 or Arlon 25FR

APPLICATION CIRCUITS

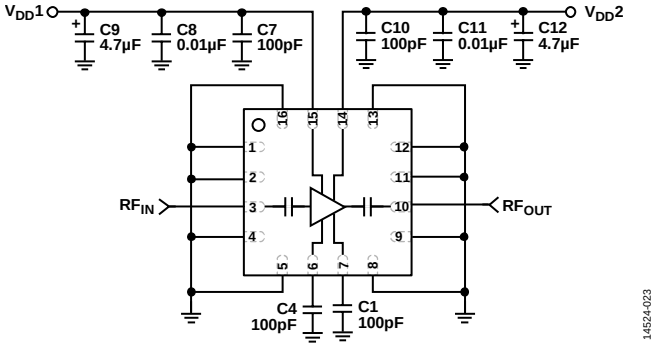

Figure 23. Standard (Self Biased) Operation

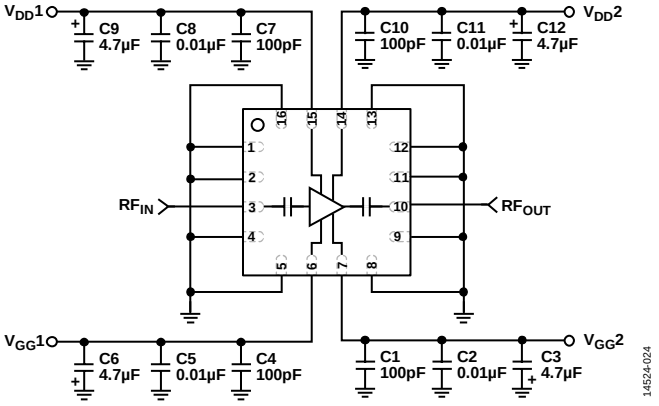

Figure 24. Gate Control, Reduced Current Operation