GaAs, pHEMT, MMIC, Single Positive Supply, DC to 7.5 GHz, 1 W Power Amplifier

Data Sheet

HMC637BPM5E

FEATURES

P1dB output power: 28 dBm typical
Gain: 15.5 dB typical
Output IP3: 39 dBm typical
Self biased at V_{DD} = 12 V at 345 mA typical
  Optional bias control on $V_{GG}1$ for I_{DQ} adjustment
  Optional bias control on $V_{GG}2$ for IP2 and IP3 optimization
50 Ω matched input/output
32-lead, 5 mm × 5 mm LFCSP package: 25 mm²

APPLICATIONS

Military and space
Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

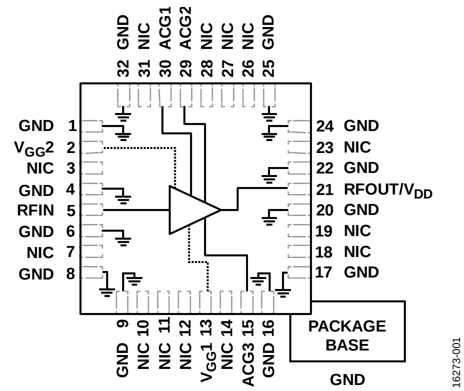

Figure 1.

GENERAL DESCRIPTION

The HMC637BPM5E is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), cascode distributed power amplifier. The device is self biased in normal operation and features optional bias control for quiescent current (I_{DQ}) adjustment and for second-order intercept (IP2) and third-order intercept (IP3) optimization. The amplifier operates from dc to 7.5 GHz, providing 15.5 dB of small signal gain, 28 dBm output power at 1 dB gain compression, a typical output IP3 of 39 dBm, and a 3.5 dB noise figure, while requiring 345 mA from a 12 V supply voltage (V_{DD}). Gain flatness is excellent from dc to 7.5 GHz at ±0.5 dB typical, making the HMC637BPM5E ideal for military, space, and test equipment applications. The HMC637BPM5E also features inputs/outputs (I/Os) that are internally matched to 50 Ω, housed in a RoHS-compliant, 5 mm × 5 mm, premolded cavity, lead frame chip scale package (LFCSP), making the device compatible with high volume, surface-mount technology (SMT) assembly equipment.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

8/2020—Rev. 0 to Rev. A

Changes to Figure 17 Caption ... 8
Added Figure 68; Renumbered Sequentially ... 16

5/2018—Revision 0: Initial Version

SPECIFICATIONS

FREQUENCY RANGE = DC TO 7.5 GHz

T_A = 25°C, V_{DD} = 12 V, I_{DQ} = 345 mA, $V_{GG}1$ = GND, $V_{GG}2$ = open, for nominal self biased operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		DC		7.5	GHz	
GAIN		12.5	15.5		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			±0.015		dB/°C	
NOISE FIGURE			3.5		dB	
RETURN LOSS						
Input			15		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	25	28		dBm	
Saturated Output Power	P_{SAT}		30.5		dBm	
Output Third-Order Intercept	IP3		39		dBm	Measurement taken at output power (P_{OUT})/tone = 10 dBm
SUPPLY						
Current	I_{DQ}		345		mA	For the external bias condition, adjust the gate bias voltage ($V_{GG}1$) between −2 V up to +0.5 V to achieve the desired quiescent current (I_{DQ})
Voltage	V_{DD}	8	12	13	V	

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter[1]	Rating
Drain Bias Voltage (V_{DD})	14 V
Gate 1 Voltage ($V_{GG}1$)	−2 V to +1 V
Gate 2 Voltage ($V_{GG}2$)	3.5 V to 7 V
Radio Frequency (RF) Input Power (RFIN)	25 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 63.29 mW/°C Above 85°C)	5.7 W
Output Load Voltage Standing Wave Ratio (VSWR)	7:1
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Maximum Peak Reflow Temperature	260°C
ESD Sensitivity	
Human Body Model (HBM)	Class 1C
Junction Temperature to Maintain 1 Million Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T = 85°C, V_{DD} = 12 V)	148.52°C

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of the multifunction pins, refer to the Pin Configuration and Function Descriptions section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package	θ_{JC}	Unit
CG-32-2[1]	15.8	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 36 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

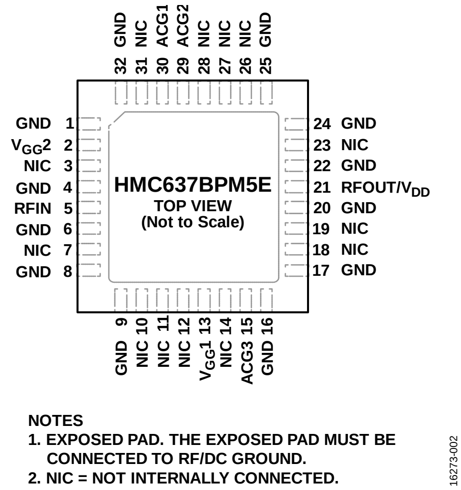


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground. These pins and the exposed pad must be connected to RF/dc ground.
2	$V_{GG}2$	Gate Control 2 for the Amplifier. $V_{GG}2$ is left open for self biased mode. Adjusting the voltage controls the gain response. External capacitors are required (see Figure 70). See Figure 7 for the interface schematic.
3, 7, 10 to 12, 14, 18, 19, 23, 26 to 28, 31	NIC	Not Internally Connected. These pins must be connected to RF/dc ground.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
13	$V_{GG}1$	Optional Gate Control for the Amplifier. If this pin is grounded, the amplifier runs in self biased mode at the standard current of 345 mA. Adjusting the voltage above or below the ground potential controls the drain current. External capacitors are required (see Figure 70). See Figure 8 for the interface schematic.
15, 29, 30	ACG1, ACG2, ACG3	Low Frequency Termination. External bypass capacitors are required on these pins (see Figure 70). See Figure 4 and Figure 5 for the interface schematics.
21	RFOUT/V_{DD}	RF Output for the Amplifier (RFOUT).
		Drain Bias Voltage (V_{DD}). Connect the dc bias (V_{DD}) network to provide the drain current, I_{DD} (see Figure 70). See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

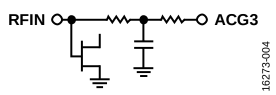


Figure 4. ACG3 Interface Schematic

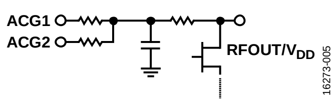


Figure 5. RFOUT/V_{DD}, ACG1, ACG2 Interface Schematic

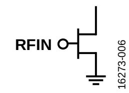


Figure 6. RFIN Interface Schematic

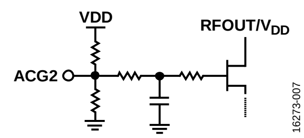


Figure 7. $V_{GG}2$ Interface Schematic

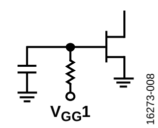


Figure 8. $V_{GG}1$ Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTIC

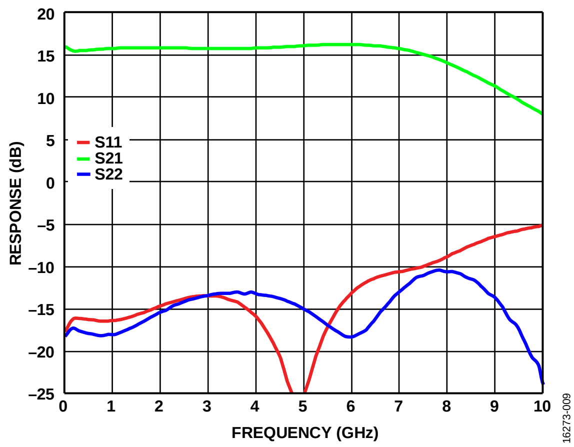


Figure 9. Gain and Return Loss Response vs. Frequency, Self Biased Mode, V_{DD} = 12 V, $V_{GG}1$ = GND, $V_{GG}2$ = Open

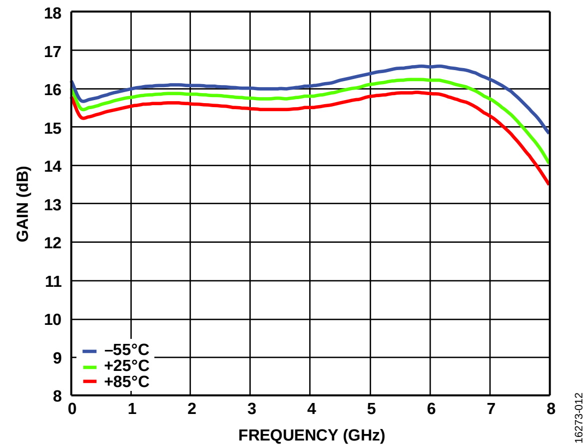


Figure 12. Gain vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, $V_{GG}1$ = GND, $V_{GG}2$ = Open

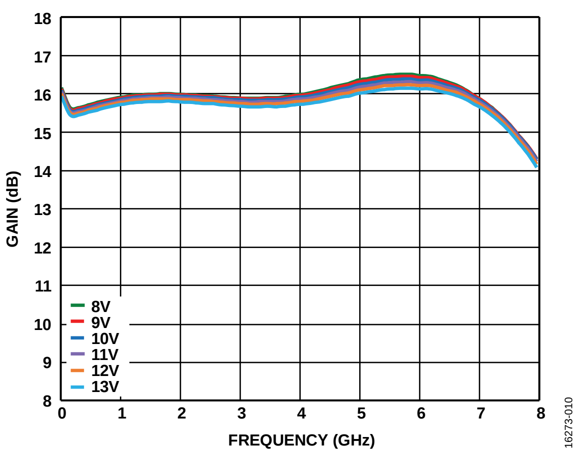


Figure 10. Gain vs. Frequency for Various Supply Voltages (V_{DD}), Self Biased Mode, $V_{GG}1$ = GND, $V_{GG}2$ = Open

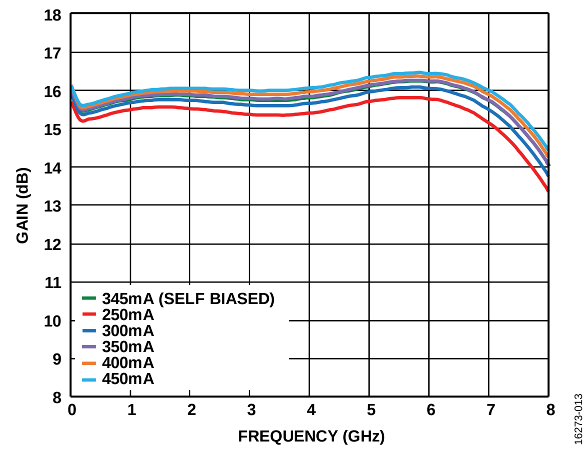
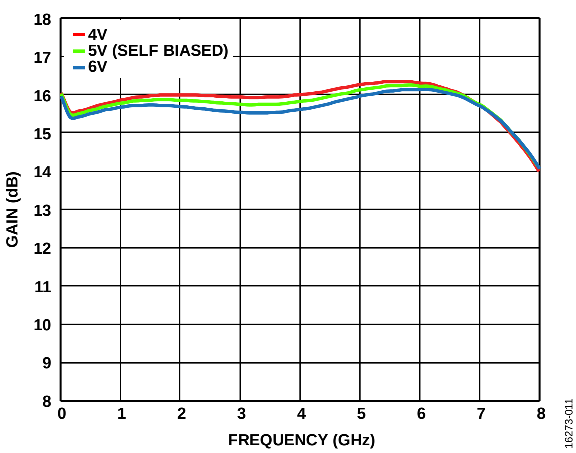


Figure 13. Gain vs. Frequency for Various Supply Currents (I_{DD}), Externally Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$



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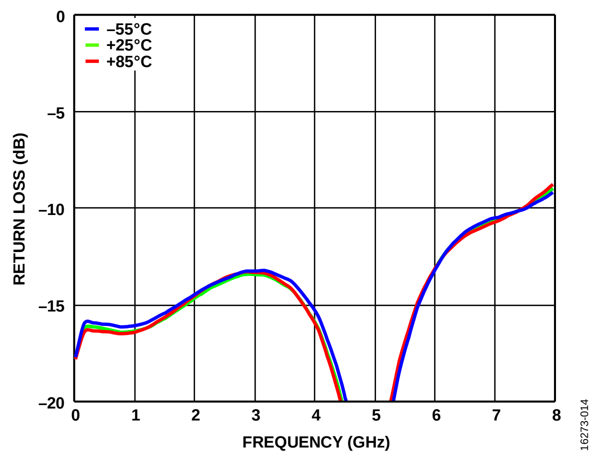

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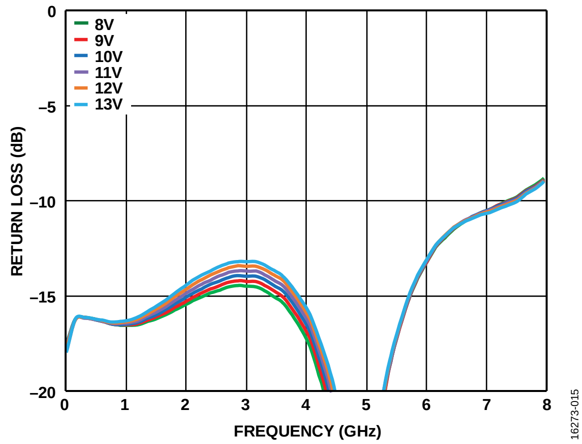


Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages (V_{DD}), Self Biased Mode, $V_{GG}2$ = Open, $V_{GG}1$ = GND

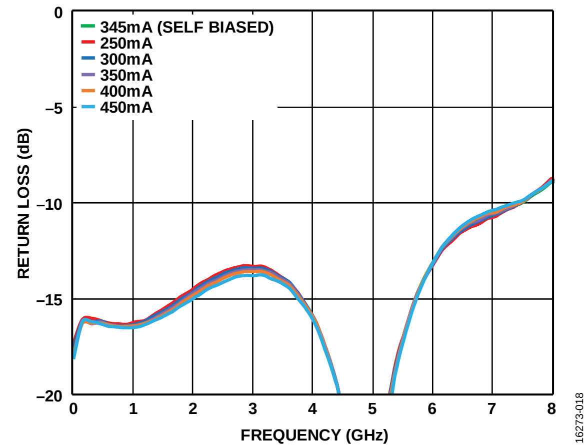


Figure 18. Input Return Loss vs. Frequency for Various Supply Currents (I_{DD}), Externally Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$

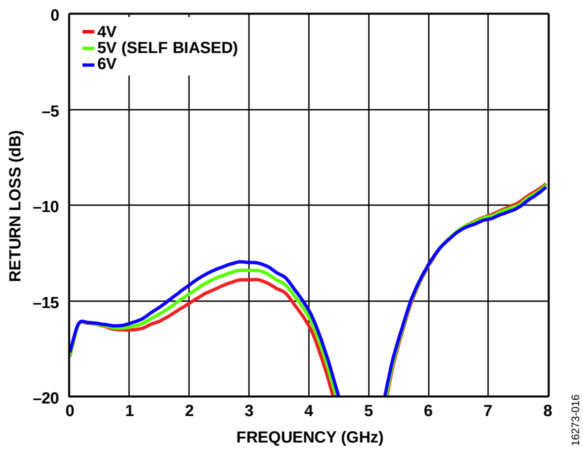


Figure 16. Input Return Loss vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$= GND

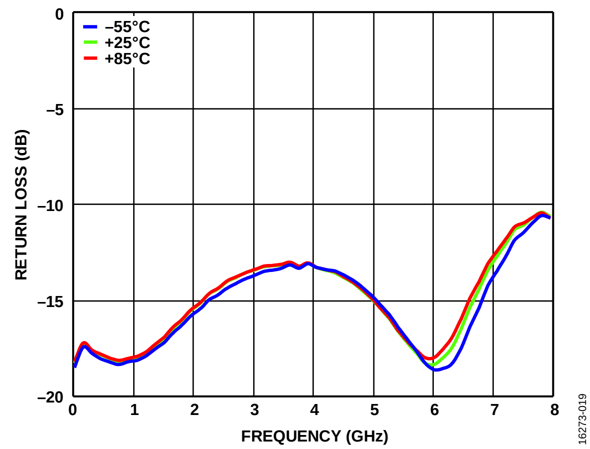


Figure 19. Output Return Loss vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} =12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

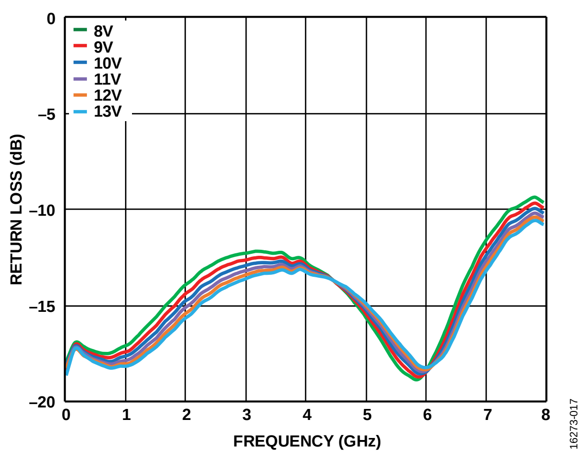
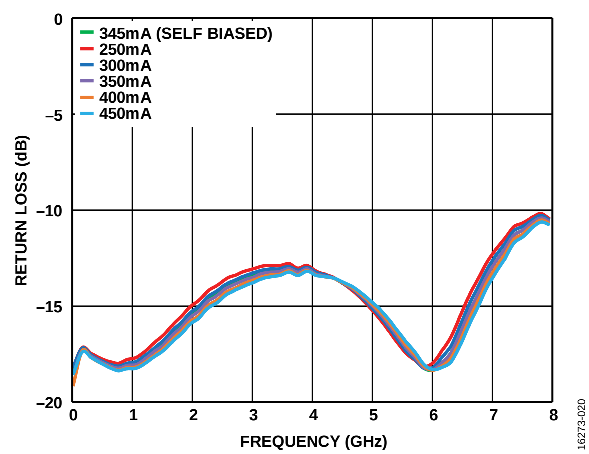


Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages (V_{DD}), Self Biased Mode, $V_{GG}2$ = Open, $V_{GG}1$ = GND



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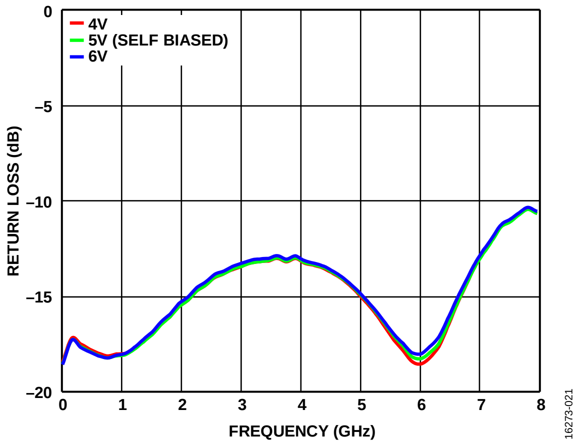
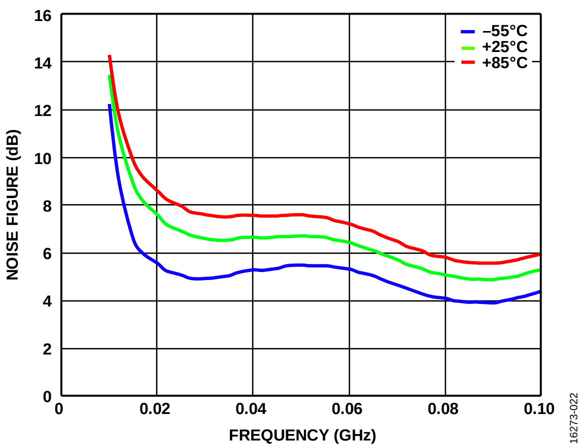


Figure 21. Output Return Loss vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$ = GND



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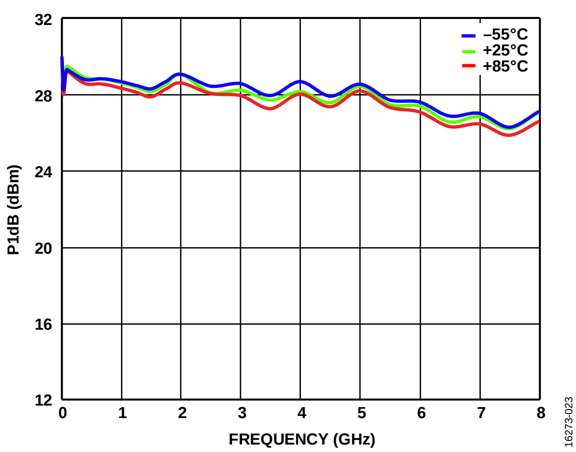


Figure 23. P1dB vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

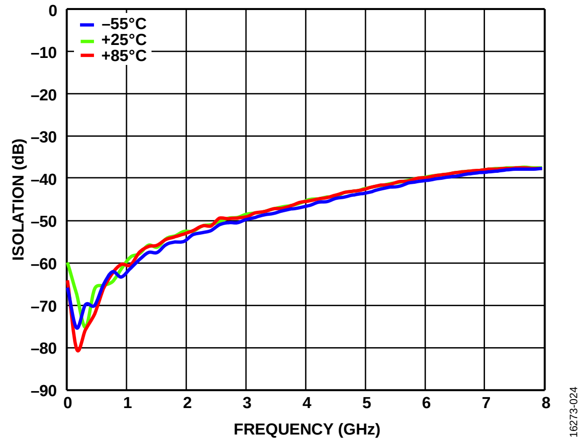
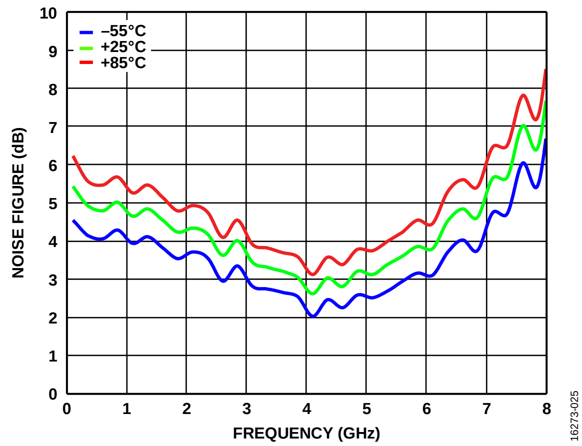


Figure 24. Reverse Isolation vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND



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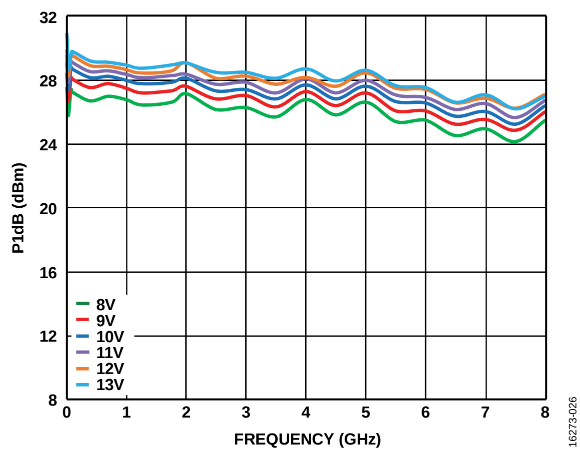


Figure 26. P1dB vs. Frequency for Various Supply Voltages (V_{DD}), $V_{GG}2$ = Open, $V_{GG}1$ = GND

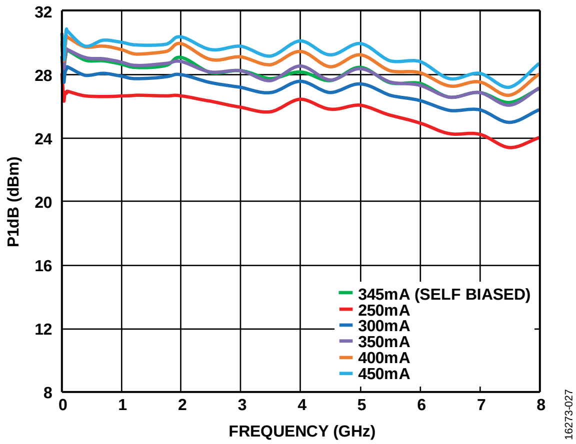


Figure 27. P1dB vs. Frequency for Various Supply Currents (I_{DD}), Externally Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$

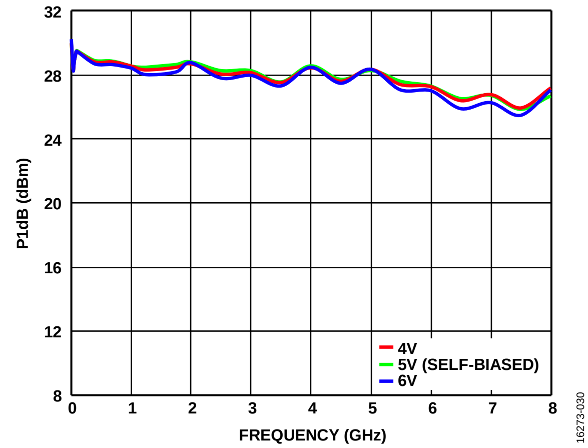
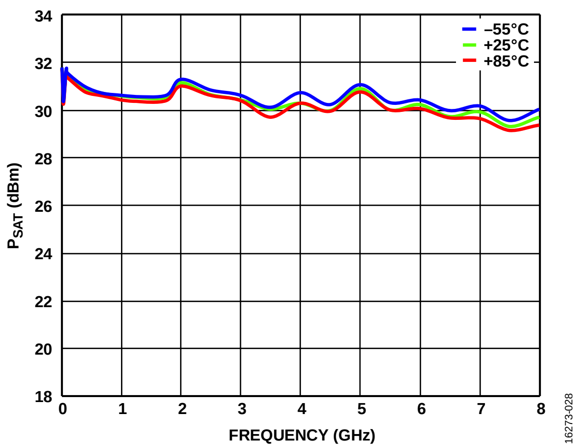


Figure 30. P1dB vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$ = GND



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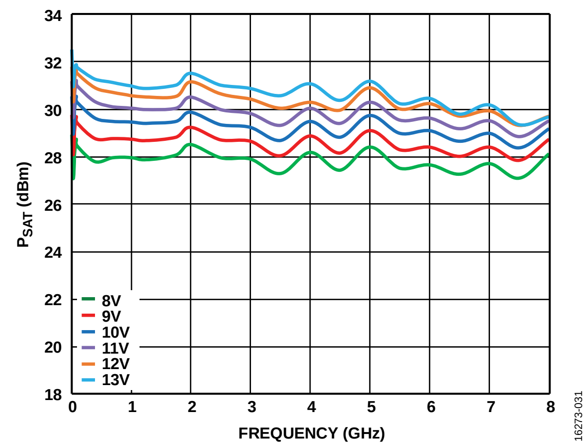

Figure 31. P_{SAT} vs. Frequency for Various Supply Voltages (V_{DD}), $V_{GG}2$ = Open, $V_{GG}1$ = GND

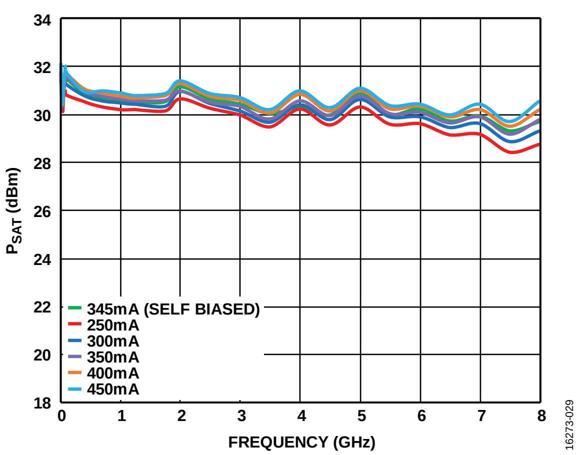

Figure 29. P_{SAT} vs. Frequency for Various Supply Currents (I_{DD}), V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$

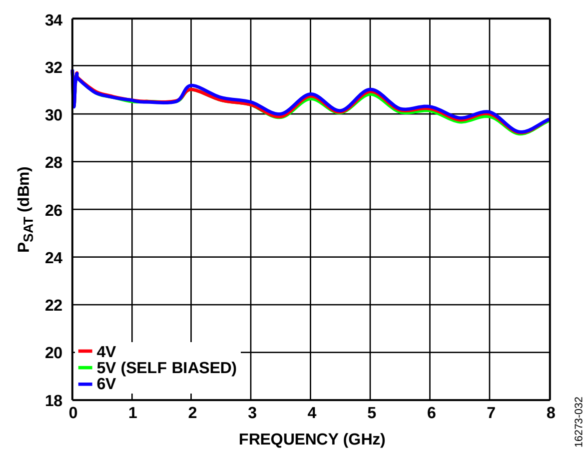

Figure 32. P_{SAT} vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$ = GND

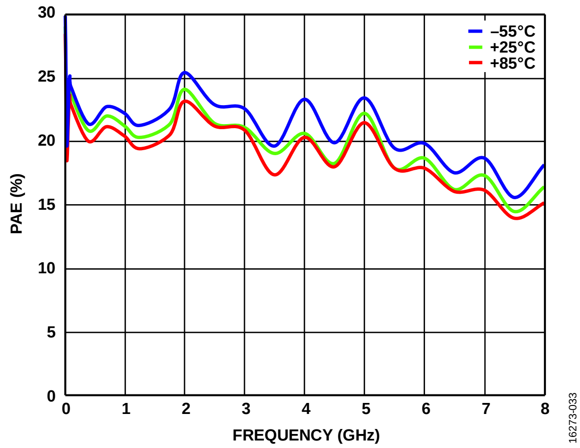

Figure 33. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND, PAE Measured at P_{SAT}

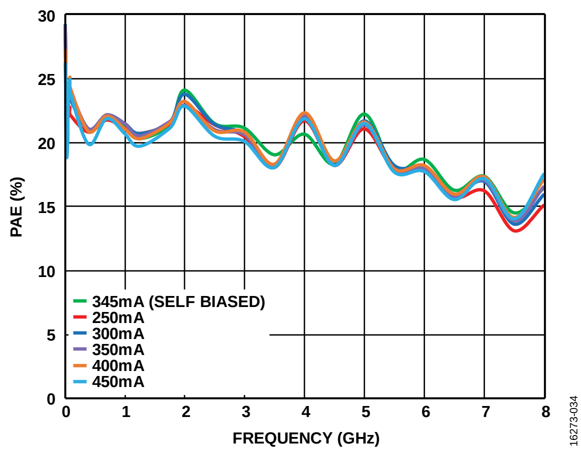

Figure 34. PAE vs. Frequency for Various Supply Currents (I_{DD}), V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$, PAE Measured at P_{SAT}

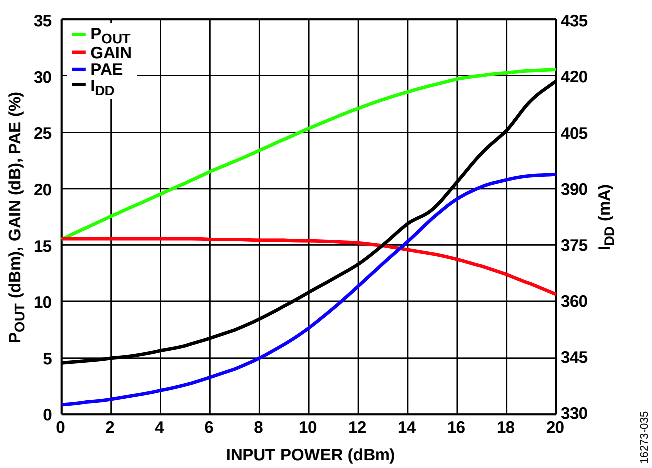

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 1 GHz, V_{DD} = 12 V, $V_{GG}1$= GND, $V_{GG}2$ = Open

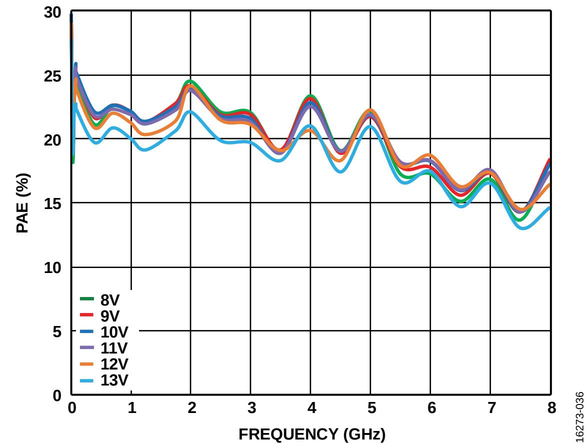

Figure 36. PAE vs. Frequency for Various Supply Voltages (V_{DD}), $V_{GG}2$ = Open, $V_{GG}1$ = GND, PAE Measured at P_{SAT}

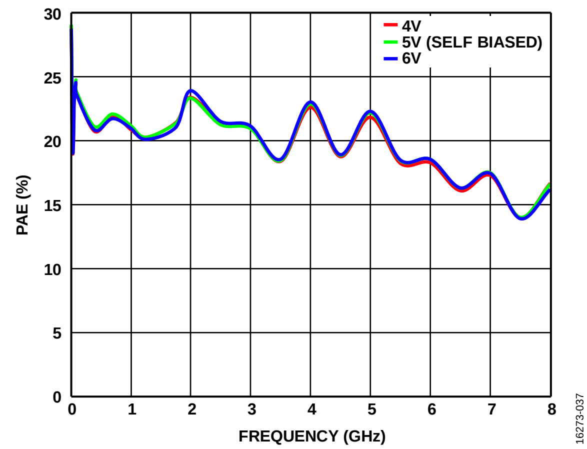

Figure 37. PAE vs. Frequency for Various $V_{GG}2$ Values, V_{DD} =12 V, $V_{GG}1$ = GND, PAE Measured at P_{SAT}

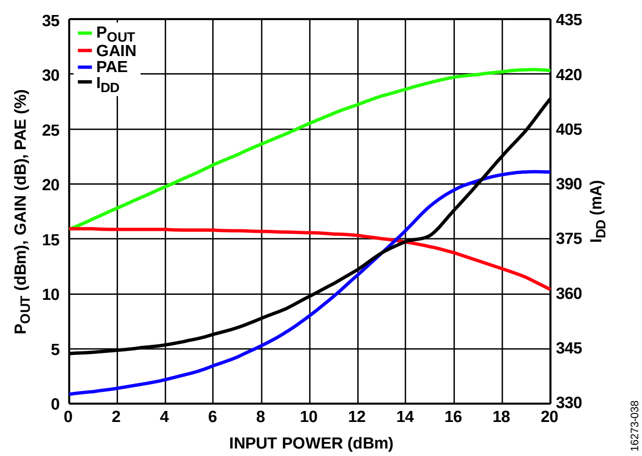

Figure 38. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 3 GHz, V_{DD} = 12 V, $V_{GG}1$ = GND, $V_{GG}2$ = Open

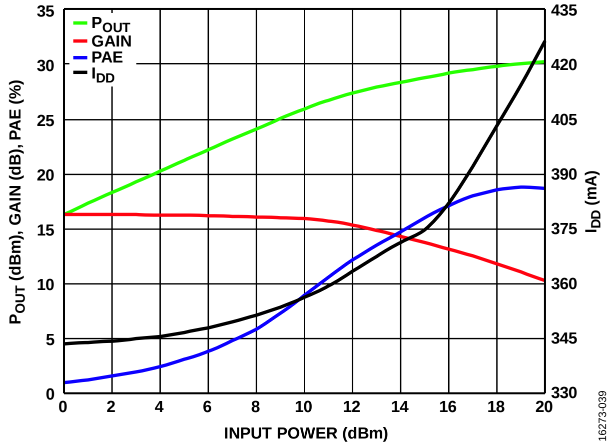

Figure 39. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 6 GHz, V_{DD} = 12 V, $V_{GG}1$= GND, $V_{GG}2$ = Open

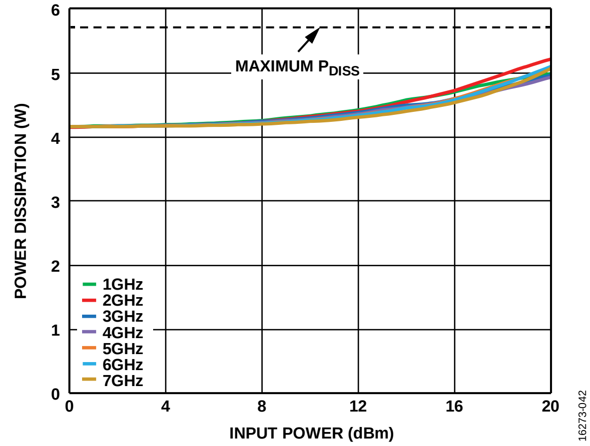

Figure 42. Power Dissipation vs. Input Power at T_A = 85°C, V_{DD} = 12 V, $V_{GG}1$ = GND, $V_{GG}2$ = Open

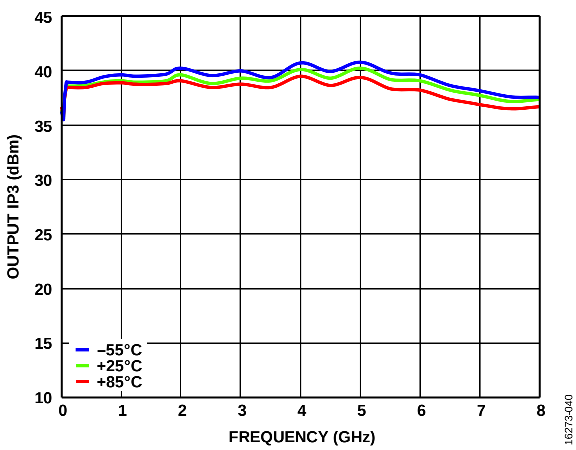

Figure 40. Output IP3 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 10 dBm, Self Biased Mode, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

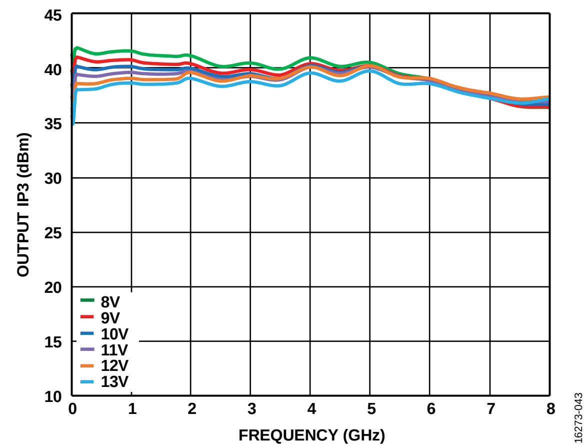

Figure 43. Output IP3 vs. Frequency for Various Supply Voltages (V_{DD}), $V_{GG}2$ = Open, $V_{GG}1$ = GND, P_{OUT}/Tone = 10 dBm

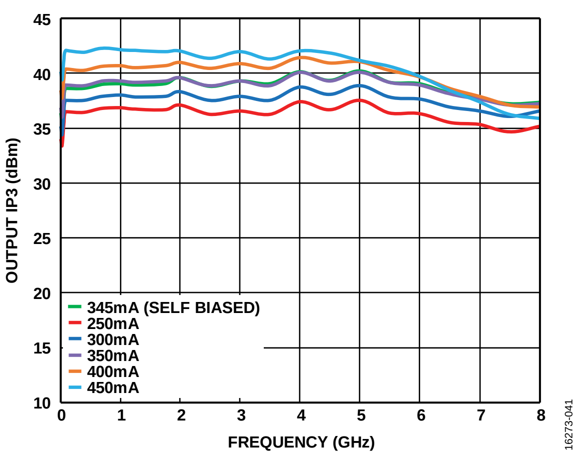

Figure 41. Output IP3 vs. Frequency for Various Supply Current (I_{DD}), V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$, P_{OUT}/Tone = 10 dBm

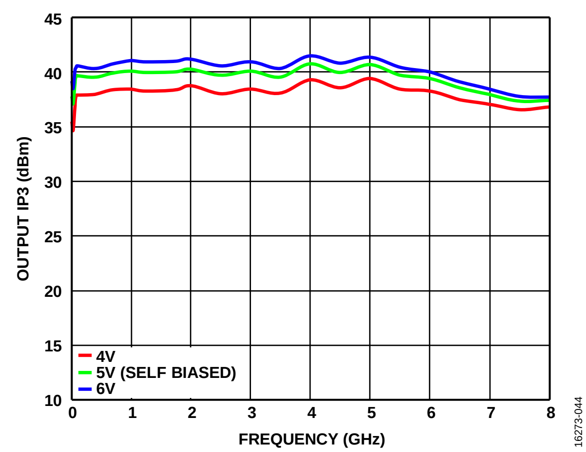

Figure 44. Output IP3 vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$ = GND, P_{OUT}/Tone = 10 dBm

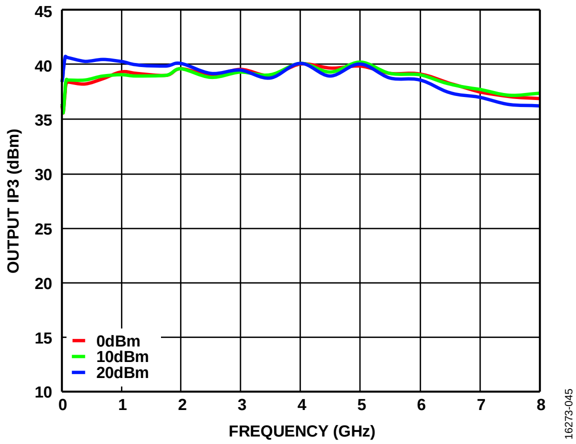

Figure 45. Output IP3 vs. Frequency for Various P_{OUT}/Tone, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

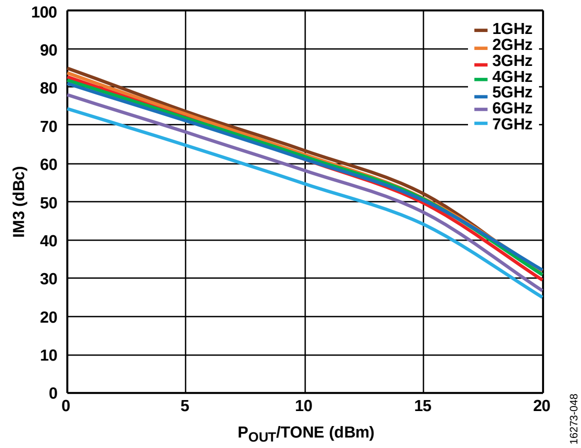

Figure 48. IM3 vs. P_{OUT}/Tone, V_{DD} = 8 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

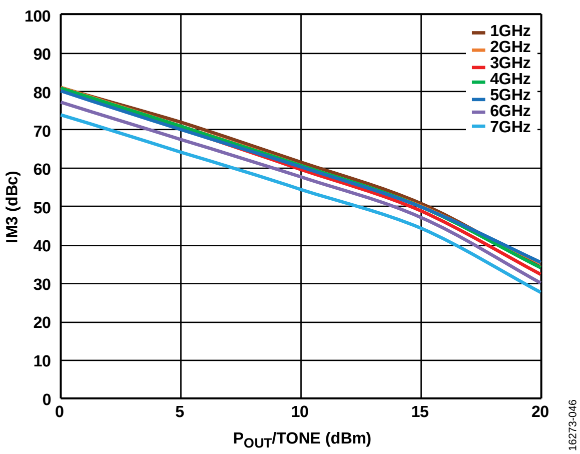

Figure 46. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT}/Tone, V_{DD} = 9 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

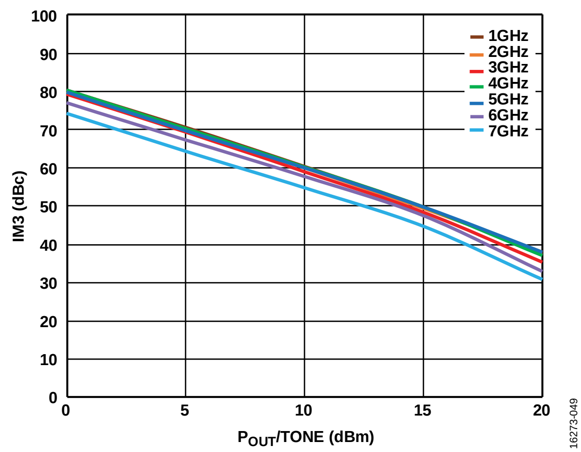

Figure 49. IM3 vs. P_{OUT}/Tone, V_{DD} = 10 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

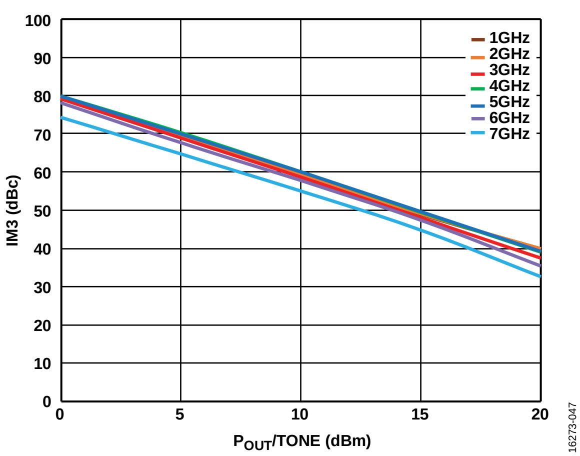

Figure 47. IM3 vs. P_{OUT}/Tone, V_{DD} = 11 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

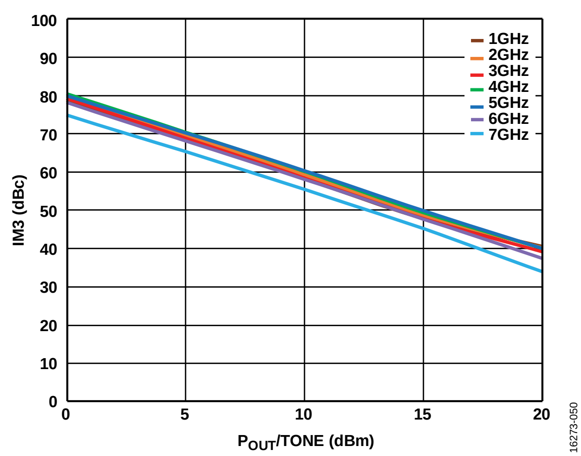

Figure 50. IM3 vs. P_{OUT}/Tone, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

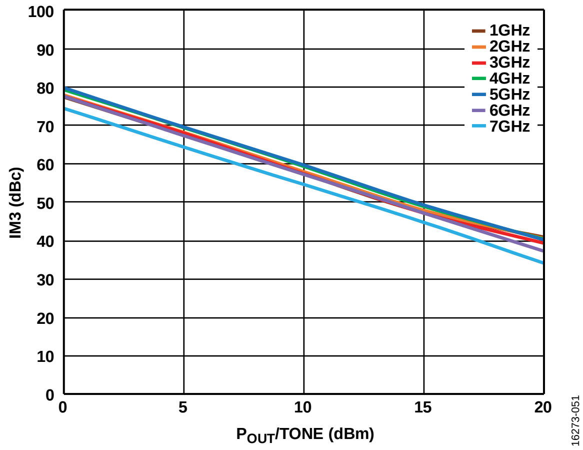

Figure 51. IM3 vs. P_{OUT}/Tone, V_{DD} = 13 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

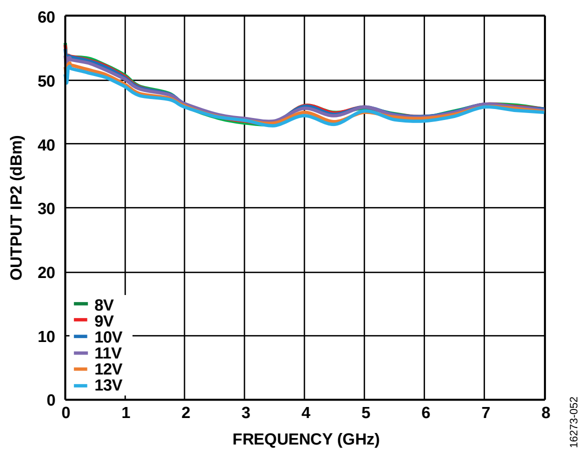

Figure 52. Output IP2 vs. Frequency for Various Supply Voltages (V_{DD}), $V_{GG}2$ = Open, $V_{GG}1$ = GND, P_{OUT}/Tone = 10 dBm

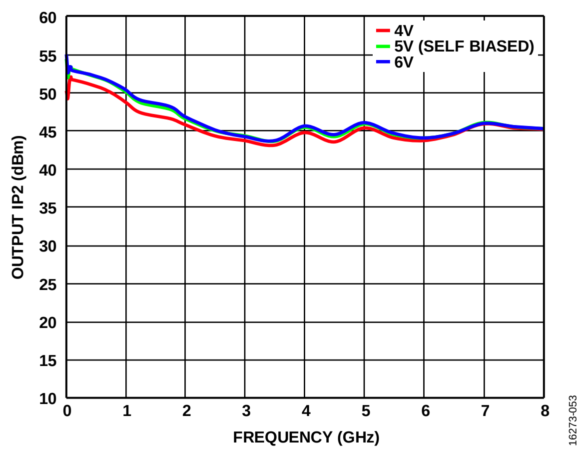

Figure 53. Output IP2 vs. Frequency for Various $V_{GG}2$ Values, V_{DD} =12 V, $V_{GG}1$ = GND, P_{OUT}/Tone = 10 dBm

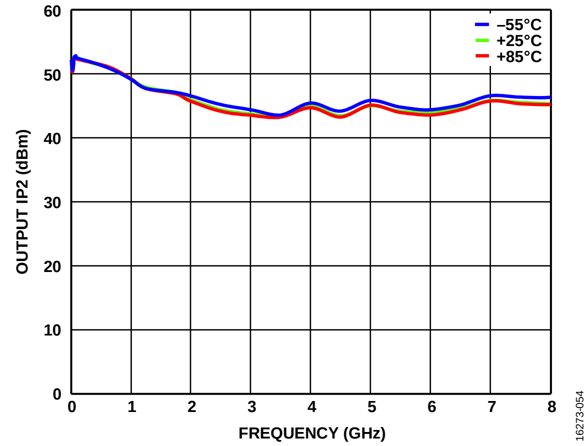

Figure 54. Output IP2 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 10 dBm, V_{DD} =12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND (Self Biased)

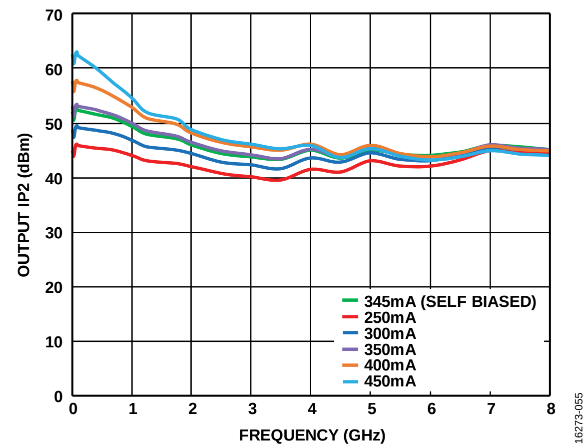

Figure 55. Output IP2 vs. Frequency for Various Supply Currents (I_{DD}), V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$, P_{OUT}/Tone = 10 dBm

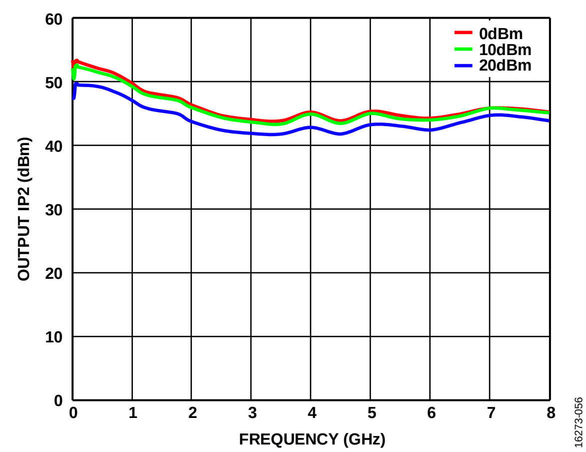

Figure 56. Output IP2 vs. Frequency for Various P_{OUT}/Tone Values, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

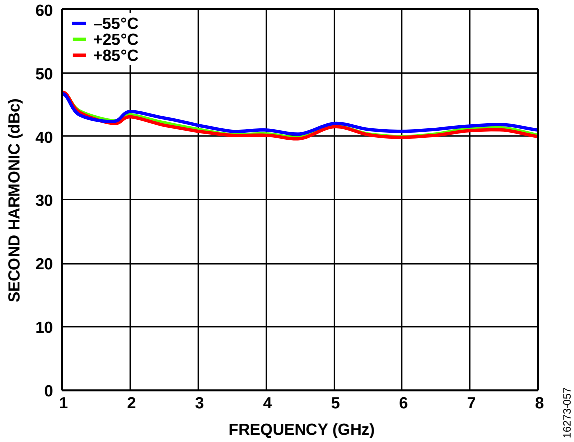

Figure 57. Second Harmonic vs. Frequency for Various Temperatures, P_{OUT} = 10 dBm, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND (Self Biased)

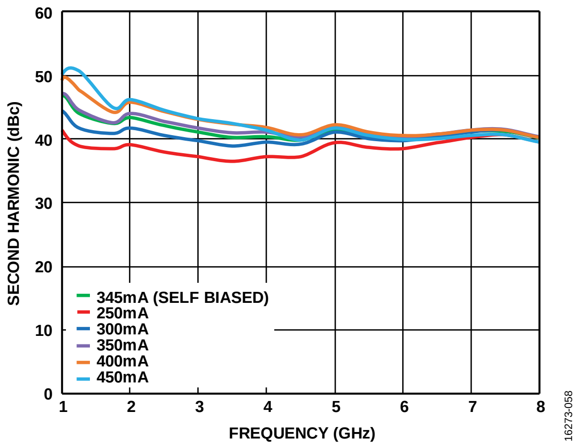

Figure 58. Second Harmonic vs. Frequency for Various Supply Currents (I_{DD}), V_{DD} = 12 V, $V_{GG}2$ = Open, Controlled $V_{GG}1$, P_{OUT} = 10 dBm

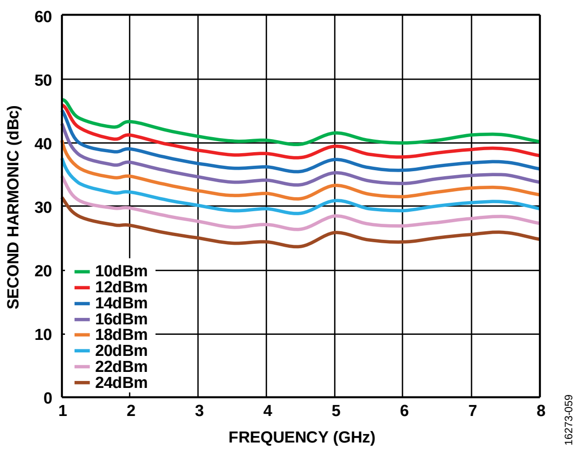

Figure 59. Second Harmonic vs. Frequency for Various P_{OUT} Values, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND (Self Biased)

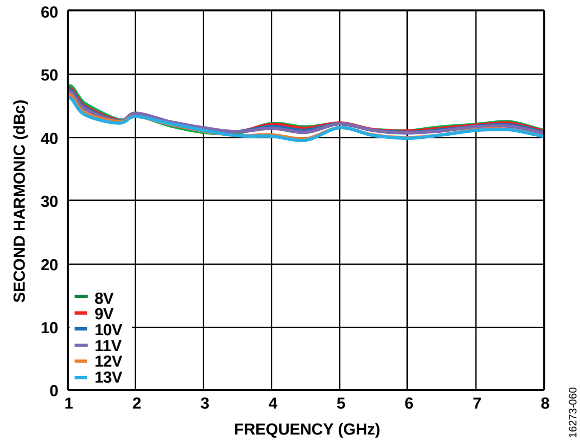

Figure 60. Second Harmonic vs. Frequency for Various Supply Voltages (V_{DD}), P_{OUT} = 10 dBm, $V_{GG}2$ = Open, $V_{GG}1$ = GND

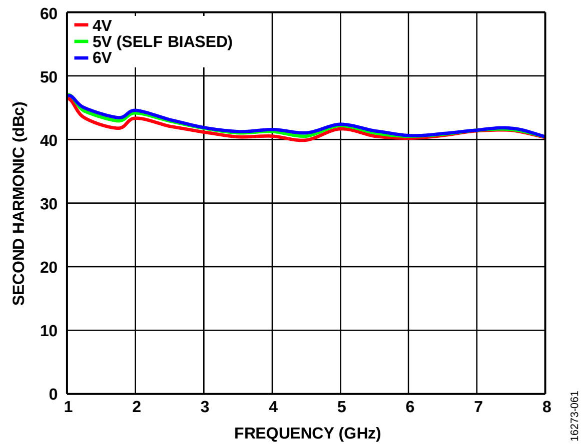

Figure 61. Second Harmonic vs. Frequency for Various $V_{GG}2$ Values, V_{DD} = 12 V, $V_{GG}1$ = GND, P_{OUT} = 10 dBm

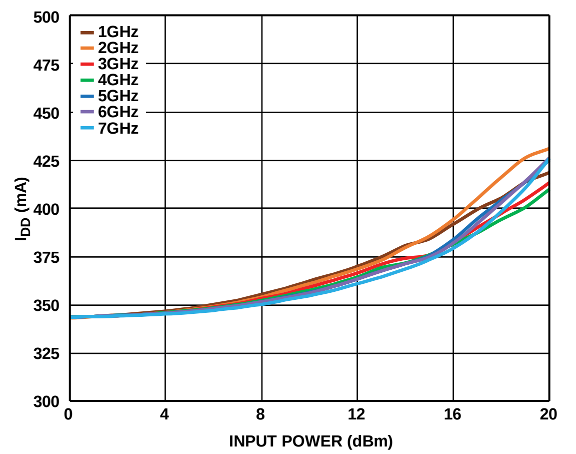

Figure 62. I_{DD} vs. Input Power for Various Frequencies, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

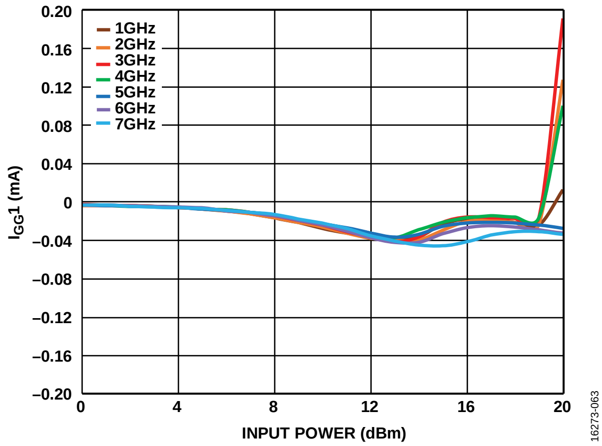

Figure 63. Gate 1 Current ($I_{GG}1$) vs. Input Power for Various Frequencies, V_{DD} = 12 V, $V_{GG}2$ = Open, $V_{GG}1$ = GND

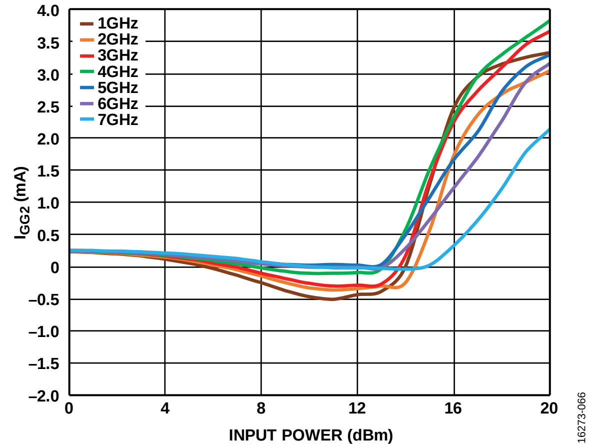

Figure 66. Gate 2 Current ($I_{GG}2$) vs. Input Power for Various Frequencies, V_{DD} = 12 V, $V_{GG}2$ = 5 V, $V_{GG}1$ = GND

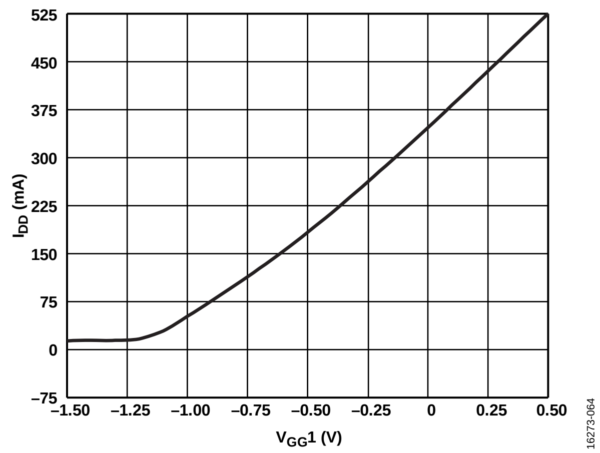

Figure 64. I_{DD} vs. $V_{GG}1$, V_{DD} = 12 V, $V_{GG}2$ = Open

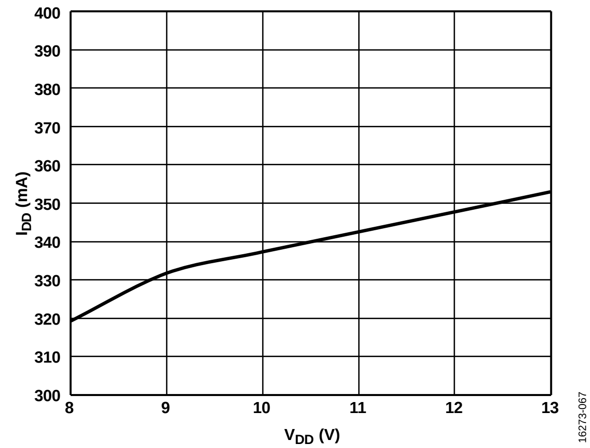

Figure 67. I_{DD} vs. V_{DD}, $V_{GG}2$ = Open, $V_{GG}1$ = GND

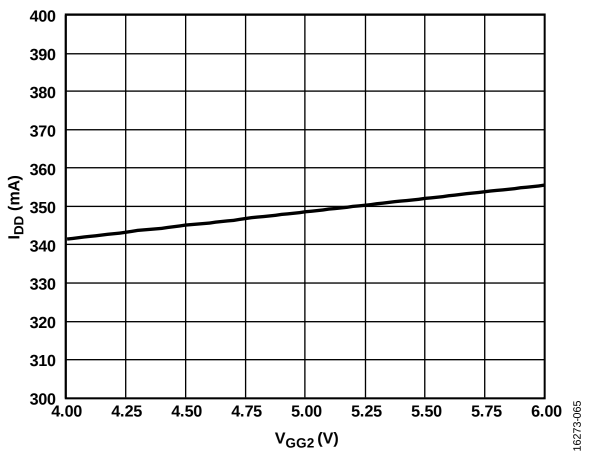

Figure 65. I_{DD} vs. $V_{GG}2$, V_{DD} = 12 V, $V_{GG}1$ = GND

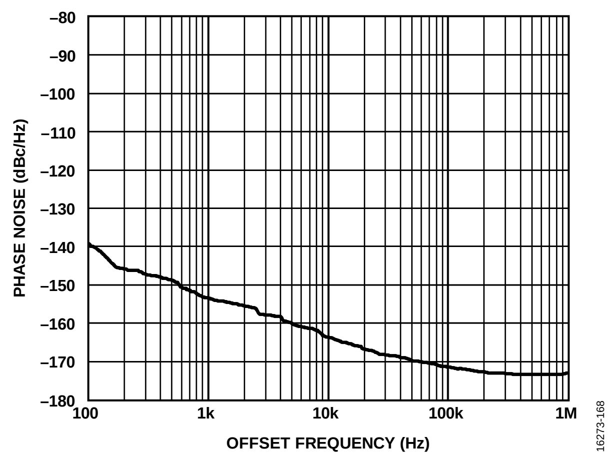

Figure 68. Additive Phase Noise vs. Offset Frequency, RF Frequency = 6 GHz, RF Input Power = 1 dBm (P1dB)

THEORY OF OPERATION

The HMC637BPM5E is a GaAs, MMIC, pHEMT, cascode distributed power amplifier. The cascode distributed architecture of the HMC637BPM5E uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to the drain of the lower FET. The fundamental cell is then duplicated several times with an RFIN transmission line interconnecting the gates of the lower FETs and an RFOUT transmission line interconnecting the drains of the upper FETs.

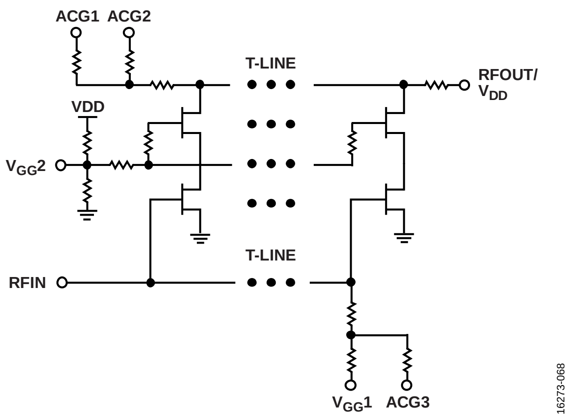

Figure 69. Simplified Schematic of the Cascode Distributed Amplifier

Additional circuit design techniques are used around each cell to optimize the overall bandwidth, output power, and noise figure. The major benefit of this architecture is that a high output level is maintained across a bandwidth far greater than what a single instance of the fundamental cell provides. A simplified schematic of this architecture is shown in Figure 69.

The gate bias voltages of the upper FETs are set internally by a resistive voltage divider tapped off at V_{DD}, resulting in a 5 V bias for the nominal V_{DD} value of 12 V. However, the $V_{GG}2$ pin is provided to allow the application of an externally generated bias voltage within the range of 4 V up to 6 V. Application of such a voltage allows adjustment of IP3 and IP2 by as much as 3 dB and 1.5 dB, respectively, while minimally affecting the gain, noise figure, P1dB, P_{SAT}, and PAE. The effect of this bias adjustment on performance is more apparent at lower operating frequencies.

For simplified biasing without the need for a negative voltage rail, $V_{GG}1$ can be connected directly to GND. With V_{DD} = 12 V and $V_{GG}1$ grounded, a quiescent drain current of 345 mA (typical) results. An externally generated $V_{GG}1$ voltage can optionally be applied, allowing adjustment of the quiescent drain current above and below the 345 mA nominal value. As an example, Figure 64 shows that by adjusting $V_{GG}1$ from −0.3 V to +0.3 V (approximately), quiescent drain currents from 250 mA to 450 mA can be obtained.

The HMC637BPM5E has single-ended input and output ports with impedances nominally equal to 50 Ω over the dc to 7.5 GHz frequency range. Therefore, the device can be directly inserted into a 50 Ω system with no required impedance matching circuitry. Similarly, the input and output impedances are sufficiently stable across variations in temperature and supply voltage so that no impedance matching compensation is required. The RF output port additionally functions as the V_{DD} bias pin, requiring an RF choke through which dc bias is applied.

Though the device technically operates down to dc, blocking capacitors are recommended at the RF input and output ports to prevent the stages with which they interface from loading the dc bias supplies and suffering damage. The RF choke and blocking capacitor at the RF output together constitute a bias tee. In practice, the external RF choke and dc blocking capacitor selections limit the lowest frequency of operation.

ACG1 through ACG3 are nodes at which ac terminations (capacitors) to ground can be provided. The use of such terminations serves to roll off the gain at frequencies below 200 MHz, allowing the flattest possible gain response to be obtained over various frequencies.

It is critical to supply very low inductance ground connections to the GND pins and to the package base exposed pad to ensure stable operation. To achieve optimal performance from the HMC637BPM5E and to prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Capacitive bypassing is required for V_{DD} and $V_{GG}1$, as shown in the typical application circuit in Figure 70. Both the RFIN and RFOUT/V_{DD} pins are dc-coupled. Use of an external dc blocking capacitor at RFIN is recommended. Use of an external RF choke plus a dc blocking capacitor (for example, a bias tee) at RFOUT/
V_{DD} is required. For wideband applications, ensure that the frequency responses of the external biasing and blocking components are adequate for use across the entire frequency range of the application.

The HMC637BPM5E operates in either self biased or externally biased mode. To operate in self biased mode, ground the $V_{GG}1$ pin and leave $V_{GG}2$ open. For the externally biased configuration, adjust $V_{GG}1$ within −2 V to +0.5 V to set the target drain current and adjust $V_{GG}2$ from 4 V to 6 V for IP2 and IP3 control.

The recommended bias sequence during power-up for self biased operation is as follows:

1. Connect GND.
2. Set V_{DD} to 12 V.
3. Apply the RF signal.

The recommended bias sequence during power-down for self biased operation is as follows :

1. Turn off the RFIN signal.
2. Set V_{DD} to 0 V.

The recommended bias sequence during power-up for externally biased operation is as follows:

1. Connect GND.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 12 V.
4. Increase $V_{GG}1$ to achieve the desired quiescent current (I_{DQ}).
5. Apply the RF signal.
6. When using the IP2/IP3 control function, apply a voltage from 4 V to 6 V until the desired performance is obtained.

The recommended bias sequence during power-down for externally biased operation is as follows:

1. Turn off the RFIN signal.
2. Remove the $V_{GG}2$ voltage.
3. Decrease $V_{GG}1$ to −2 V to achieve a typical I_{DQ} of 0 mA.
4. Set V_{DD} to 0 V.
5. Set $V_{GG}1$ to 0 V.

Adhere to the values shown in the Absolute Maximum Ratings section.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 70), and biased per the conditions in this section. The bias conditions described in this section are the operating points recommended to optimize the overall device performance. Operation using other bias conditions may result in performance that differs from what is shown in the Typical Performance Characteristic section. To obtain the best performance while avoiding damage to the device, follow the recommended biasing sequences described in this section.

TYPICAL APPLICATION CIRCUIT

In Figure 70, the drain bias (V_{DD}) must be applied through an external broadband bias tee connected at RFOUT/V_{DD} and connected to an external dc block at RFIN. Optional capacitors can be used if the device is to be operated below 200 MHz.

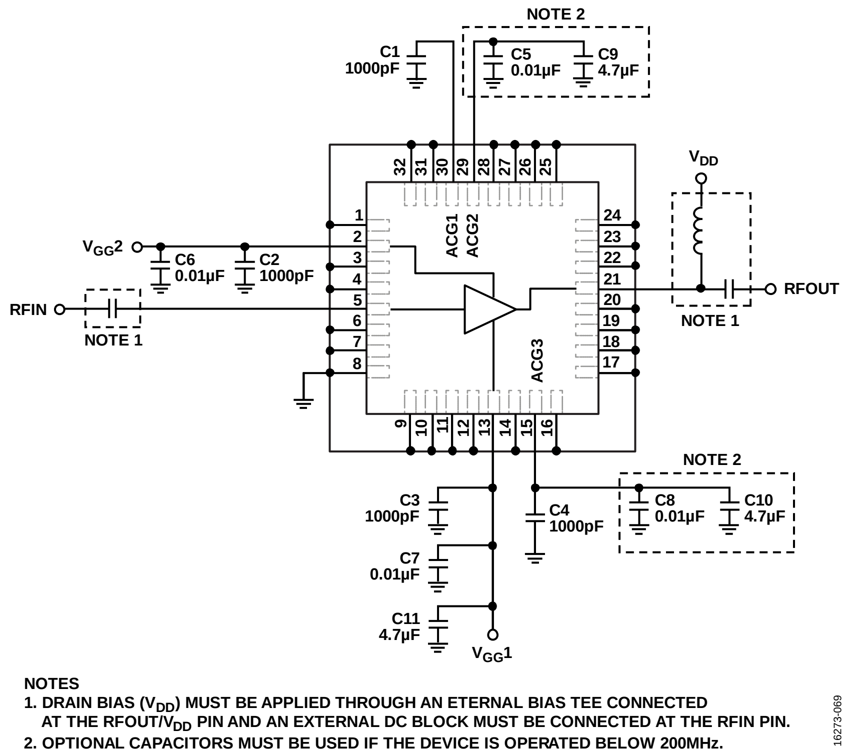

Figure 70. Typical Application Circuit

EVALUATION PCB

The EV1HMC637BPM5 (600-01711-00) evaluation PCB is shown in Figure 71.

BILL OF MATERIALS

Use RF circuit design techniques for the circuit board used in the application. Provide 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed pad to the ground plane, similar to what is shown in Figure 71. Use a sufficient number of via holes to connect the top and bottom ground planes, including the grounds directly beneath the ground pad to provide adequate electrical and thermal conduction. Use of a heat sink on the bottom side of the PCB is recommended. The evaluation PCB shown in Figure 71 is available from Analog Devices, Inc., upon request.

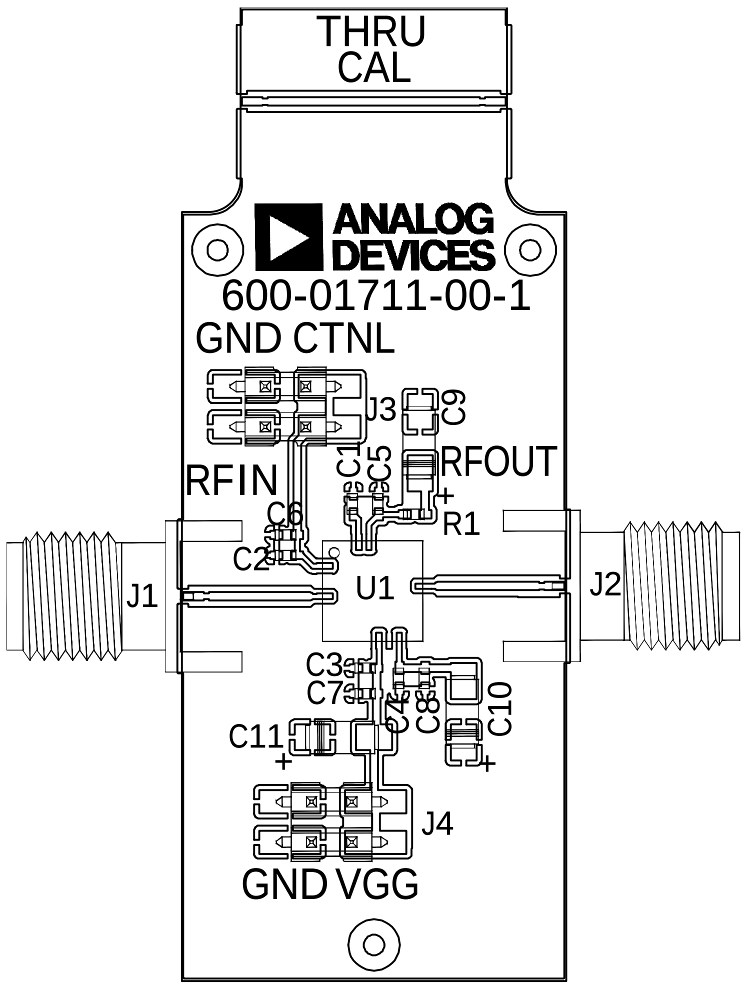

Figure 71. Evaluation PCB

Table 5. Bill of Materials for the Evaluation PCB EV1HMC637BPM5 (600-01711-00)

Item	Description
J1, J2	PCB Mount K connectors
J3, J4	DC pins
C1, C2, C3, C4	1000 pF capacitors, 0402 package
C5, C6, C7, C8	10000 pF capacitors, 0402 package
C9, C10, C11	4.7 µF capacitors, tantalum, 1206 package
R1	0 Ω resistor, 0402 package
U1	HMC637BPM5E
PCB	600-01711-00 evaluation PCB; circuit board material: Rogers 4350 or Arlon 25FR