Low Noise Amplifier, 0.4 GHz to 11 GHz

HMC8412

FEATURES

Low noise figure: 1.4 dB typical
Single positive supply (self biased)
High gain: ≤15.5 dB typical
High OIP3: ≤33 dBm typical
RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP

APPLICATIONS

Test instrumentation
Telecommunications
Military radar and communication
Electronic warfare
Aerospace

FUNCTIONAL BLOCK DIAGRAM

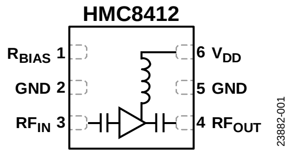

Figure 1.

GENERAL DESCRIPTION

The HMC8412 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 0.4 GHz to 11 GHz.

The HMC8412 provides a typical gain of 15.5 dB, a 1.4 dB typical noise figure, and a typical output third-order intercept (OIP3) of ≤33 dBm, requiring only 60 mA from a 5 V drain supply voltage. The saturated output power (P_{SAT}) of ≤20.5 dBm typical enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for many Analog Devices, Inc., balanced, inphase and quadrature (I/Q) or image rejection mixers.

The HMC8412 also features inputs and outputs that are internally matched to 50 Ω, making the device ideal for surface-mount technology (SMT)-based, high capacity microwave radio applications.

The HMC8412 is housed in an RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP.

Rev. 0 **Document Feedback**

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Technical Support **www.analog.com**

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REVISION HISTORY

5/2020—Revision 0: Initial Version

SPECIFICATIONS

0.4 GHz TO 3 GHz FREQUENCY RANGE

V_{DD} = 5 V, supply current (I_{DQ}) = 60 mA, R_{BIAS} = 1.47 kΩ, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.4		3	GHz	
GAIN	13	15.5		dB	
Gain Variation over Temperature		0.010		dB/°C	
NOISE FIGURE		1.4		dB	
RETURN LOSS					
Input		14		dB	
Output		13		dB	
OUTPUT					
Power for 1 dB Compression (OP1dB)	15	18		dBm	
P_{SAT}		20.5		dBm	
OIP3		32		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
Second-Order Intercept (OIP2)		40		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		28		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		60		mA	
V_{DD}	2	5	6	V	

3 GHz TO 9 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	3		9	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.012		dB/°C	
NOISE FIGURE		1.5		dB	
RETURN LOSS					
Input		15		dB	
Output		16		dB	
OUTPUT					
OP1dB	15.5	18		dBm	
P_{SAT}		20.5		dBm	
OIP3		33		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		41.5		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		29		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		60		mA	
V_{DD}	2	5	6	V	

9 GHz TO 11 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ, and T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	9		11	GHz	
GAIN	12	14		dB	
Gain Variation over Temperature		0.022		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input		14		dB	
Output		10		dB	
OUTPUT					
OP1dB	11	14		dBm	
P_{SAT}		18		dBm	
OIP3		31		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		49.5		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		15.5		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		60		mA	
V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	7 V
RF Input Power	25 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 9.15 mW/°C Above 85°C)	0.82 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Peak Reflow (Moisture Sensitivity Level 1 (MSL1))[1]	260°C
Junction Temperature to Maintain 1,000,000 Hours Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 60 mA	117.8°C

[1] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-6-12	109.3	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

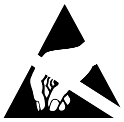
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for HMC8412

Table 6. HMC8412, 6-Lead LFCSP

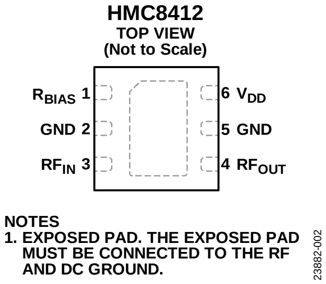
ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF AND DC GROUND.

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{BIAS}	Current Mirror Bias Resistor. Use the R_{BIAS} pin to set the quiescent current by connecting the external bias resistor as defined in Table 8. Refer to Figure 60 for the bias resistor connection. See Figure 3 for the interface schematic.
2, 5	GND	Ground. The GND pin must be connected to RF and dc ground. See Figure 6 for the interface schematic.
3	RF_{IN}	RF Input. The RF_{IN} pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
4	RF_{OUT}	RF Output. The RF_{OUT} pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
6	V_{DD}	Drain Supply Voltage for the Amplifier. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

INTERFACE SCHEMATICS

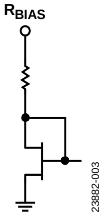


Figure 3. R_{BIAS} Interface Schematic

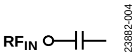


Figure 4. RF_{IN} Interface Schematic

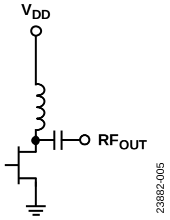


Figure 5. V_{DD} and RF_{OUT} Interface Schematic

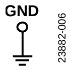


Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

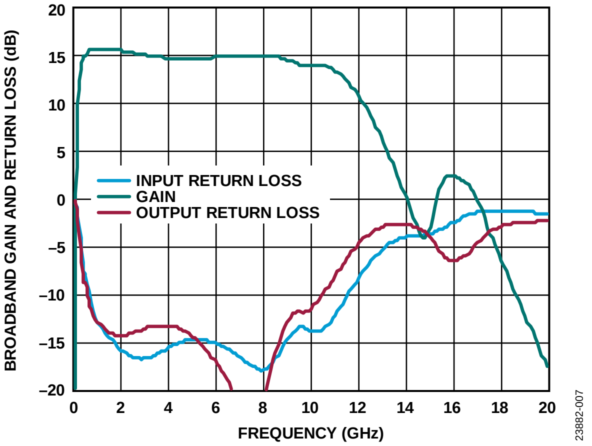


Figure 7. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 20 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

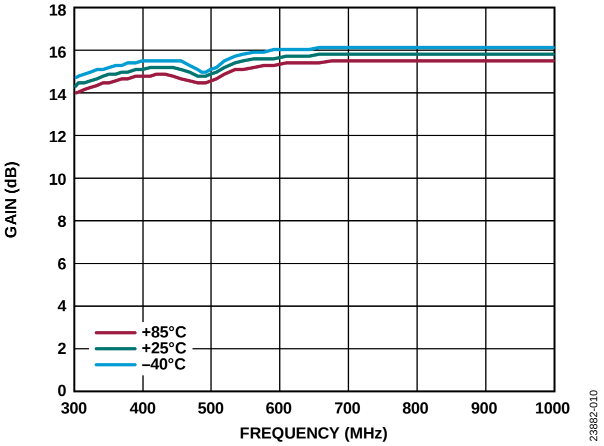


Figure 10. Gain vs. Frequency for Various Temperatures, 300 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

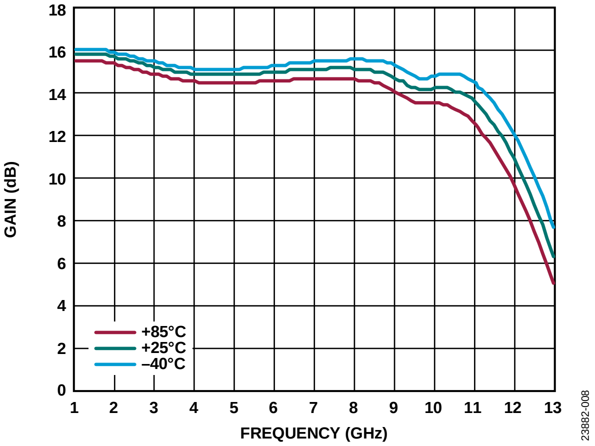


Figure 8. Gain vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

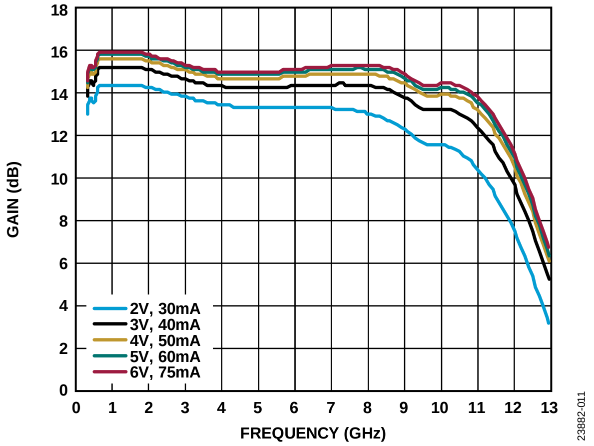


Figure 11. Gain vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

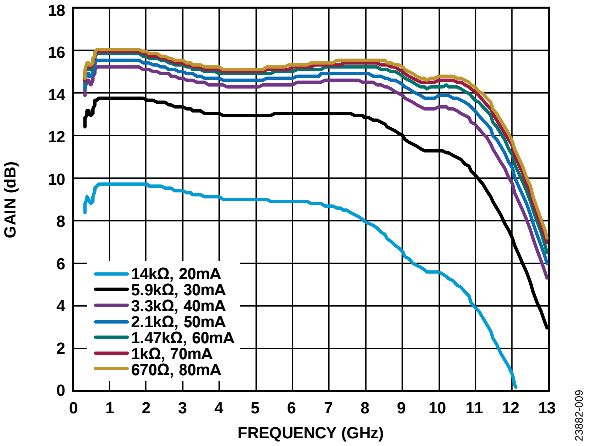


Figure 9. Gain vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

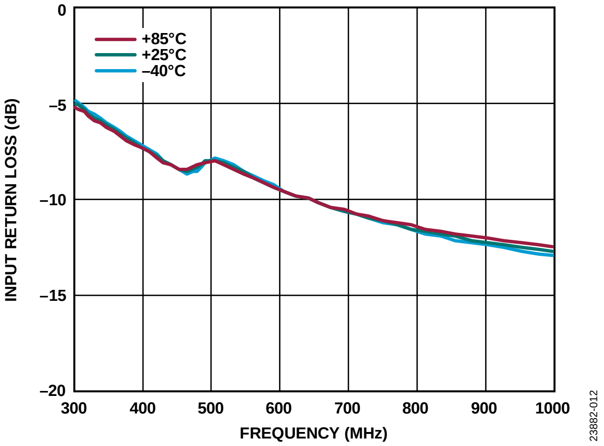


Figure 12. Input Return Loss vs. Frequency for Various Temperatures, 300 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

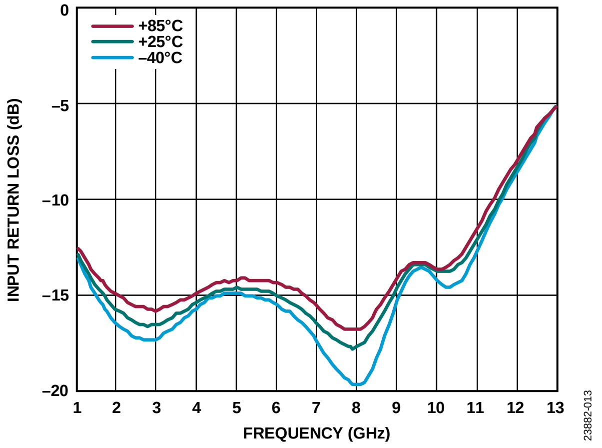


Figure 13. Input Return Loss vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

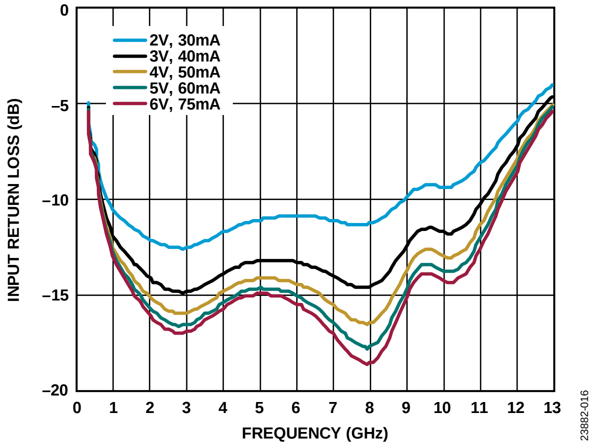


Figure 16. Input Return Loss vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

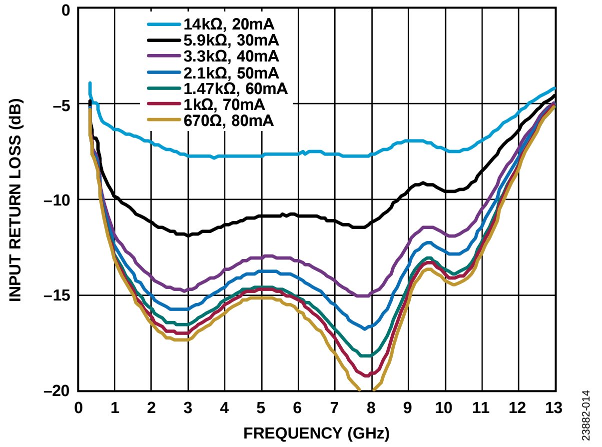


Figure 14. Input Return Loss vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

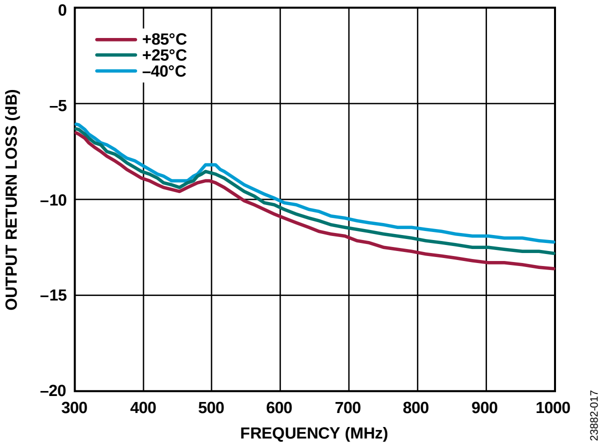


Figure 17. Output Return Loss vs. Frequency for Various Temperatures, 300 MHz to 1 GHz, R_{BIAS} = 1.47 kΩ

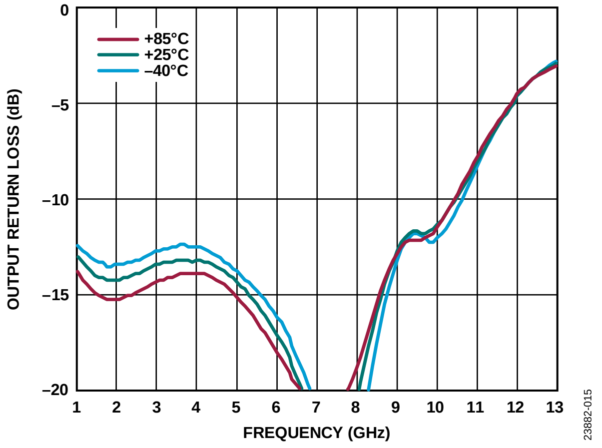


Figure 15. Output Return Loss vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

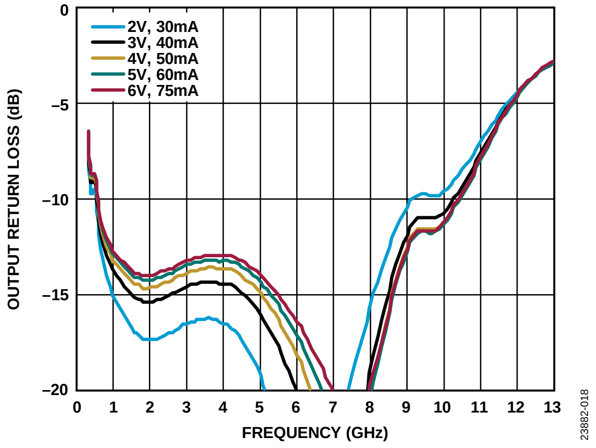


Figure 18. Output Return Loss vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

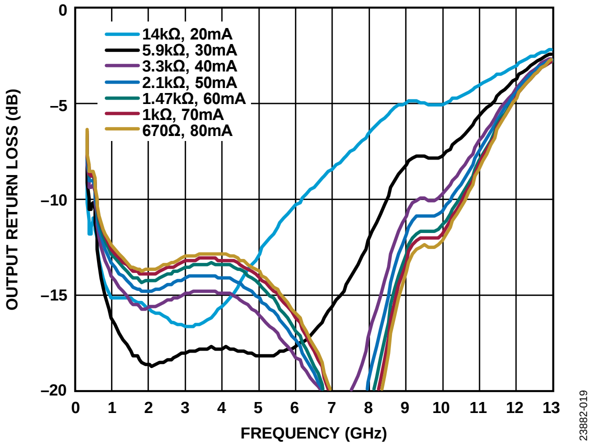


Figure 19. Output Return Loss vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

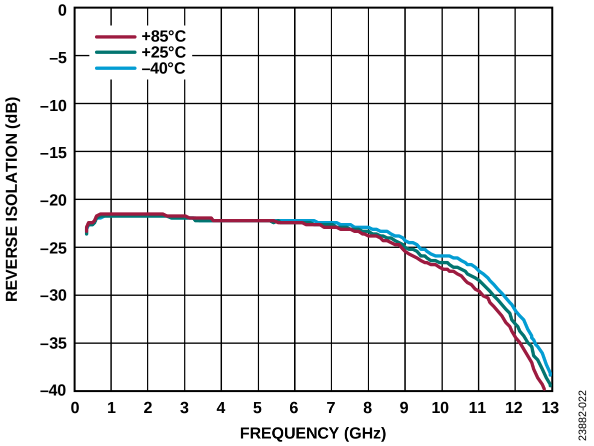


Figure 22. Reverse Isolation vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

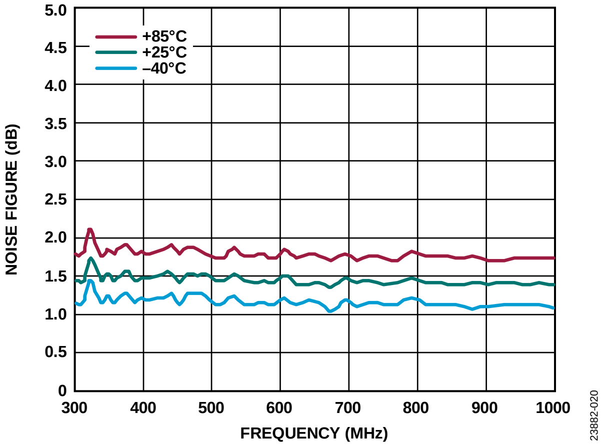


Figure 20. Noise Figure vs. Frequency for Various Temperatures, 300 MHz to 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

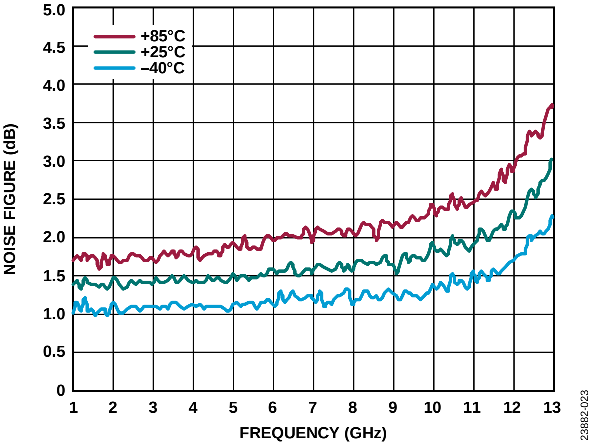


Figure 23. Noise Figure vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

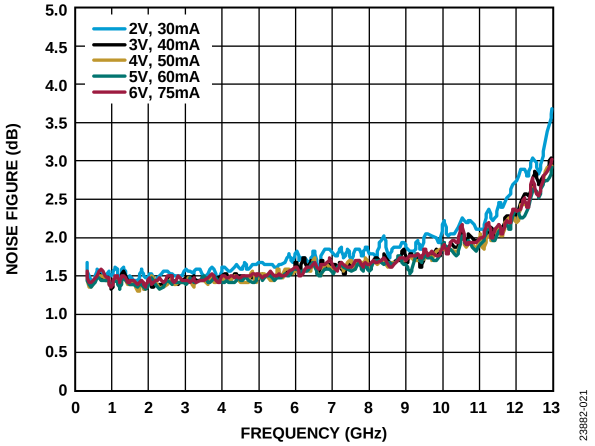


Figure 21. Noise Figure vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

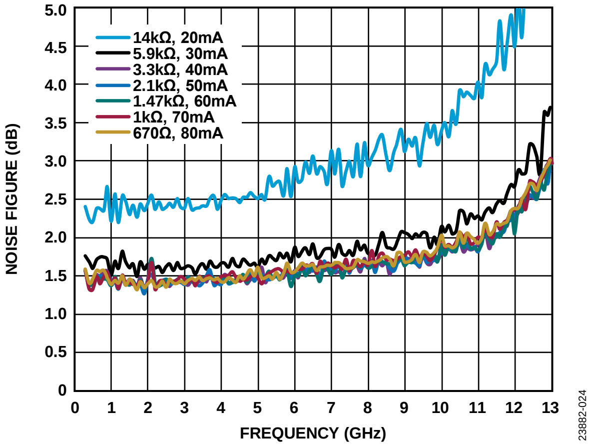


Figure 24. Noise Figure vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

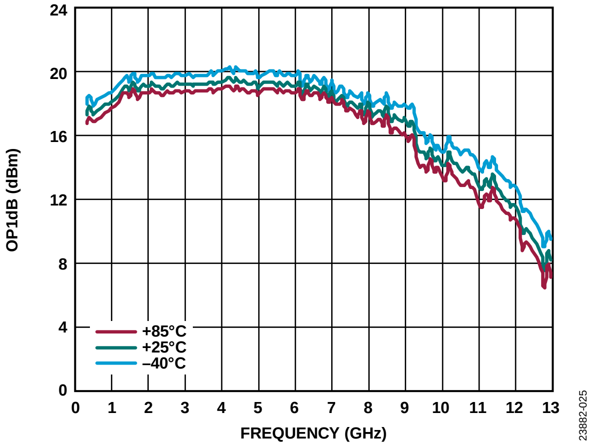


Figure 25. OP1dB vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

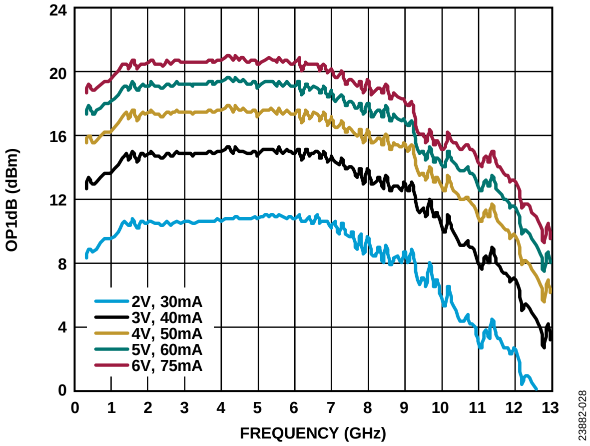


Figure 28. OP1dB vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

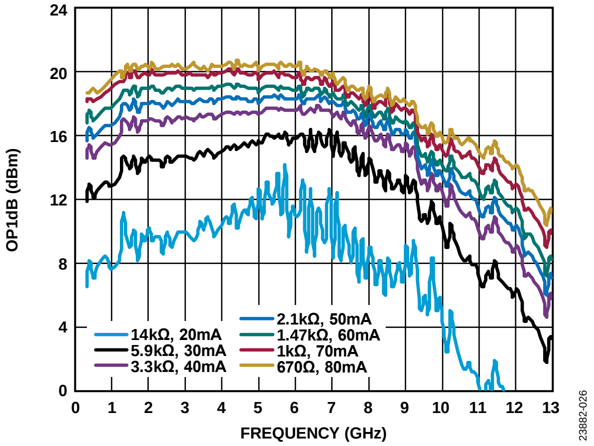


Figure 26. OP1dB vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

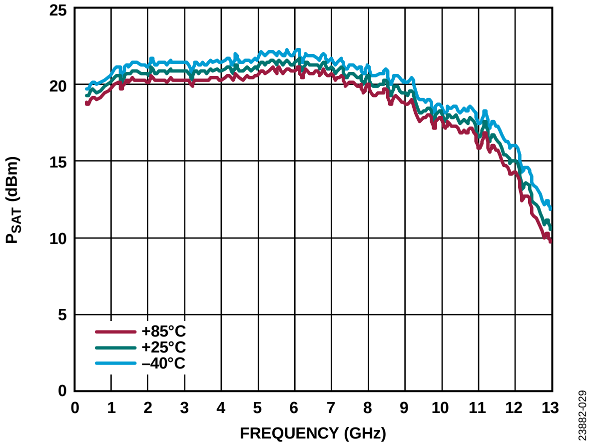


Figure 29. P_{SAT} vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

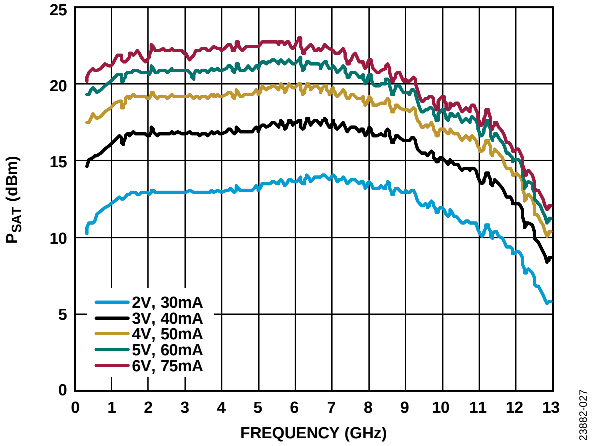


Figure 27. P_{SAT} vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

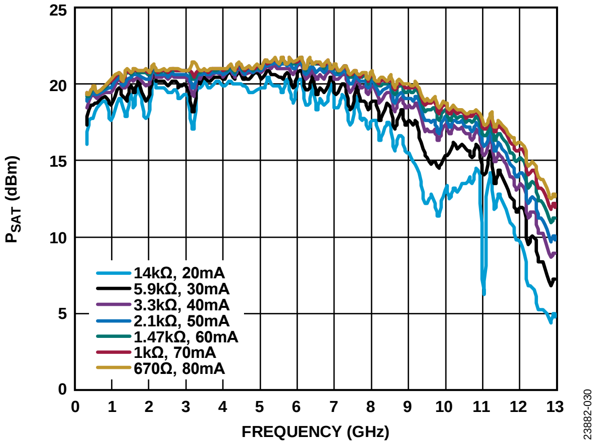


Figure 30. P_{SAT} vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

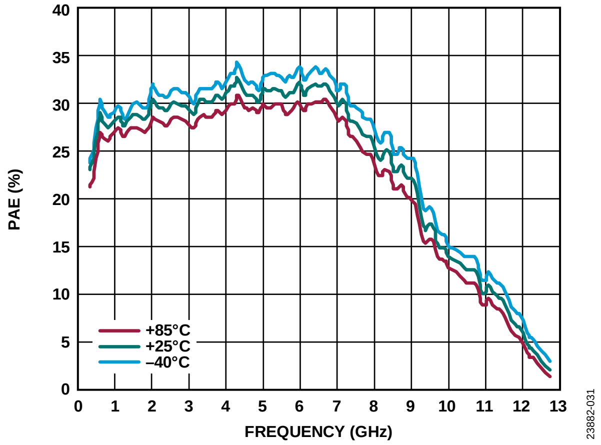


Figure 31. PAE vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

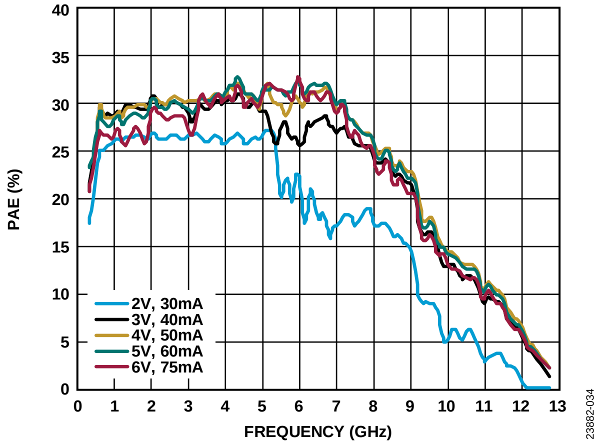


Figure 34. PAE vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ

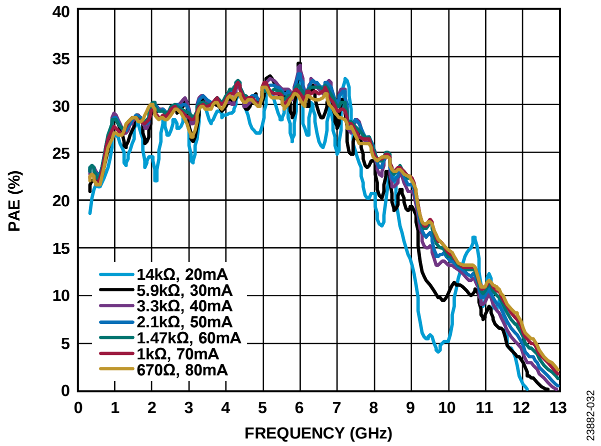


Figure 32. PAE vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V

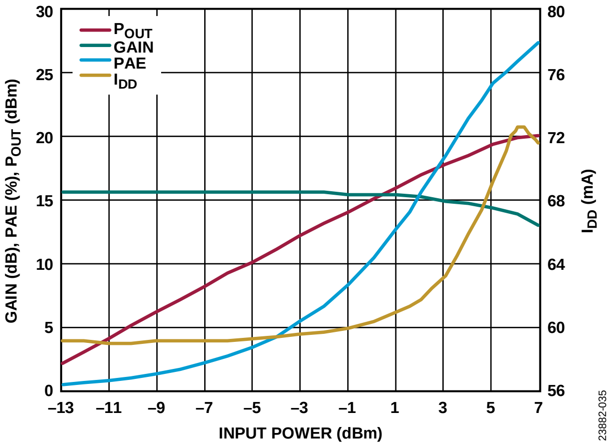


Figure 35. Gain, PAE, P_{OUT}, and I_{DD} vs. Input Power, Power Compression at 1 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

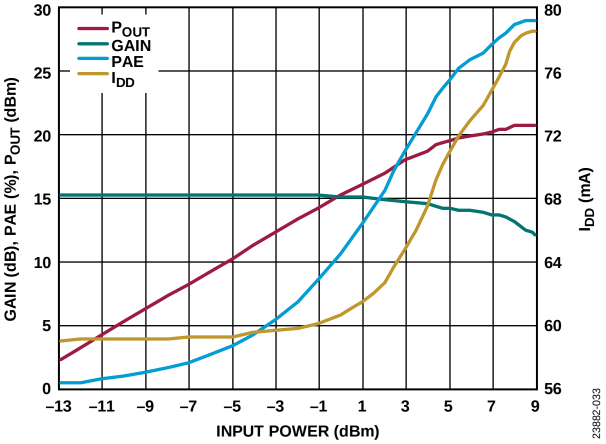


Figure 33. Gain, PAE, P_{OUT}, and Drain Current (I_{DD}) vs. Input Power, Power Compression at 3 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

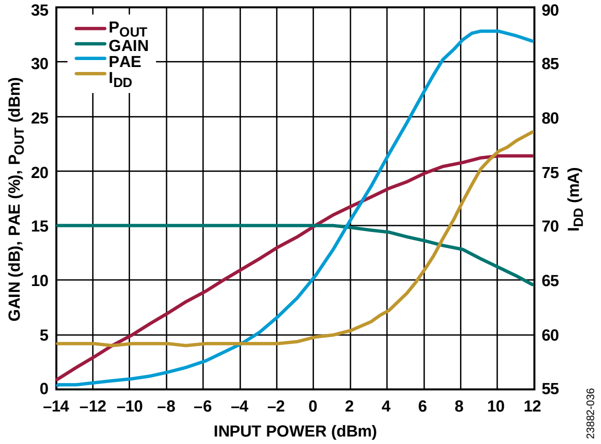


Figure 36. Gain, PAE, P_{OUT}, and I_{DD} vs. Input Power, Power Compression at 6 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

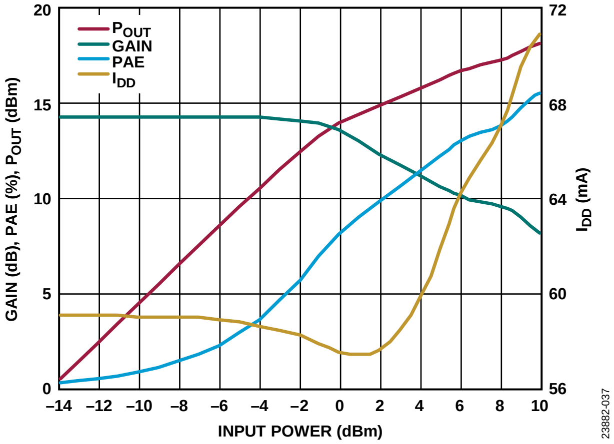


Figure 37. Gain, PAE, P_{OUT}, and I_{DD} vs. Input Power, Power Compression at 10 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

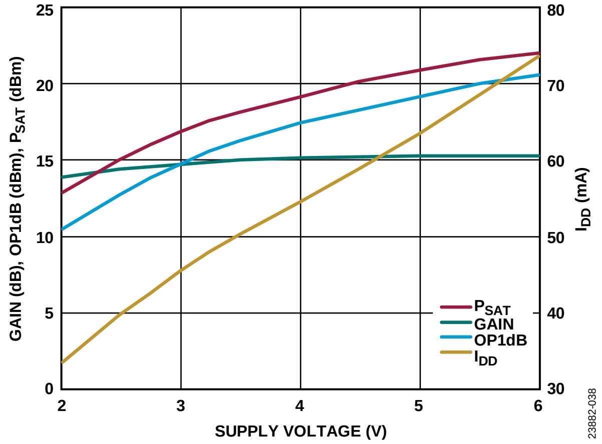


Figure 38. Gain, OP1dB, P_{SAT}, and I_{DD} vs. Supply Voltage, Power Compression at 3 GHz, R_{BIAS} = 1.47 kΩ

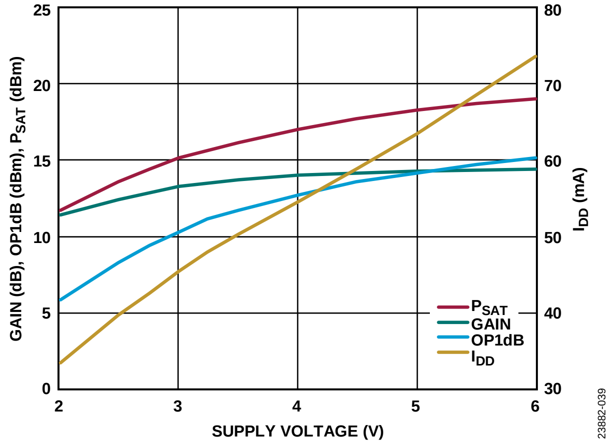


Figure 39. Gain, OP1dB, P_{SAT}, and I_{DD} vs. Supply Voltage, Power Compression at 10 GHz, R_{BIAS} = 1.47 kΩ

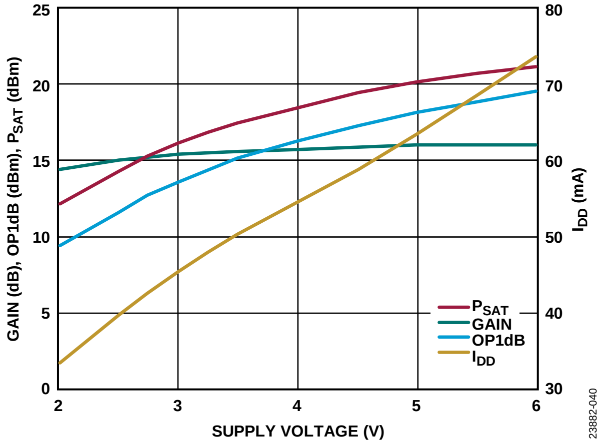


Figure 40. Gain, OP1dB, P_{SAT}, and I_{DD} vs. Supply Voltage, Power Compression at 1 GHz, R_{BIAS} = 1.47 kΩ

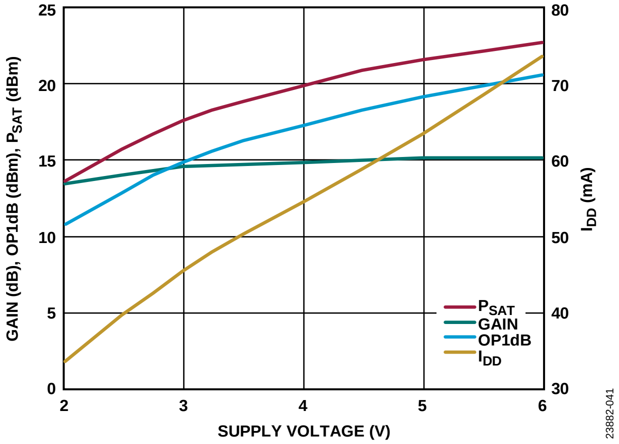


Figure 41. Gain, OP1dB, P_{SAT}, and I_{DD} vs. Supply Voltage, Power Compression at 6 GHz, R_{BIAS} = 1.47 kΩ

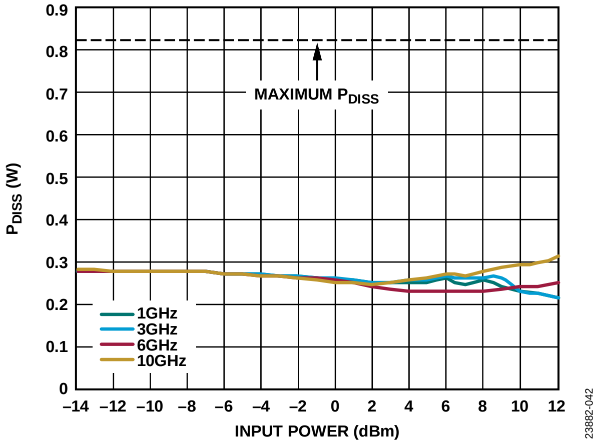


Figure 42. P_{DISS} vs. Input Power at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ

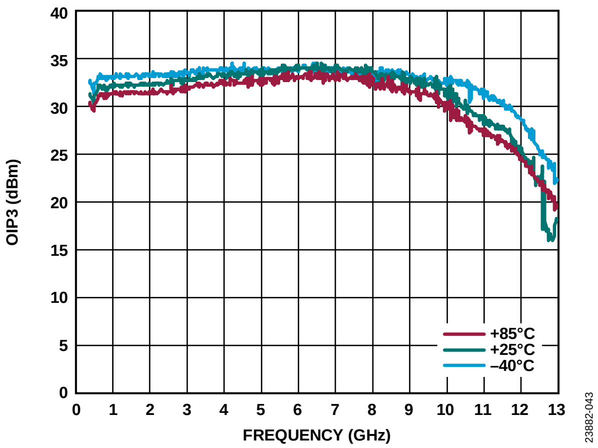


Figure 43. OIP3 vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ, P_{OUT} per Tone = 0 dBm

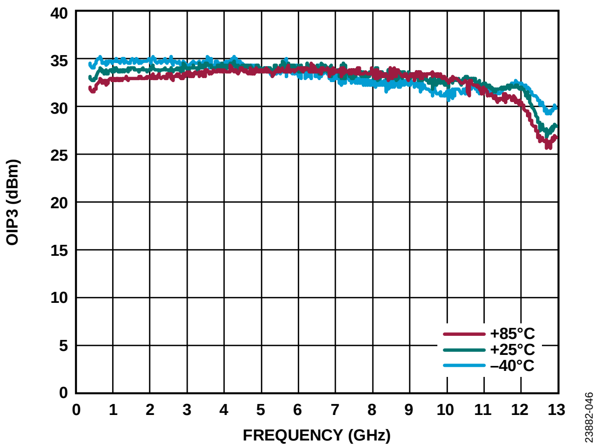


Figure 46. OIP3 vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 70 mA, R_{BIAS} = 1 kΩ, P_{OUT} per Tone = 0 dBm

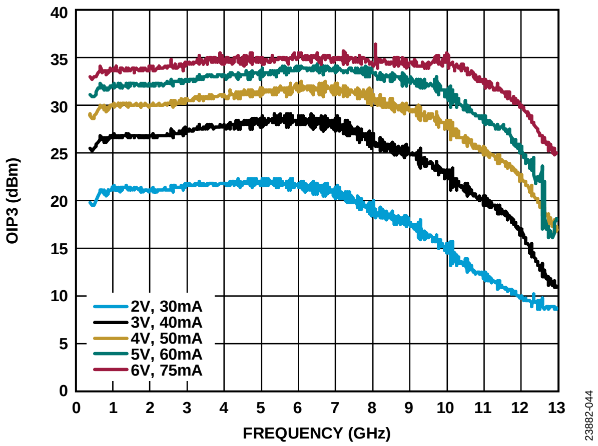


Figure 44. OIP3 vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ, P_{OUT} per Tone = 0 dBm

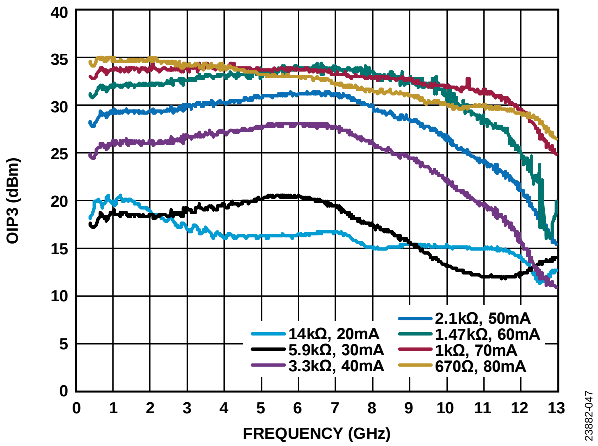


Figure 47. OIP3 vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V, P_{OUT} per Tone = 0 dBm

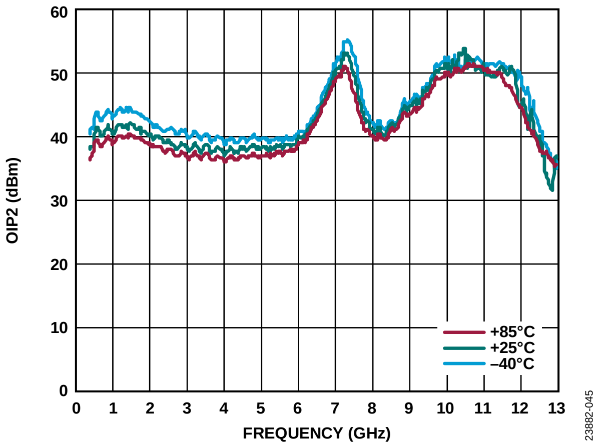


Figure 45. OIP2 vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 60 mA, R_{BIAS} = 1.47 kΩ, P_{OUT} per Tone = 0 dBm

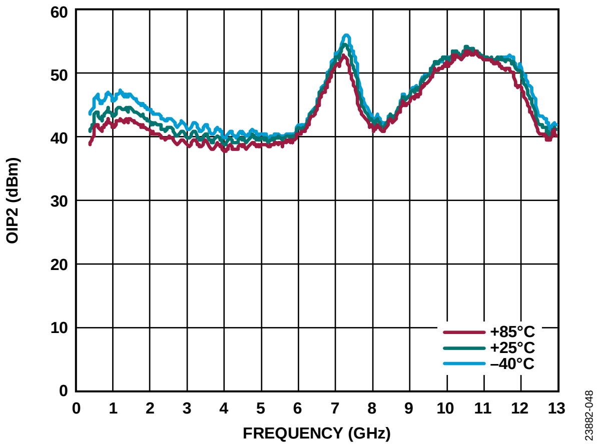


Figure 48. OIP2 vs. Frequency for Various Temperatures, 300 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 70 mA, R_{BIAS} = 1 kΩ, P_{OUT} per Tone = 0 dBm

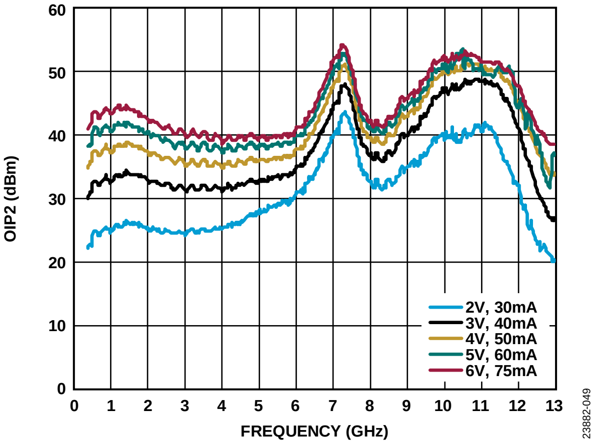


Figure 49. OIP2 vs. Frequency for Various V_{DD} and I_{DQ} Values, 300 MHz to 13 GHz, R_{BIAS} = 1.47 kΩ, P_{OUT} per Tone = 0 dBm

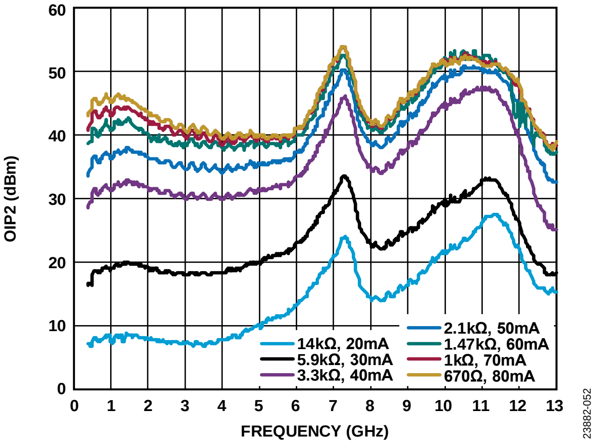


Figure 52. OIP2 vs. Frequency for Various R_{BIAS} Values and I_{DQ}, 300 MHz to 13 GHz, V_{DD} = 5 V, P_{OUT} per Tone = 0 dBm

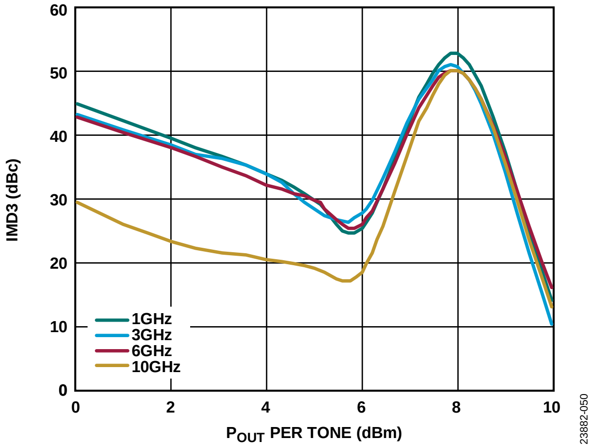


Figure 50. Third-Order Intermodulation Distortion Relative to Carrier (IMD3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, R_{BIAS} = 1.47 kΩ

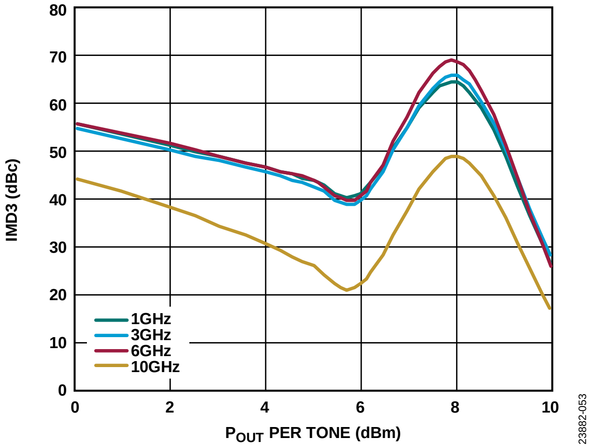


Figure 53. IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, R_{BIAS} = 1.47 kΩ

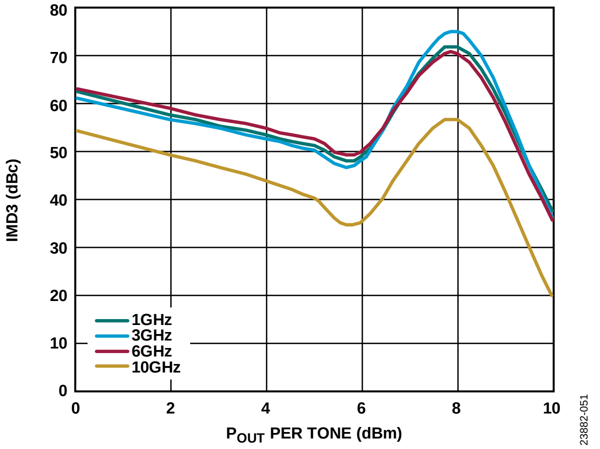


Figure 51. IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 4 V, R_{BIAS} = 1.47 kΩ

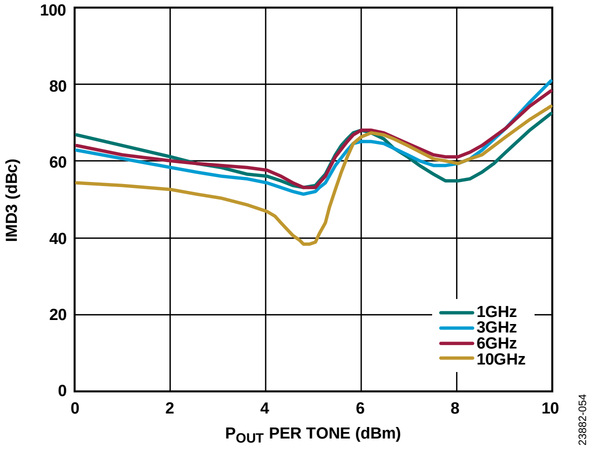


Figure 54. IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 1.47 kΩ

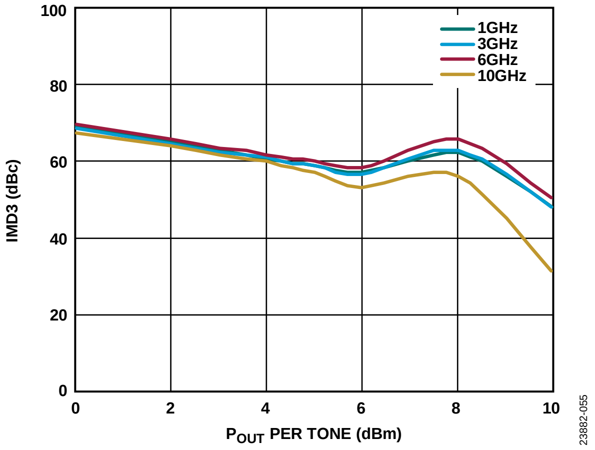


Figure 55. IMD3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 6 V, R_{BIAS} = 1.47 kΩ

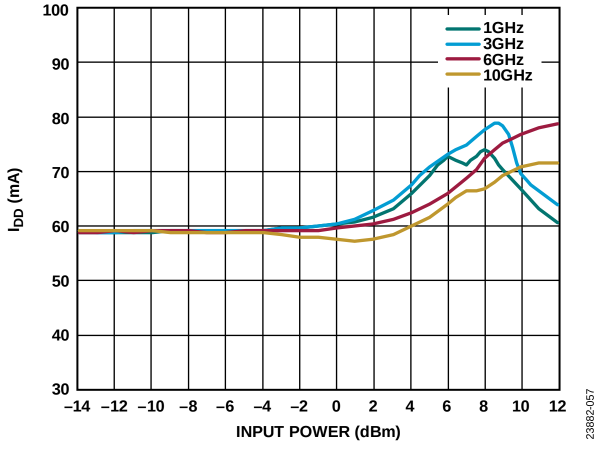


Figure 57. I_{DD} vs. Input Power for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 1.47 kΩ

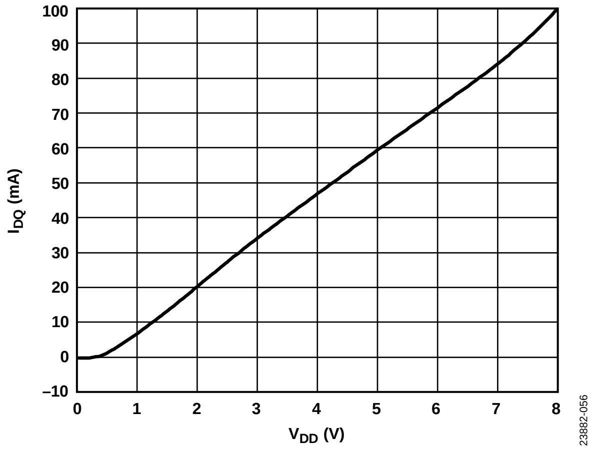


Figure 56. I_{DQ} vs. V_{DD}, R_{BIAS} = 1.47 kΩ

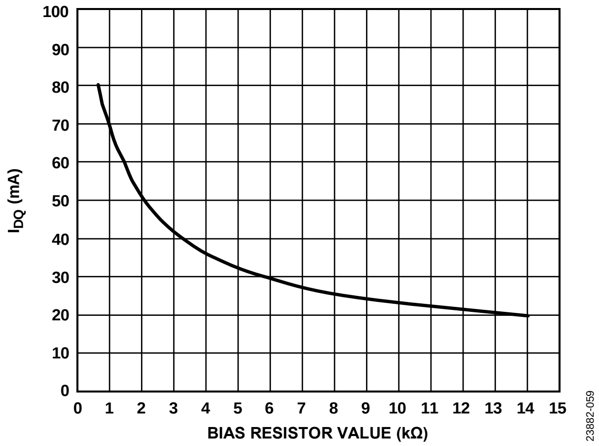


Figure 58. I_{DQ} vs. Bias Resistor Value, V_{DD} = 5 V

THEORY OF OPERATION

The HMC8412 is a GaAs, MMIC, pHEMT, low noise wideband amplifier with integrated ac-coupling capacitors and a bias inductor. A simplified schematic is shown in Figure 59.

The HMC8412 has ac-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 0.4 GHz to 11 GHz frequency range. No external matching components are required. To adjust the drain bias current, connect an external resistor between the R_{BIAS} and V_{DD} pins.

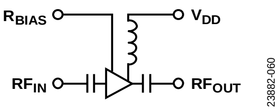


Figure 59. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the HMC8412 over the specified frequency range are shown in Figure 60. No external biasing inductor is required, allowing the 5 V supply to be connected to the V_{DD} pin. 0.1 µF and 100 pF power supply decoupling capacitors are recommended. The power supply decoupling capacitors shown in Figure 60 represent the configuration used to characterize and qualify the HMC8412. It is possible to reduce the number of capacitors, but this varies from system to system. It is recommended to first remove the largest capacitors that are farthest from the device when reducing the number of capacitors.

To set I_{DQ}, connect a resistor, R1, between the R_{BIAS} and V_{DD} pins. A default value of 1.47 kΩ is recommended, which results in a nominal I_{DQ} of 60 mA. Table 8 shows how the I_{DQ} and I_{DD} varies vs. the bias resistor value. The R_{BIAS} pin also draws a current that varies with the value of R_{BIAS} (see Table 8). Do not leave the R_{BIAS} pin open.

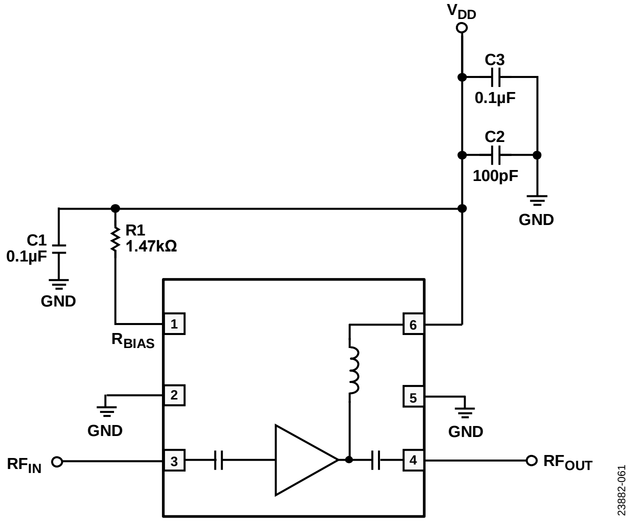


Figure 60. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

Power-Up Sequence

To power up, follow this bias sequence:

1. Set V_{DD} to 5 V.
2. Apply the RF signal.

Power-Down Sequence

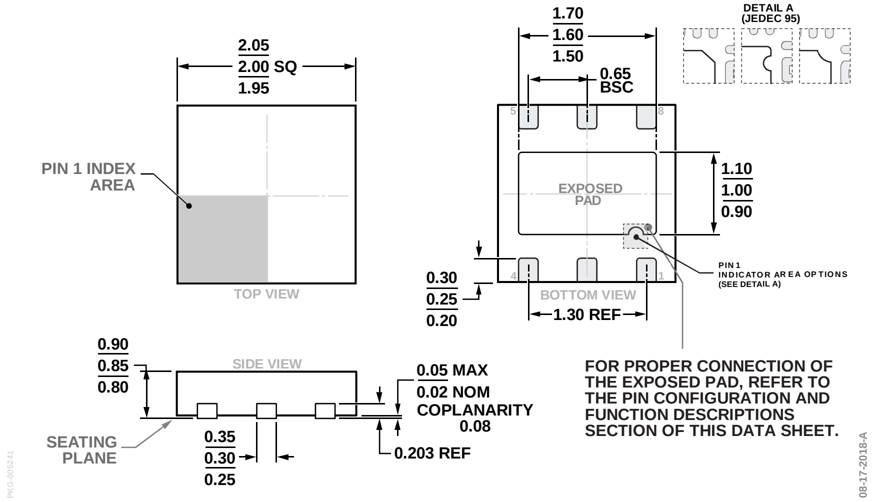
To power down, follow this bias sequence:

1. Turn off the RF signal.
2. Set V_{DD} to 0 V.

Table 8. Recommended Bias Resistor Values

R_{BIAS} (Ω)	Total Current (mA)	I_{DD} (mA)	R_{BIAS} Current (mA)
670	80	77.05	2.95
790	75	72.29	2.71
1000	70	67.53	2.47
1170	65	62.76	2.24
1470	60	58.04	1.96
1730	55	53.24	1.76
2100	50	48.45	1.55
2600	45	43.67	1.33
3300	40	38.89	1.11
4300	35	34.11	0.89
5900	30	29.38	0.62
8500	25	24.51	0.49
14000	20	19.69	0.31

OUTLINE DIMENSIONS



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 61. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-6-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description[4]	Package Option
HMC8412LP2FE	−40°C to +85°C	MSL1	6-Lead Lead Frame Chip Scale Package [LFCSP]	CP-6-12
HMC8412LP2FETR	−40°C to +85°C	MSL1	6-Lead Lead Frame Chip Scale Package [LFCSP]	CP-6-12
EV1HMC8412LP2F			Evaluation Board	

[1] The HMC8412LP2FE, HMC8412LP2FETR, and EV1HMC8412LP2F are RoHS compliant parts.
[2] When ordering the evaluation board only, reference the model number, EV1HMC8412LP2F.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC8412LP2FE and HMC8412LP2FETR is nickel palladium gold (NiPdAu).

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