# XR1020-QH

## Receiver
## 31 - 36 GHz

Rev. V1

### Features

- Integrated LNA, Mixer and LO Buffer Amplifier
- 3 dB Noise Figure
- 14 dB Conversion Gain
- Lead-Free 4 mm PQFN 24-lead Package
- RoHS* Compliant

### Description

The XR1020-QH is a 31 - 36 GHz receiver that has a noise figure of 3 dB and 14 dB conversion gain. The device integrates an LNA, image reject mixer and LO buffer amplifier within a fully molded lead-free 4 mm 24-lead PQFN package.

The image reject mixer eliminates the need for a bandpass filter after the LNA to remove thermal noise at the image frequency. I and Q mixer outputs are provided and an external 90° hybrid is required to select the desired sideband.

This device is well suited for Point-to-Point Radio, SATCOM and Military applications.

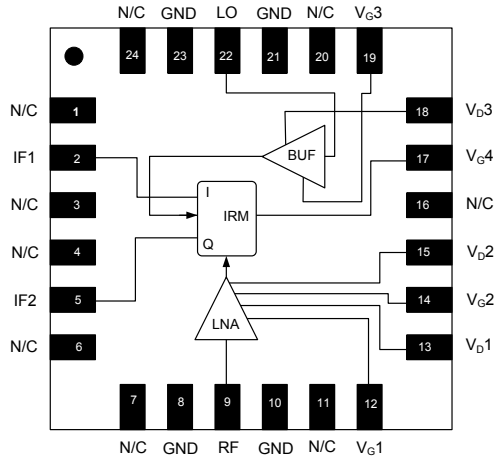
### Ordering Information[1,2]

| Part Number | Package |
|---|---|
| XR1020-QH-A000 | bulk quantity |
| XR1020-QH-TR0500 | 500 piece reel |
| XR1020-QH-TR1000 | 1000 piece reel |
| XR1020-QH-EV1 | evaluation module |

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

*Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

### Functional Schematic




### Pin Configuration[3]

| Pin No. | Function | Function |
|---|---|---|
| 1 | N/C | No Connection |
| 2 | IF1 | IF1 Output |
| 3 | N/C | No Connection |
| 4 | N/C | No Connection |
| 5 | IF2 | IF2 Output |
| 6 | N/C | No Connection |
| 7 | N/C | No Connection |
| 8 | GND | Ground |
| 9 | RF | RF Input |
| 10 | GND | Ground |
| 11 | N/C | No Connection |
| 12 | $V_G1$ | Gate LNA Stage 1 |
| 13 | $V_D1$ | Drain LNA Stage 1 |
| 14 | $V_G2$ | Gate LNA Stage 2 |
| 15 | $V_D2$ | Drain LNA Stage 2 |
| 16 | N/C | No Connection |
| 17 | $V_G4$ | Mixer Bias |
| 18 | $V_D3$ | Drain, LO Buffer |
| 19 | $V_G3$ | Gate, LO Buffer |
| 20 | N/C | No Connection |
| 21 | GND | Ground |
| 22 | LO | LO Input |
| 23 | GND | Ground |
| 24 | N/C | No Connection |
| 25[4] | Paddle | Ground |

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.

## Electrical Specifications:[5] $T_B$ = +25°C, $V_D$1,2,3 = 3 V, $V_G$4 = -3 V, IF = 2 GHz

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Frequency Range (RF) | GHz | 31 | - | 36 |
| Frequency Range (LO) | GHz | 27.5 | - | 39.5 |
| Frequency Range (IF) | GHz | DC | - | 3.5 |
| Conversion Gain<br>RF = 34 GHz, LO = 32 GHz | dB | 11.0 | 13.5 | - |
| Noise Figure<br>RF = 34 GHz, LO = 32 GHz | dB | - | 3 | 4.5 |
| LO Input Power | dBm | - | 4 | - |
| Input Third Order Intercept | dBm | - | -2 | - |
| Image Rejection | dBc | - | 20 | - |
| LO/RF Isolation | dB | - | -30 | - |
| RF Input Return Loss | dB | - | 10 | - |
| LO Input Return Loss | dB | - | 10 | - |
| IF Return Loss | dB | - | 12 | - |
| Supply Current ($I_D$1 + $I_D$2 + $I_D$3) | mA | - | 105 | - |

5. Apply gate voltages prior to drain voltages. Adjust $V_G$1, $V_G$2, $V_G$3 between -1.0 and -0.1 V to achieve specific drain current. Typical drain current: 105 mA = 10 mA ($I_D$1) + 30 mA ($I_D$2) + 65 mA ($I_D$3). Refer to App Note [1] for biasing details.

## Absolute Maximum Ratings[6,7,8]

| Parameter | Absolute Max. |
|---|---|
| Drain Voltage ($V_D$1,2,3) | +4.3 V |
| Drain Current ($I_D$1,2,3) | 200 mA |
| Gate Voltage ($V_G$1,2,3) | -1.7 to 0 V |
| Gate Voltage ($V_G$4) | -4 V |
| RF Input Power | 5 dBm |
| LO Input Power | 13 dBm |
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -55°C to +85°C |
| Channel Temperature | +150ºC |

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF > 1 x $10^6$ hours.

## App Note [1] Biasing -

As shown in the Pin Configuration table, the XR1020-QH is operated by biasing $V_D$1,2,3 at 3 V with 10, 30, 65 mA respectively. Additionally, a fixed voltage bias of -3 V is required for mixer bias. It is recommended to use active bias on $V_G$1, $V_G$2, and $V_G$3 to keep the currents in $V_D$1, $V_D$2, and $V_D$3 constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.4 V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

## App Note [2] Board Layout -

It is recommended to provide 100 pF decoupling capacitors as close to the bias pins as possible (see board layout), 10 µF capacitors can be added further along the DC lines.

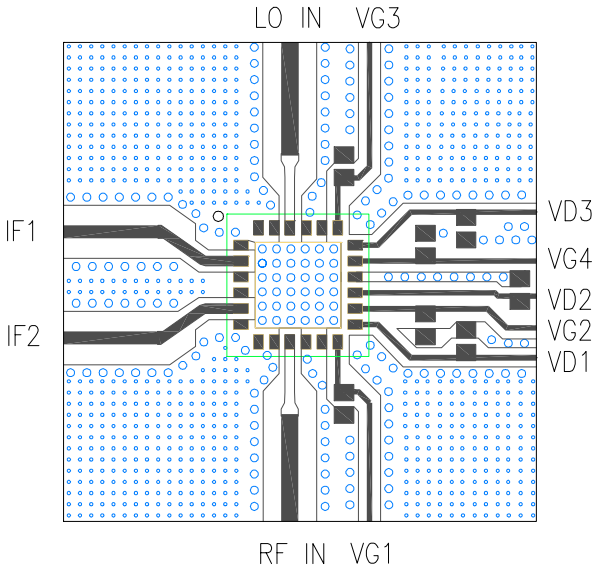
## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

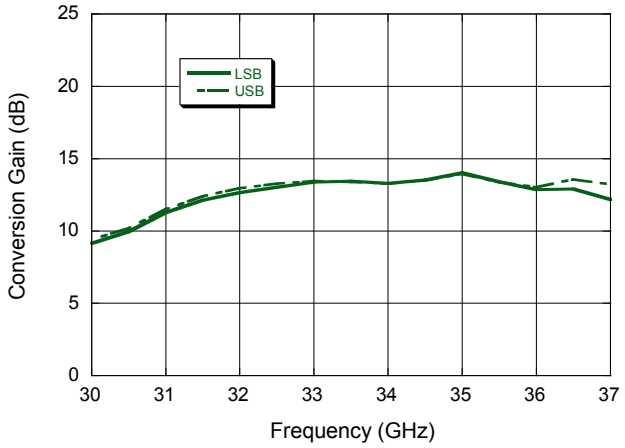
## Recommended Board Layout[9,10]



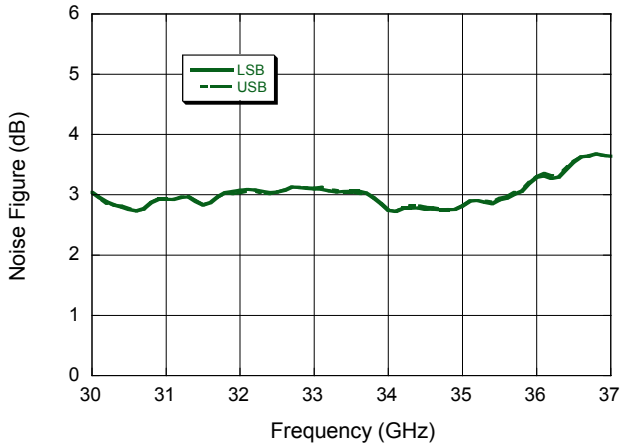

9. Recommended decoupling capacitors:
   100 pF, 0402
   10 µF, 0805 (optional)
10. Recommend to externally ground all N/C pins.

## Typical Performance Curves

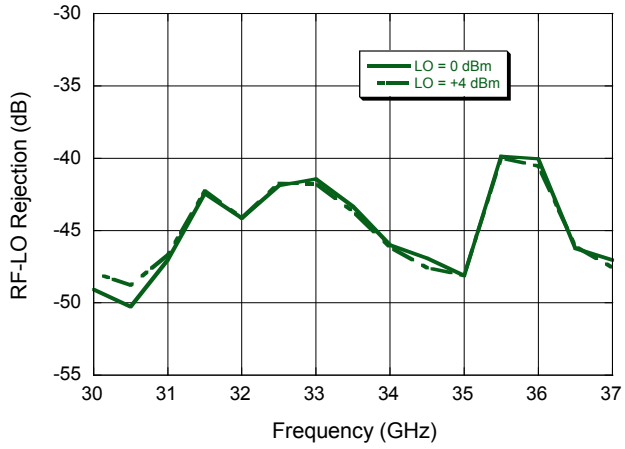
***Conversion Gain, IF = 2 GHz***



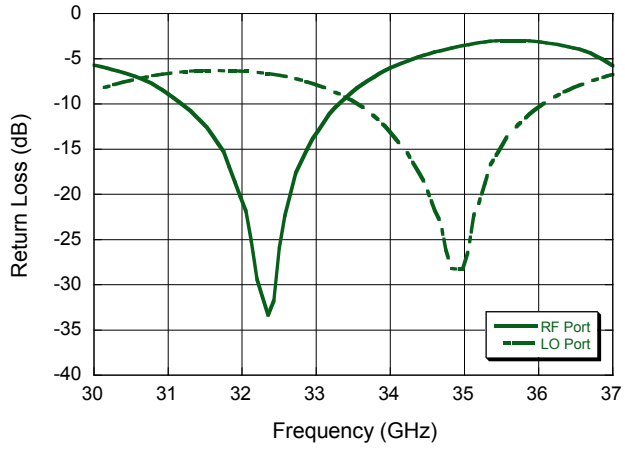

***Noise Figure, IF = 2 GHz***




***RF-LO Rejection***

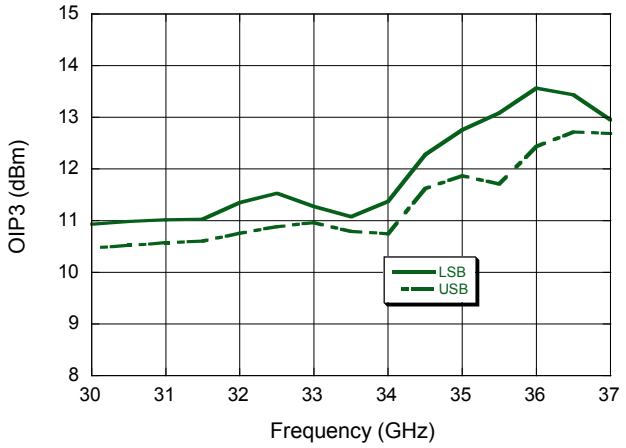



***RF and LO Return Loss***



## Typical Performance Curves

***Output IP3, IF = 120 MHz***




***Input IP3, IF = 120 MHz***

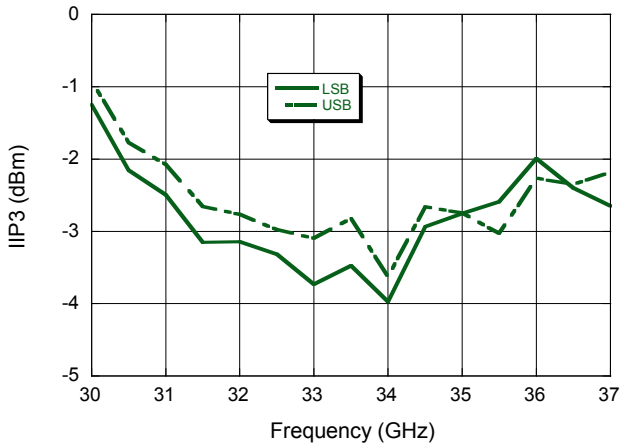
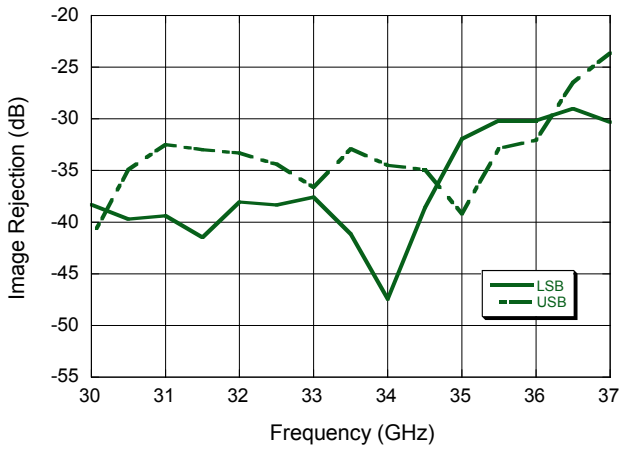
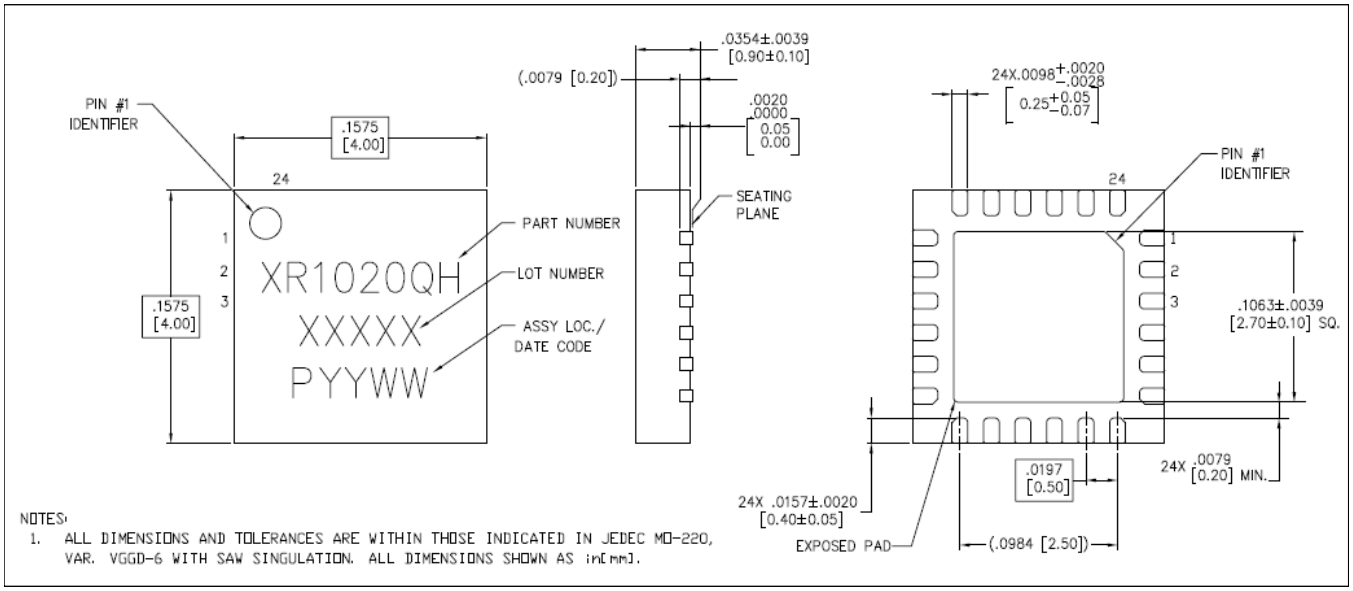



***Image Rejection, IF = 120 MHz***



## *Lead-Free* Package Dimensions/Layout†




† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is 100% matte tin.