20A Synchronous Step-Down COT Regulators

Description

The XR76121 is a synchronous step-down regulator combining the controller, drivers, bootstrap diode and MOSFETs in a single package for point-of-load supplies. The XR76121 has a load current rating of 20A. A wide 5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V and 19.6V rails.

With a proprietary emulated current mode constant on-time (COT) control scheme, the XR76121 provides extremely fast line and load transient response using ceramic output capacitors. They require no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.1% load and 0.1% line regulation and maintains constant operating frequency. A selectable power saving mode, allows the user to operate in discontinuous mode (DCM) at light current loads thereby significantly increasing the converter efficiency.

A host of protection features, including overcurrent, over temperature, overvoltage, short-circuit, open feedback detect and UVLO, helps achieve safe operation under abnormal operating conditions.

The XR76121 is available in a RoHS compliant, green/halogen-free space-saving 5mm x 6mm QFN package.

FEATURES

- 20A step-down regulator
  - 4.5V to 5.5V low V_{IN} operation
  - 5V to 22V wide single input voltage
  - 3V to 22V operation with external 5V bias
  - ≥0.6V adjustable output voltage
- Proprietary constant on-time control
  - No loop compensation required
  - Ceramic output capacitor stable operation
  - Programmable 70ns-1µs on-time
  - Constant 200kHz-1MHz frequency
  - Selectable CCM or CCM/DCM operation
- Power-good flag with low impedance when power removed
- Precision enable
- Programmable soft-start
- 5mm x 6mm QFN package

APPLICATIONS

- Servers
- Distributed power architecture
- Point-of-load converters
- FPGA, DSP and processor supplies
- Base stations, switches/routers

Typical Application

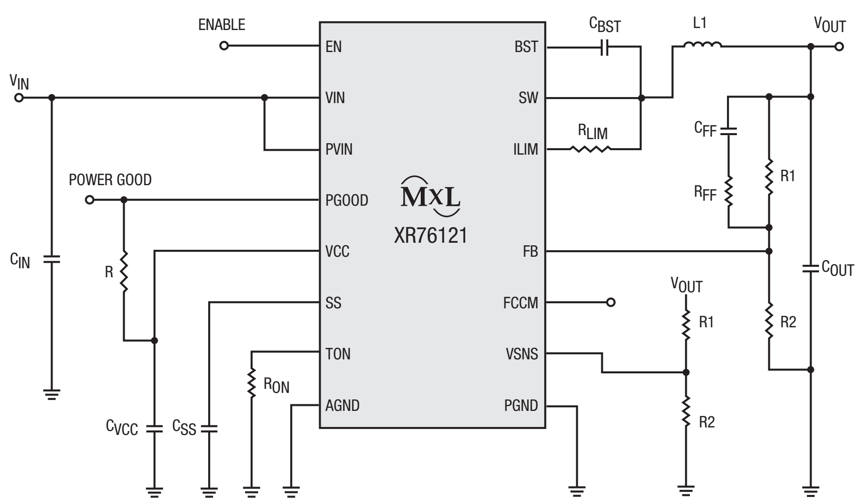


Figure 1. Typical Application

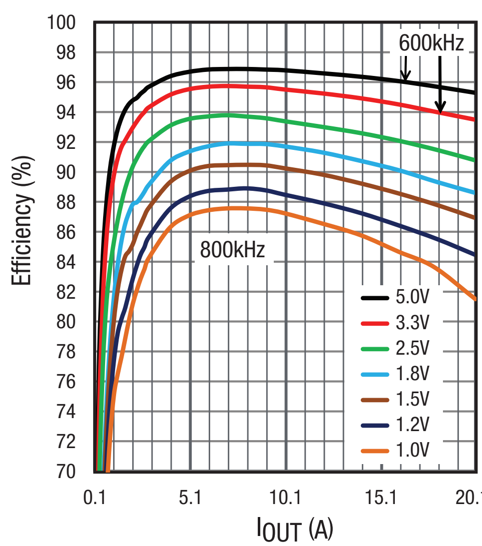


Figure 2. Efficiency

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} .... -0.3V to 25V

V_{CC} .... -0.3V to 6.0V

BST .... -0.3V to 31V(1)

BST-SW .... -0.3V to 6V

SW, ILIM .... -1V to 25V(1)(2)

All other pins .... -0.3V to V_{CC} + 0.3V

Storage temperature .... -65°C to 150°C

Junction temperature .... 150°C

Power dissipation .... Internally limited

Lead temperature (soldering, 10 second) .... 300°C

ESD rating (HBM – human body model) 2kV

ESD rating (CDM – charged device model) 1kV

ESD rating (MM – machine model) 200V

Operating Conditions

PV_{IN} .... 3V to 22V

V_{IN} .... 4.5V to 22V

V_{CC} .... 4.5V to 5.5V

SW, ILIM .... -1V to 22V(2)

PGOOD, TON, SS, EN .... -0.3V to 5.5V(2)

Switching frequency .... 200kHz-1MHz(3)

Junction temperature range (T_J) .... -40°C to 125°C

Package power dissipation max at 25°C 4.1W

Package thermal resistance θ_{JA} .... 24°C/W(4)

NOTES:

1. No external voltage applied.
2. SW pin's DC range is -1V, transient is -5V for less than 50ns.
3. Recommended.
4. Measured on MaxLinear evaluation board.

Electrical Characteristics

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	V_{CC} regulating	•	5	12	22	V
		V_{CC} tied to V_{IN}		4.5	5.0	5.5	
I_{VIN}	V_{IN} supply current	Not switching, V_{IN} = 12V, V_{FB} = 0.7V	•		0.8	1.3	mA
I_{VCC}	V_{CC} quiescent current	Not switching, V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V	•		0.8	1.3	mA
I_{VIN}	V_{IN} supply current	f = 600kHz, R_{ON} = 49.9k, V_{FB} = 0.58V			17		mA
I_{OFF}	Shutdown current	Enable = 0V, PV_{IN} = V_{IN} = 12V			1		µA
Enable and Undervoltage Lock-Out UVLO							
V_{IH_EN}	EN pin rising threshold		•	1.8	1.9	2.0	V
V_{EN_HYS}	EN pin hysteresis				60		mV
	V_{CC} UVLO start threshold, rising edge		•	4.00	4.25	4.40	V
	V_{CC} UVLO hysteresis		•	100	170		mV

Electrical Characteristics (Continued)

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

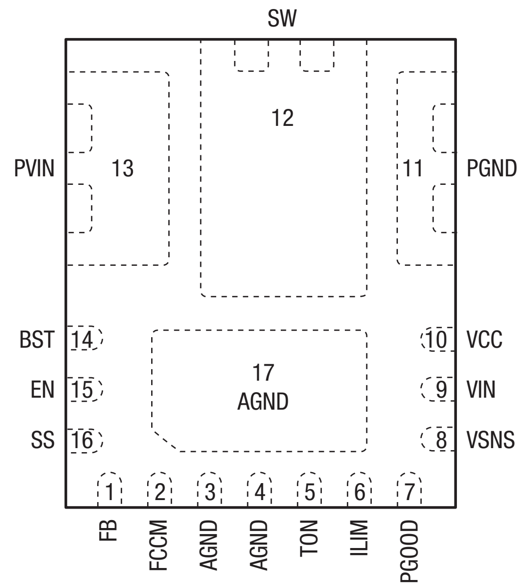
Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5V - 22V, V_{CC} regulating		0.597	0.600	0.603	V
		V_{IN} = 4.5V - 5.5V, V_{CC} tied to V_{IN}		0.596	0.600	0.604	V
		V_{IN} = 5V - 22V, V_{CC} regulating V_{IN} = 4.5V - 5.5V, V_{CC} tied to V_{IN}	•	0.594	0.600	0.606	V
	DC load regulation	CCM operation, closed loop, applies to any C_{OUT}			±0.1		%
	DC line regulation				±0.1		%
Programmable Constant On-Time							
	On-time 1	R_{ON} = 5.90kΩ, V_{IN} = 12V	•	170	200	230	ns
	f corresponding to on-time 1	V_{OUT} = 1.0V		360	415	490	kHz
	On-time 2	R_{ON} = 16.2kΩ, V_{IN} = 12V	•	425	500	575	ns
	f corresponding to on-time 2	V_{OUT} = 3.3V		478	550	647	kHz
	On-time 3	R_{ON} = 3.01kΩ, V_{IN} = 12V	•	90	110	135	ns
	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test			-2		mV
Soft-Start							
I_{SS_CHARGE}	Charge current		•	-14	-10	-6	µA
$I_{SS\_DISCHARGE}$	Discharge current	Fault present	•	1	3		mA
V_{CC} Linear Regulator							
V_{CC}	Output voltage	V_{IN} = 6V to 22V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5V, R_{ON} = 16.2kΩ, f_{SW} = 678kHz	•	4.6	4.8		
Power Good Output							
	Power good threshold			-10	-7.5	-5	%
	Power good hysteresis				1	4	%
	Power good	Minimum I_{SINK} = 1mA				0.2	V
	Power good, unpowered	I_{SINK} = 1mA				0.5	V
	Power good assertion delay, FB rising				2		ms
	Power good de-assertion delay, FB falling				65		µs

Electrical Characteristics (Continued)

Specifications are for operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a •. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V, SW = AGND = PGND = 0V, C_{VCC} = 4.7uF.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Mode Control (FCCM)							
	FCCM mode logic high threshold	FCCM rising	•	2.4			V
	FCCM mode logic low threshold	FCCM falling	•			0.4	V
	Input leakage current				100		nA
Open Feedback/OVP Detect (VSNS)							
	OVP trip high threshold	VSNS rising. Specified as % of V_{REF}	•	115	120	125	%
	OVP trip low threshold	VSNS falling. Specified as % of V_{REF}	•		115		%
	OVP comparator delay	VSNS rising	•	0.5	1	3.5	µs
	Delay to turn off power stage from an overvoltage event	VSNS rising	•			3.5	µs
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	I_{LIM}/R_{DS}			14.5	16.2	18.0	µA/mΩ
	I_{LIM} current temperature coefficient				0.4		%/°C
	I_{LIM} comparator offset			-4.7	0	4.7	mV
	I_{LIM} comparator offset		•	-8.0	0	8.0	mV
	Current limit blanking				100		ns
	Thermal shutdown threshold	Rising temperature			138		°C
	Thermal hysteresis				15		°C
	Feedback pin short-circuit threshold	Percent of V_{REF}, short circuit is active. After PGOOD asserts high.	•	50	60	70	%
Output Power Stage							
	High-side MOSFET $R_{DS(ON)}$	I_{DS} = 2A			7.7	10	mΩ
	Low-side MOSFET $R_{DS(ON)}$	I_{DS} = 2A			3.1	3.5	mΩ
	Maximum output current		•	20			A

Pin Configuration



Pin Functions

Pin Number	Pin Name	Type	Description
1	FB	A	Feedback input to feedback comparator.
2	FCCM	I	Forcing this pin logic level high forces CCM operation.
3	AGND	A	Signal ground for control circuitry. Connect to AGND pad with a short trace.
4			
5	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
6	ILIM	A	Overcurrent protection programming. Connect with a resistor to SW.
7	PGOOD	OD	Power-good output. Open drain to AGND. Low Z when IC unpowered.
8	VSNS	A	Sense pin for output OVP and open FB.
9	VIN	A	Supply input for the regulator's LDO. Normally connected to PV_{IN}.
10	VCC	A	The output of regulators LDO. It requires a 4.7µF V_{CC} bypass capacitor. For operation using a 5V rail, VCC should be tied to VIN.
11	PGND	PWR	Ground of the power stage. Internally connected to source of the low-side MOSFET.
12	SW	PWR	Switch node. Internally it connects source of the high-side MOSFET to drain of the low-side MOSFET.
13	PVIN	PWR	Input voltage for power stage. Internally connected to drain of the high-side MOSFET.
14	BST	A	High-side driver supply pin. Connect a 0.1µF bootstrap capacitor between BST and SW.
15	EN	I	Precision enable pin. Pulling this pin above 2V will enable the regulator.
16	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.
17	AGND PAD	A	Signal ground for control circuitry.

NOTE:
A = Analog, I = Input, O = Output, OD = Open Drain, PWR = Power.

Typical Performance Characteristics

Efficiency and Package Thermal Derating

Unless otherwise specified: $T_{AMBIENT}$ = 25°C, no airflow, f = 800kHz. Efficiency data includes inductor losses, schematic from the Application Information section of this datasheet.

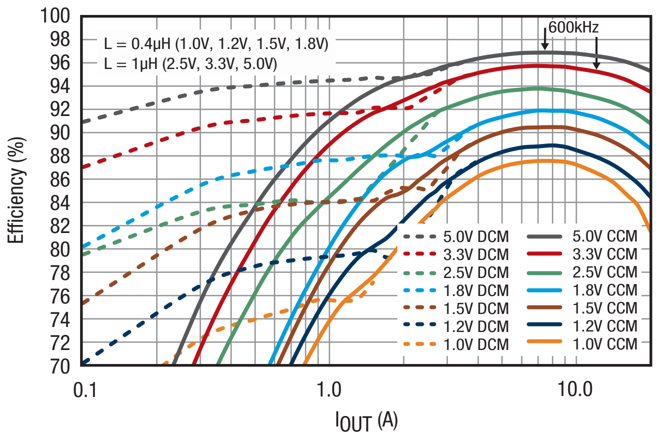


Figure 3. Efficiency, V_{IN} = 12V

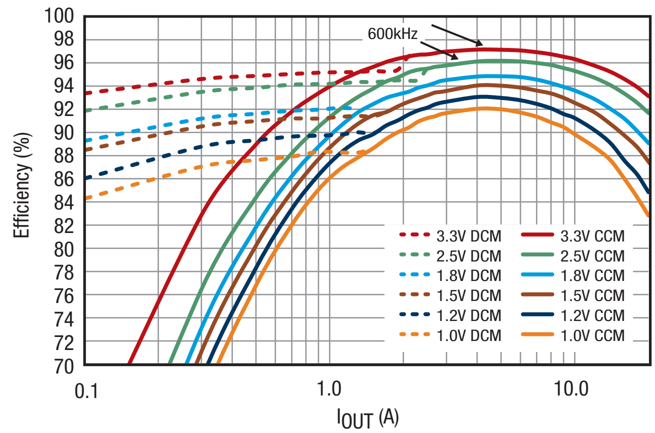


Figure 4. Efficiency, V_{IN} = 5V, L = 0.4µH

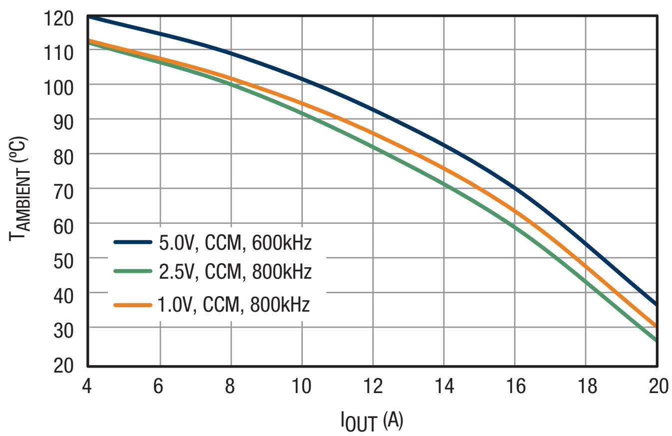


Figure 5. Maximum $T_{AMBIENT}$ vs. I_{OUT}, V_{IN} = 12V, No Airflow

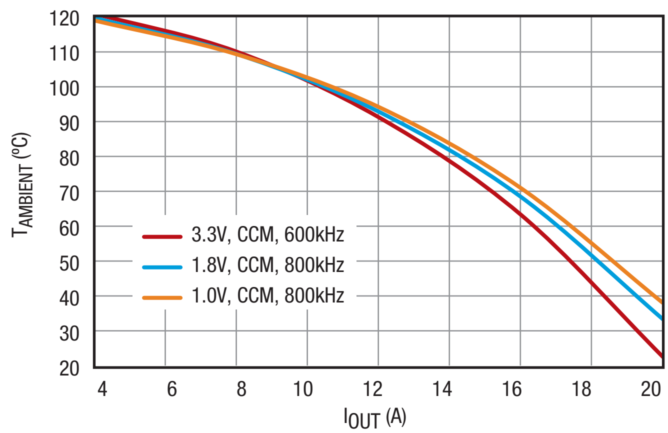


Figure 6. Maximum $T_{AMBIENT}$ vs. I_{OUT}, V_{IN} = 5V, No Airflow

Typical Performance Characteristics (Continued)

All data taken at V_{IN} = 12V, V_{OUT} = 1.8V, f = 800kHz, T_A = 25°C, no airflow, forced CCM. (Unless otherwise specified). Schematic from the Applications Information section of this datasheet.

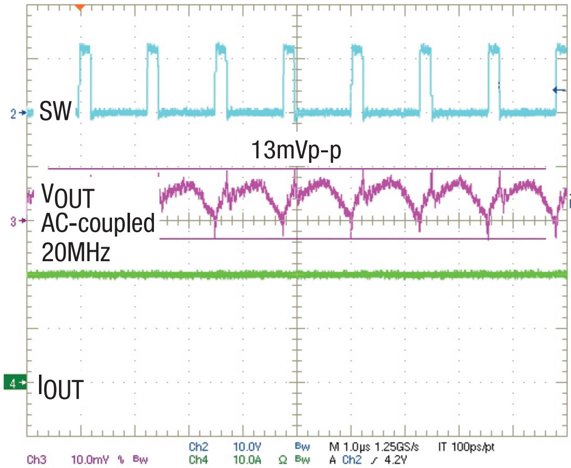


Figure 7. Steady State, I_{OUT} = 20A

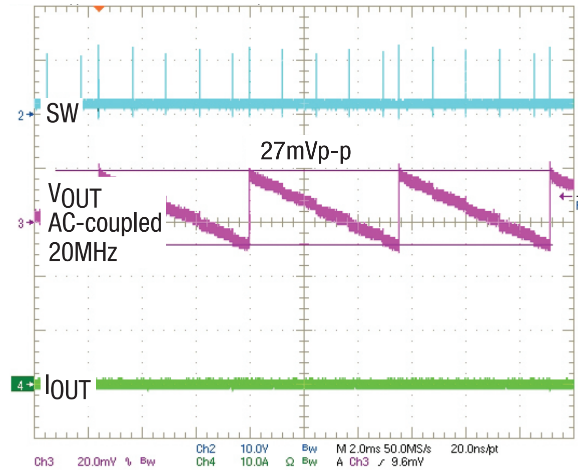


Figure 8. Steady State, DCM, I_{OUT} = 0A

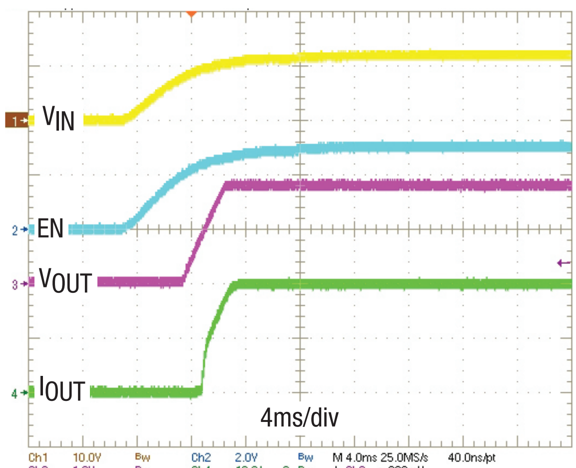


Figure 9. Power-Up, I_{OUT} = 20A

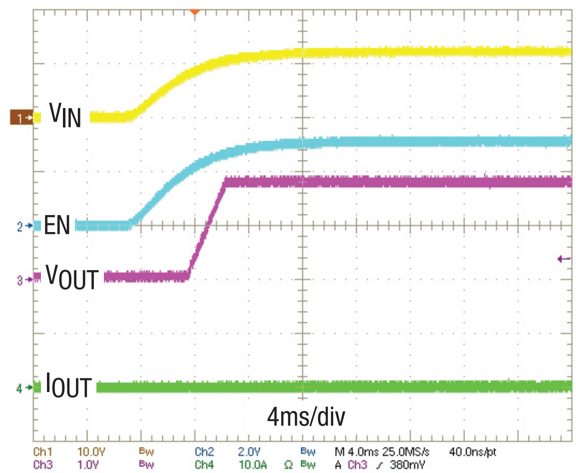


Figure 10. Power-Up, I_{OUT} = 0A

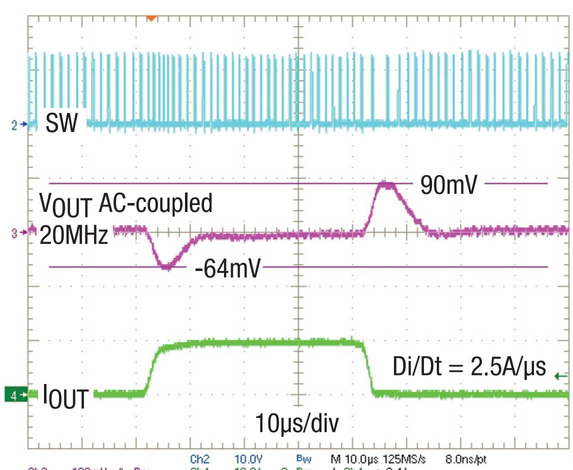


Figure 11. Load Transient, Forced CCM, 0A-10A-0A

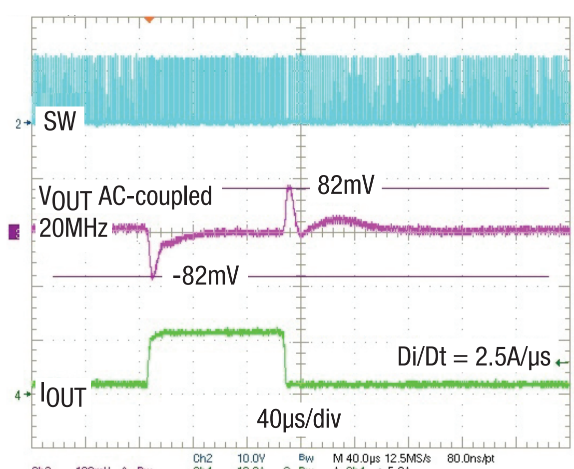


Figure 12. Load Transient, DCM, 1.8A-11.8A-1.8A

Typical Performance Characteristics (Continued)

All data taken at V_{IN} = 12V, V_{OUT} = 1.8V, f = 800kHz, T_A = 25°C, no airflow, forced CCM. (Unless otherwise specified). Schematic from the Applications Information section of this datasheet.

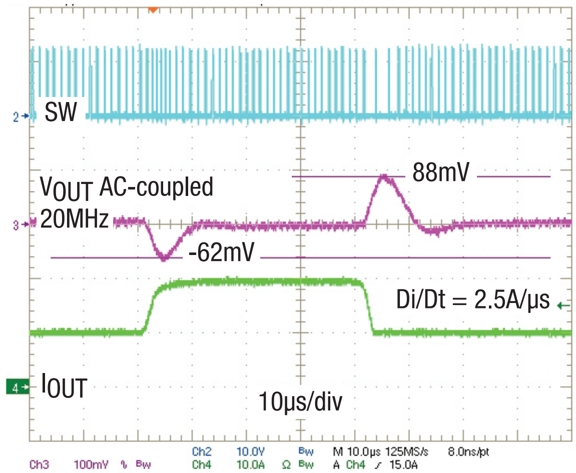


Figure 13. Load Transient, DCM or Forced CCM, 10A-20A-10A

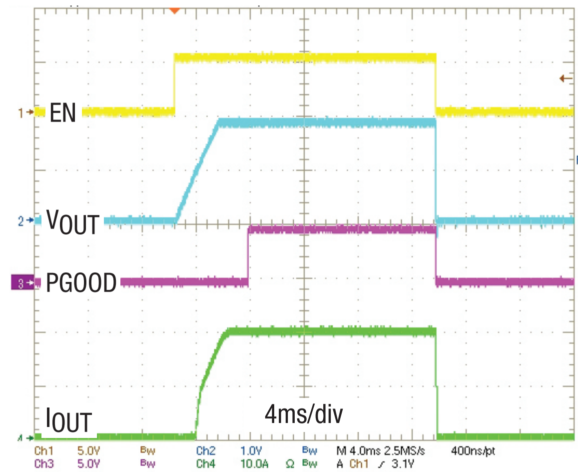


Figure 14. Enable Functionality, V_{IN} = 12V

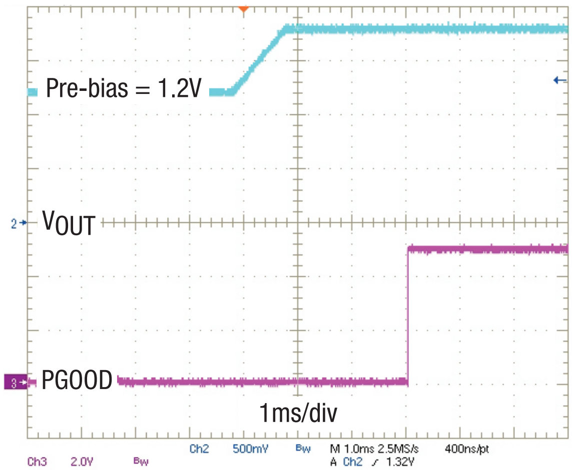


Figure 15. Power-Up with Pre-Bias Voltage, I_{OUT} = 0A

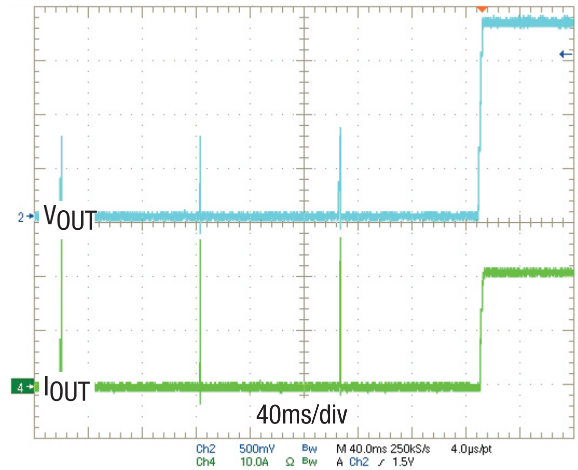


Figure 16. Short-Circuit Recovery, I_{OUT} = 20A

Typical Performance Characteristics (Continued)

All data taken at V_{IN} = 12V, V_{OUT} = 1.8V, f = 800kHz, T_A = 25°C, no airflow, forced CCM. (Unless otherwise specified). Schematic from the Applications Information section of this datasheet.

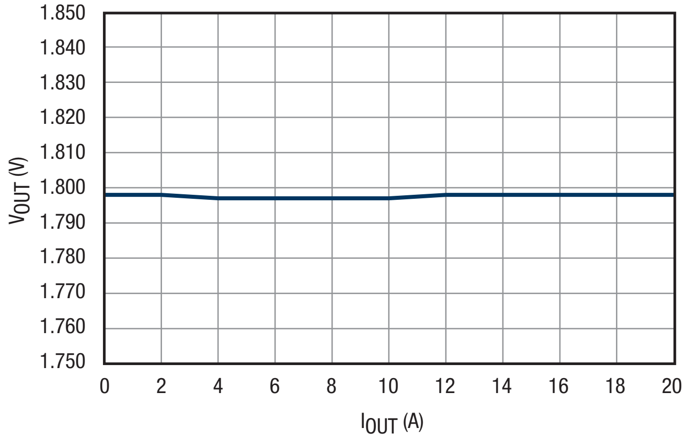


Figure 17. Load Regulation

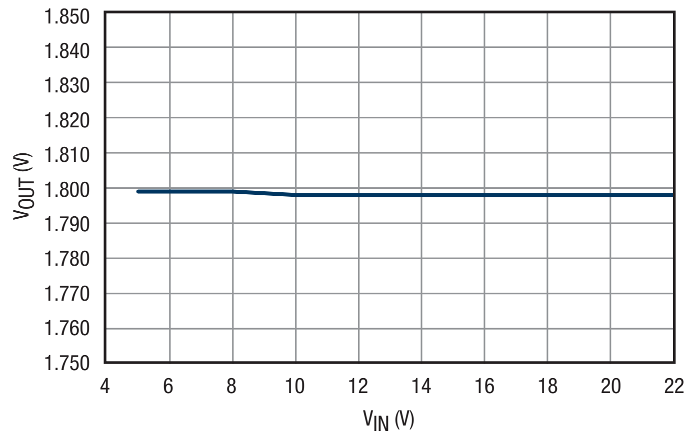


Figure 18. Line Regulation

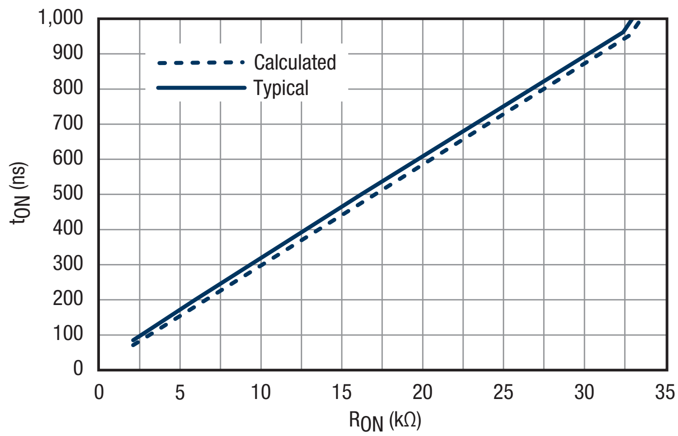


Figure 19. t_{ON} vs. R_{ON}

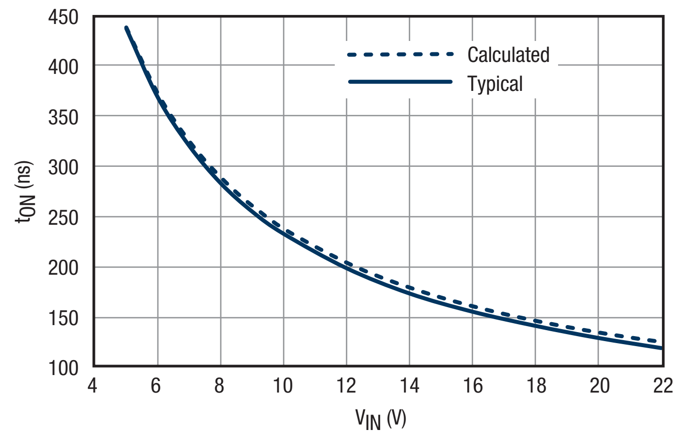


Figure 20. t_{ON} vs. V_{IN}, R_{ON} = 5.9kΩ

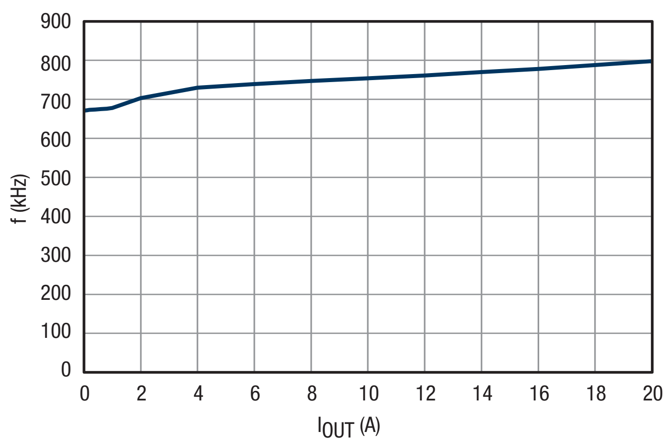


Figure 21. Frequency vs. I_{OUT}

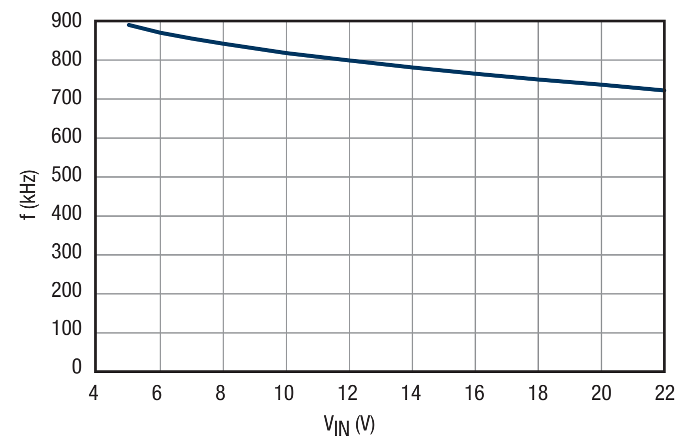


Figure 22. Frequency vs. V_{IN}

Typical Performance Characteristics (Continued)

All data taken at V_{IN} = 12V, V_{OUT} = 1.8V, f = 800kHz, T_A = 25°C, no airflow, forced CCM. (Unless otherwise specified). Schematic from the Applications Information section of this datasheet.

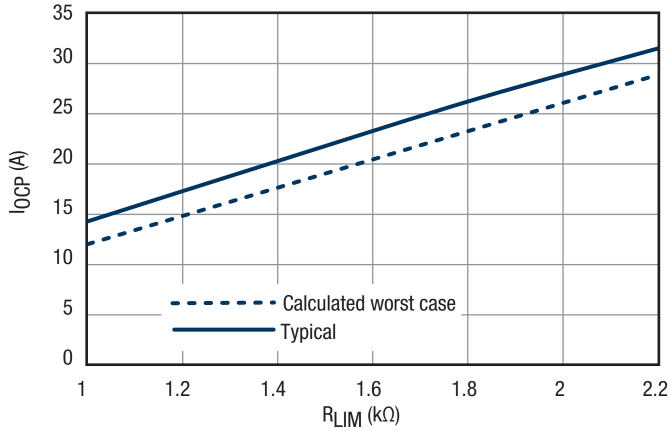


Figure 23. I_{OCP} vs. R_{LIM}

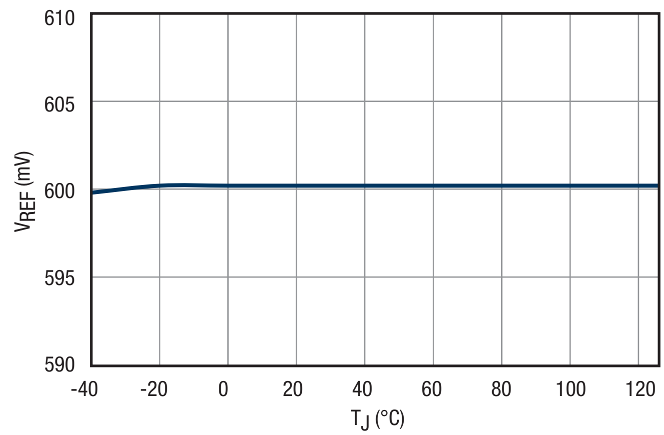


Figure 24. V_{REF} vs. Temperature

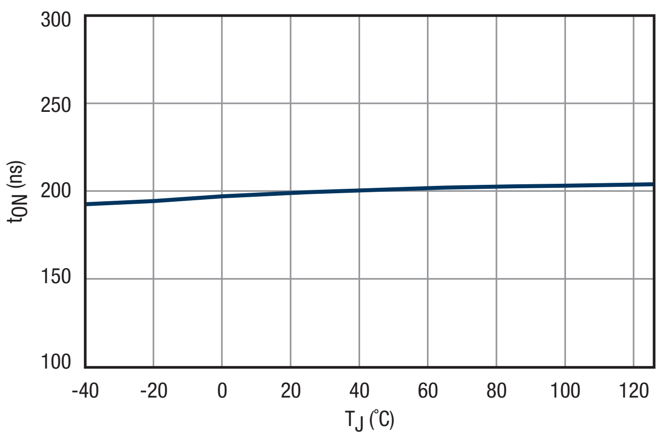


Figure 25. t_{ON} vs. Temperature, R_{ON} = 5.9k

Functional Block Diagram

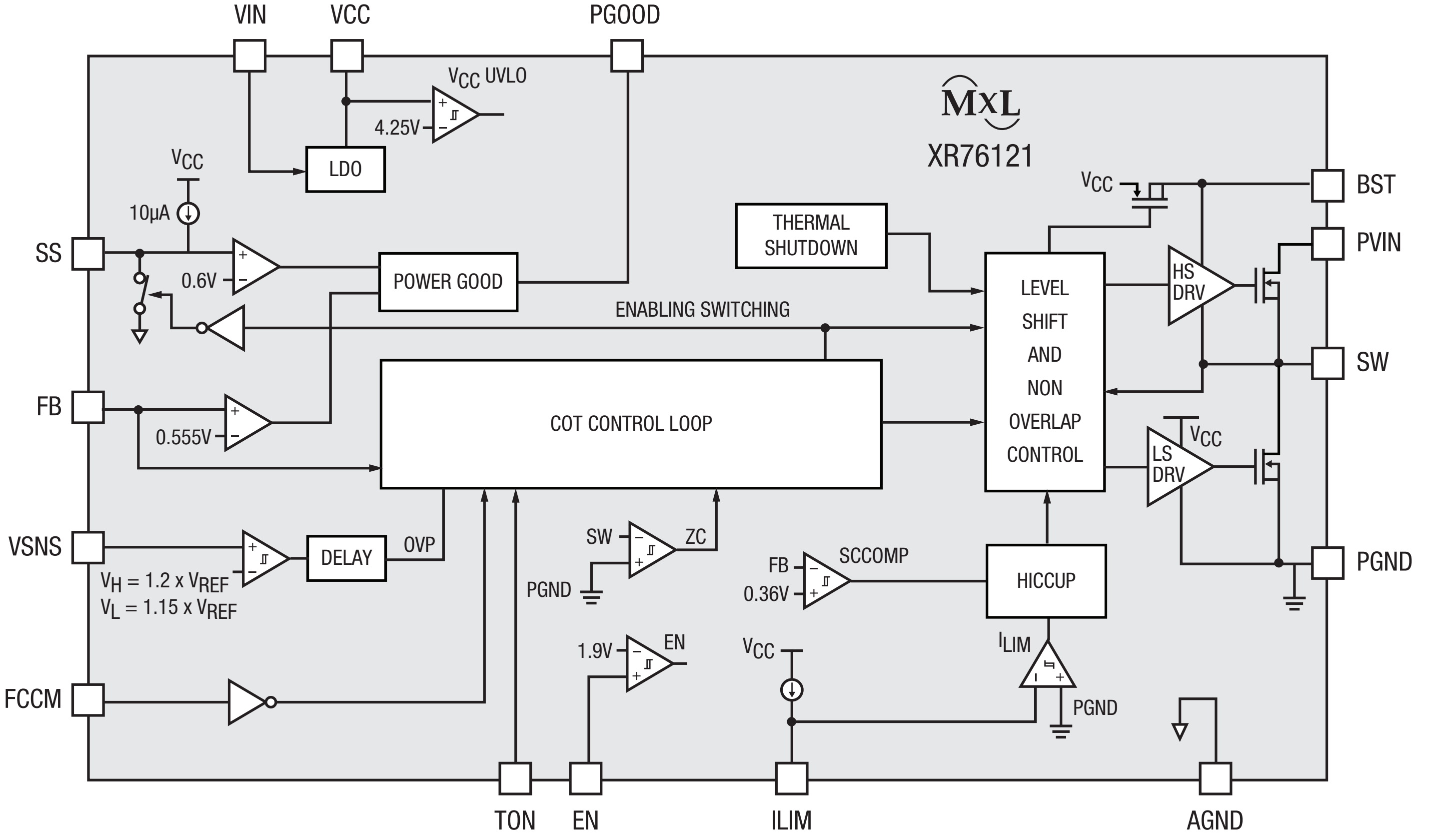


Figure 26. Functional Block Diagram

Applications Information

Detailed Operation

The XR76121 uses a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) control scheme. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with the high-side (switching) FET turning on for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed the minimum off-time. After the minimum off-time the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and allows for the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable

The enable input provides precise control for startup. Where bus voltage is well regulated, the enable input can be derived from this voltage with a suitable resistor divider. This ensures that XR76121 does not turn on until bus voltage reaches the desired level. Therefore the enable feature allows implementation of undervoltage lockout for the bus voltage PV_{IN}. Simple sequencing can be implemented by using the PGOOD signal as the enable input of a succeeding XR76121. Sequencing can also be achieved by using an external signal to control the enable pin.

Selecting the Forced CCM Mode

A voltage higher than 2.4V at the FCCM pin forces the XR76121 to operate in continuous conduction mode (CCM). Note that discontinuous conduction mode (DCM) is always on during soft-start. DCM will persist following soft-start until a sufficient load is applied to transition the regulator to CCM. Magnitude of the load required to transition to CCM is $\Delta I_L/2$, where ΔI_L is peak-to-peak inductor current ripple. Once the regulator transitions to CCM it will continue operating in CCM regardless of the load magnitude.

Selecting the DCM/CCM Mode

The DCM will always be available if a voltage less than 0.4V is applied to the FCCM pin. XR76121 will operate in either DCM or CCM depending on the load magnitude. At light loads DCM significantly increases efficiency as seen in Figures 3 and 4. A preload of 10mA is recommended for DCM operation. This helps improve voltage regulation when external load is less then 10mA and may reduce voltage ripple.

Programming the On-Time

The on-time t_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [t_{ON} - (2.5 \times 10^{-8})]}{3.45 \times 10^{-10}}$$

A graph of t_{ON} versus R_{ON}, using the above equation, is compared to typical test data in Figure 19. The graph shows that calculated data matches typical test data within 3%.

The t_{ON} corresponding to a particular set of operating conditions can be calculated based on empirical data from:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times 1.06 \times f \times Eff.}$$

Where:

- f is the desired switching frequency at nominal I_{OUT}.
- Eff. is the converter efficiency corresponding to nominal I_{OUT}.

Substituting for t_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{1.06 \times f \times Eff.}\right) - [(2.5 \times 10^{-8}) \times V_{IN}]}{(3.45 \times 10^{-10})}$$

Now R_{ON} can be calculated in terms of operating conditions V_{IN}, V_{OUT}, f and efficiency using the above equation.

At V_{IN} = 12V, f = 800kHz, I_{OUT} = 20A and using the efficiency numbers from Figure 3 we get the following R_{ON}:

V_{OUT} (V)	Eff. (%)	f (kHz)	R_{ON} (kΩ)
5.0	0.95	600	23.12
3.3	0.93	600	15.30
2.5	0.91	800	8.52
1.8	0.89	800	6.04
1.5	0.87	800	5.02
1.2	0.84	800	4.01
1.0	0.81	800	3.35

XR76121 R_{ON} for common output voltages, V_{IN} = 12V, I_{OUT} = 20A

Applications Information (Continued)

Overcurrent Protection (OCP)

If the load current exceeds the programmed overcurrent threshold I_{OCP} for four consecutive switching cycles, the regulator enters the hiccup mode of operation. In hiccup mode the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The regulator will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program overcurrent protection use the following equation:

$$R_{LIM} = \left[\frac{(I_{OCP} + (0.5 \times \Delta IL))}{\left(\frac{I_{LIM}}{R_{DS}} \right)} \right] + 0.16k\Omega$$

Where:

- R_{LIM} is resistor value in kΩ for programming I_{OCP}
- I_{OCP} is the overcurrent value to be programmed
- ΔI_L is the peak-to-peak inductor current ripple
- I_{LIM}/R_{DS} is the minimum value of the parameter specified in the tabulated data
- I_{LIM}/R_{DS} = 14.5uA/mΩ
- 0.16kΩ accounts for OCP comparator offset

The above equation is for worst-case analysis and safeguards against premature OCP. Typical value of I_{OCP}, for a given R_{LIM}, will be higher than that predicted by the above equation. Graph of calculated I_{OCP} vs. R_{LIM} is compared to typical I_{OCP} in Figures 23.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value (i.e., FB drops below 0.36V), the regulator will enter hiccup mode. Hiccup mode will persist until short-circuit is removed. The SCP circuit becomes active at the end of soft-start. Hiccup mode and short-circuit recovery waveform is shown in Figure 16.

Over Temperature Protection (OTP)

OTP triggers at a nominal controller temperature of 138°C. The gates of the switching FET and the synchronous FET are turned off. When controller temperature cools down to 123°C, soft-start is initiated and regular operation resumes.

Overvoltage Protection (OVP)

The output OVP function detects an overvoltage condition on V_{OUT} of the regulator. OVP is achieved by comparing the voltage at VSNS pin to an OVP threshold voltage set at 1.2 x V_{REF}. When VSNS voltage exceeds the OVP threshold, an internal overvoltage signal asserts after 1us (typical). This OVP signal latches off the high-side FET, turns on the low-side FET and also asserts PGOOD low. The low-side FET remains on to discharge the output capacitor until VSNS voltage drops below 1.15 x V_{REF}. Then low-side FET turns off to prevent complete discharge of V_{OUT}. The high-side and low-side FETs remain latched off until V_{IN} or EN is recycled. In order to use this feature, connect VSNS to V_{OUT} with a resistor divider as shown in the application circuit. Use the same resistor divider value that was used for programming V_{OUT}.

Programming the Output Voltage

Use a voltage divider as shown in Figure 1 to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1 \right)$$

The recommended value for R2 is 2kΩ.

Programming the Soft-Start

Place a capacitor C_{SS} between the SS and AGND pins to program the soft-start. In order to program a soft-start time of t_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS} = t_{SS} \times \frac{10\mu A}{0.6V}$$

Pre-Bias Startup

XR76121 has the capability to startup into a pre-charged output. Typical pre-bias startup waveforms are shown in Figure 15.

Maximum Allowable Voltage Ripple at FB Pin

The steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the regulator to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV then C_{OUT} and/or L should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Applications Information (Continued)

Feed-Forward Capacitor (C_{FF})

The feed-forward capacitor C_{FF} is used to set the necessary phase margin when using ceramic output capacitors. Calculate C_{FF} from the following equation:

$$C_{FF} = \frac{1}{2 \times \pi \times R1 \times 5 \times f_{LC}}$$

Where f_{LC}, the output filter double-pole frequency is calculated from:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

You must use manufacturer's DC derating curves to determine the effective capacitance corresponding to V_{OUT}. A load step test (and/or a loop frequency response test) should be performed and if necessary C_{FF} can be adjusted in order to get a critically damped transient load response.

In applications where output voltage ripple is less than about 3mV, such as when a large number of ceramic C_{OUT} are paralleled, it is necessary to use ripple injection from across the inductor. The circuit and corresponding calculations are explained in the MaxLinear design note.

Feed-Forward Resistor (R_{FF})

R_{FF} is required when C_{FF} is used. R_{FF}, in conjunction with C_{FF}, functions similar to a high frequency pole and adds gain margin to the frequency response. Calculate R_{FF} from:

$$R_{FF} = \frac{1}{2 \times \pi \times f \times C_{FF}}$$

Where f is the switching frequency.

If R_{FF} is greater than 0.1 x R1, then instead of C_{FF}/R_{FF}, use ripple injection circuit as described in MaxLinear's design note.

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR76121 is specified in the Operating Ratings section of this datasheet. The θ_{JA} thermal resistance specification is based on the XR76121 evaluation board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

The package thermal derating curves for the XR76121 are shown in Figures 5 and 6. These correspond to input voltage of 12V and 5V, respectively. The package thermal derating curves for the XR76121 are shown in Figures 9 and 10.

Applications Information

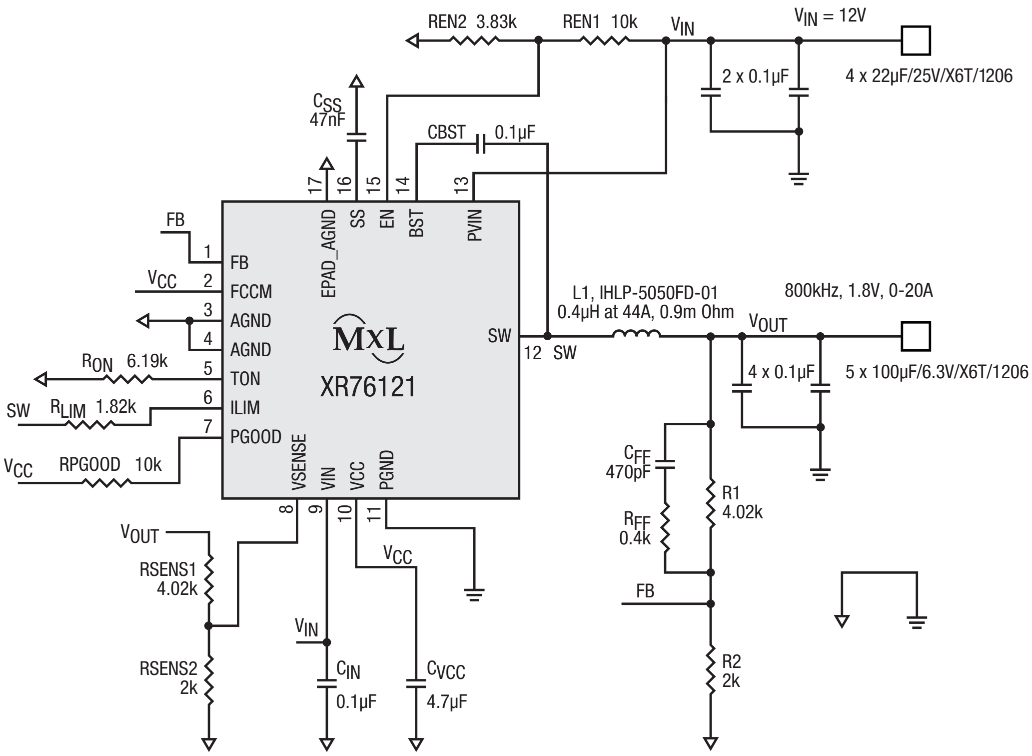
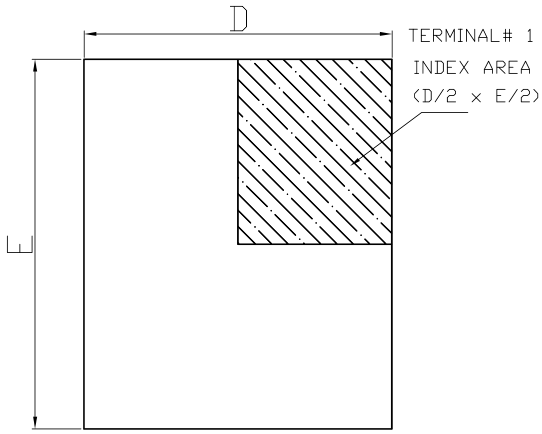
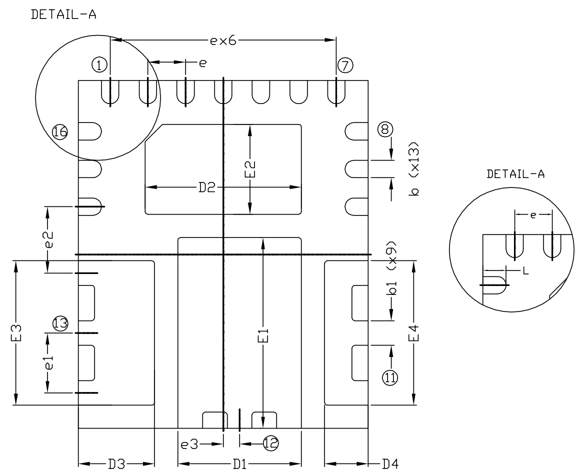


Figure 27. Application Circuit Schematic

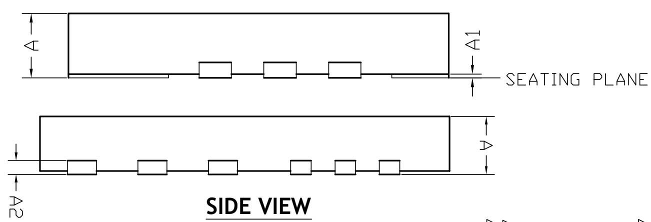
Mechanical Dimensions



TOP VIEW

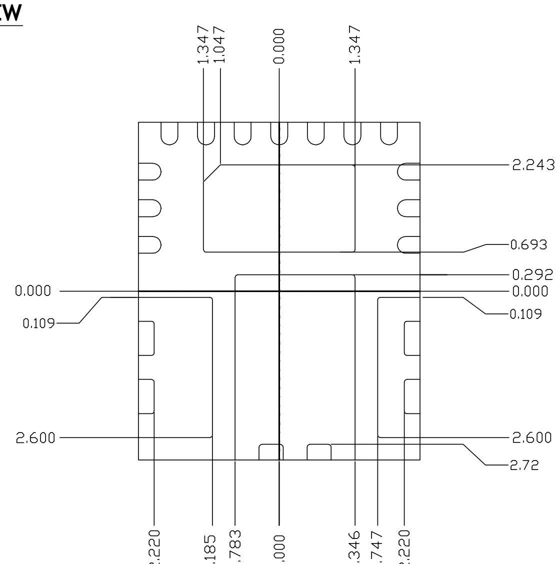


BOTTOM VIEW



SIDE VIEW

PACKAGE	17L QFN 6x5 mm		
REF.	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0	-	0.05
A2	0.20 Ref.		
b	0.250	0.300	0.350
b1	0.375	0.425	0.475
D	4.900	5.000	5.100
D1	2.079	2.129	2.179
D2	2.644	2.694	2.744
D3	1.265	1.315	1.365
D4	0.703	0.753	0.803
E	5.900	6.000	6.100
E1	3.242	3.292	3.342
E2	1.500	1.550	1.600
E3	2.441	2.491	2.541
E4	2.441	2.491	2.541
e	0.650 Ref.		
e1	1.033 Ref.		
e2	1.145 Ref.		
e3	0.281 Ref.		
L	0.350	0.400	0.450



TERMINAL DETAILS

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

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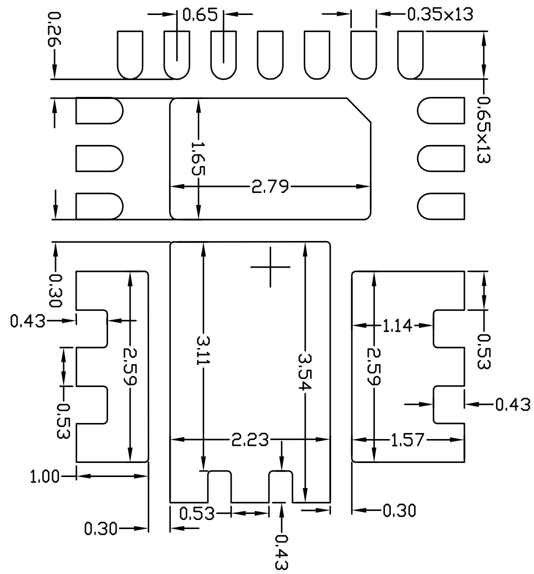
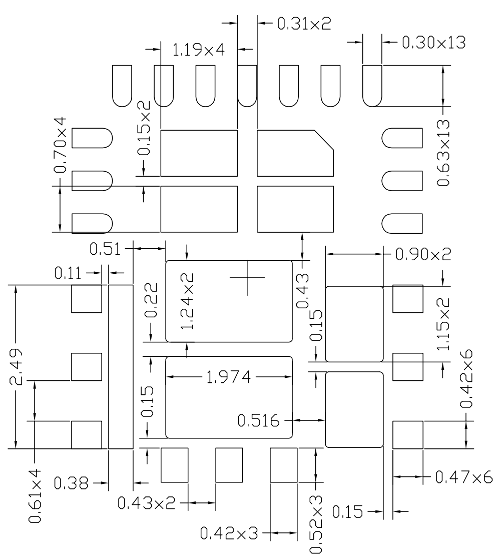
Revision: D

Figure 28. Mechanical Dimensions

Recommended Land Pattern and Stencil





NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000071

Revision: D

Figure 29. Recommended Land Pattern and Stencil