BittWare a molex company

XUP-VV8

PCIe FPGA Board

8x 100GbE Network Ports and VU9P/13P FPGA

XILINX

The XUP-VV8 offers a large Xilinx FPGA in a 3/4-length PCIe board featuring QSFP-DD (double-density) cages for maximum port density. Using the Virtex UltraScale+ VU13P or VU9P FPGA, the board supports up to 8x 100GbE or 32x 10/25GbE.

The FPGA provides large logic and memory resources—up to 3.8M logic cells and 455Mb embedded memory. The board also provides a jitter cleaner to support synchronous ethernet. The board can be configured as single width for users who don't need external memory on the DIMMs.

Xilinx VU13P FPGA: lidless package is used by BittWare's Viper thermal management for enhanced cooling performance

Module connects to one of the **QSFP-DD** cages on XUP-VV8

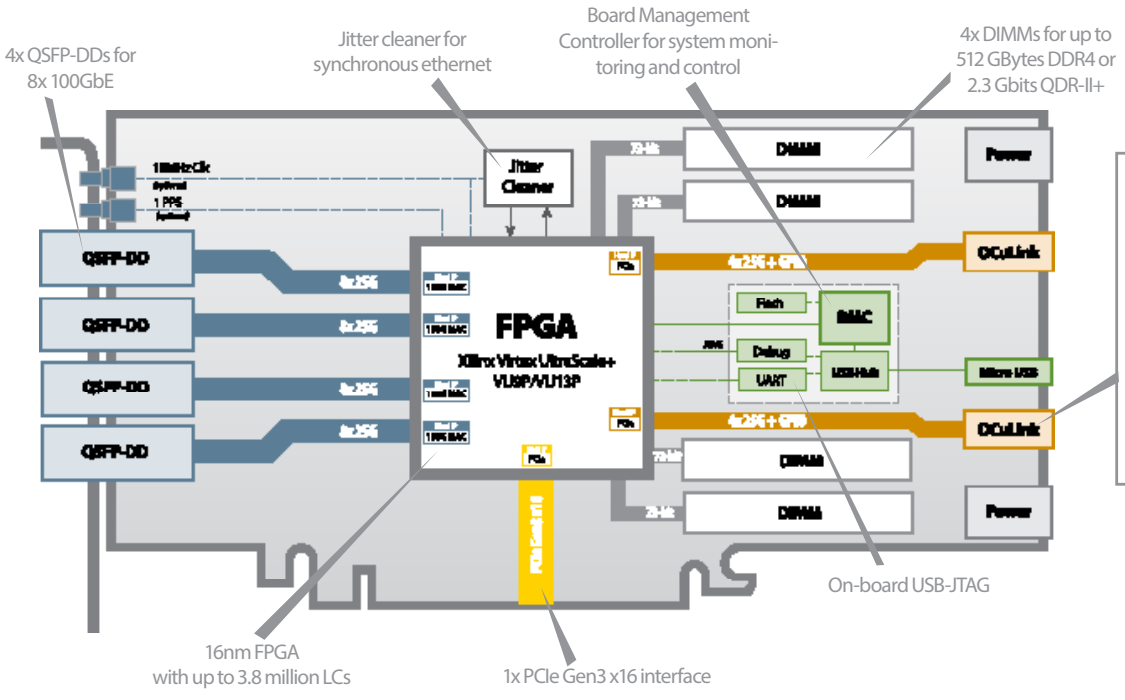
Breakout **QSFP28** to 2x 100GbE modules

key features

Four QSFP-DDs up to 8x 100GbE or 32x 10/25GbE

Up to **512 GBytes** DDR4

Up to **3.8M Logic Cells** and **455Mb Embedded RAM**



OCuLink Expansion Ports

Optimize the XUP-VV8 for your application with expansion:

- Board-to-board interconnect
- Connect to accessory boards for customization options

Inquire about customized Molex connectors/cables as required for your application.

Additional Services

Take advantage of BittWare's range of design, integration, and support options

Customization

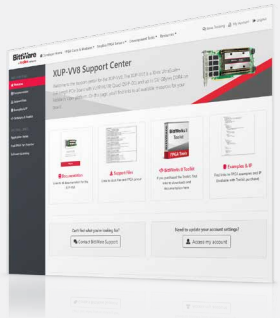
Additional specification options or accessory boards to meet your exact needs.

Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.

Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	• Virtex UltraScale+
	  • VU9P or VU13P in D2104 package
	  • Core speed grade - 2
	• Contact BittWare for other FPGA options

On-board Flash	• Flash memory for booting FPGA

External memory	• 4 DIMM sites, each supporting:
	  • Up to 128 GBytes DDR4 x72 with ECC
	  • Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)

Host interface	• x16 Gen3 interface direct to FPGA
USB port	• Micro USB: access to BMC, FPGA JTAG, and FPGA UART
Timestamp	• 1 PPS input and 10MHz clock input
OCuLink	• 2 OCuLink on rear edge, each connected to FPGA via 4x GTY transceivers
QSFP cages	• 4 QSFP-DD cages on front panel • Each supports 2x 100GbE, 2x 40GbE, 8x 25GbE, or 8x 10GbE • Jitter cleaner for network recovered clocking
Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I^2C bus access • USB 2.0 • Voltage overrides
Cooling	• Standard: dual-width passive heatsink • Optional: single-width passive heatsink*
Electrical	• On-board power derived from 12V PCIe slot & two AUX connectors (8-pin) • Power dissipation is application dependent
Environmental	• Operating temperature 5°C to 35°C
Form factor	• ¾-length, standard-height PCIe dual-width board • Single-width option* • 10 x 4.37 inches (254 x 111.15 mm)

Development Tools

System development	• BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
FPGA development	• FPGA Examples - example Vivado projects, available with the BittWorks II Toolkit • Xilinx Tools - Vivado® Design Suite

** Available on boards with no external memory*

To learn more, visit **www.BittWare.com**

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