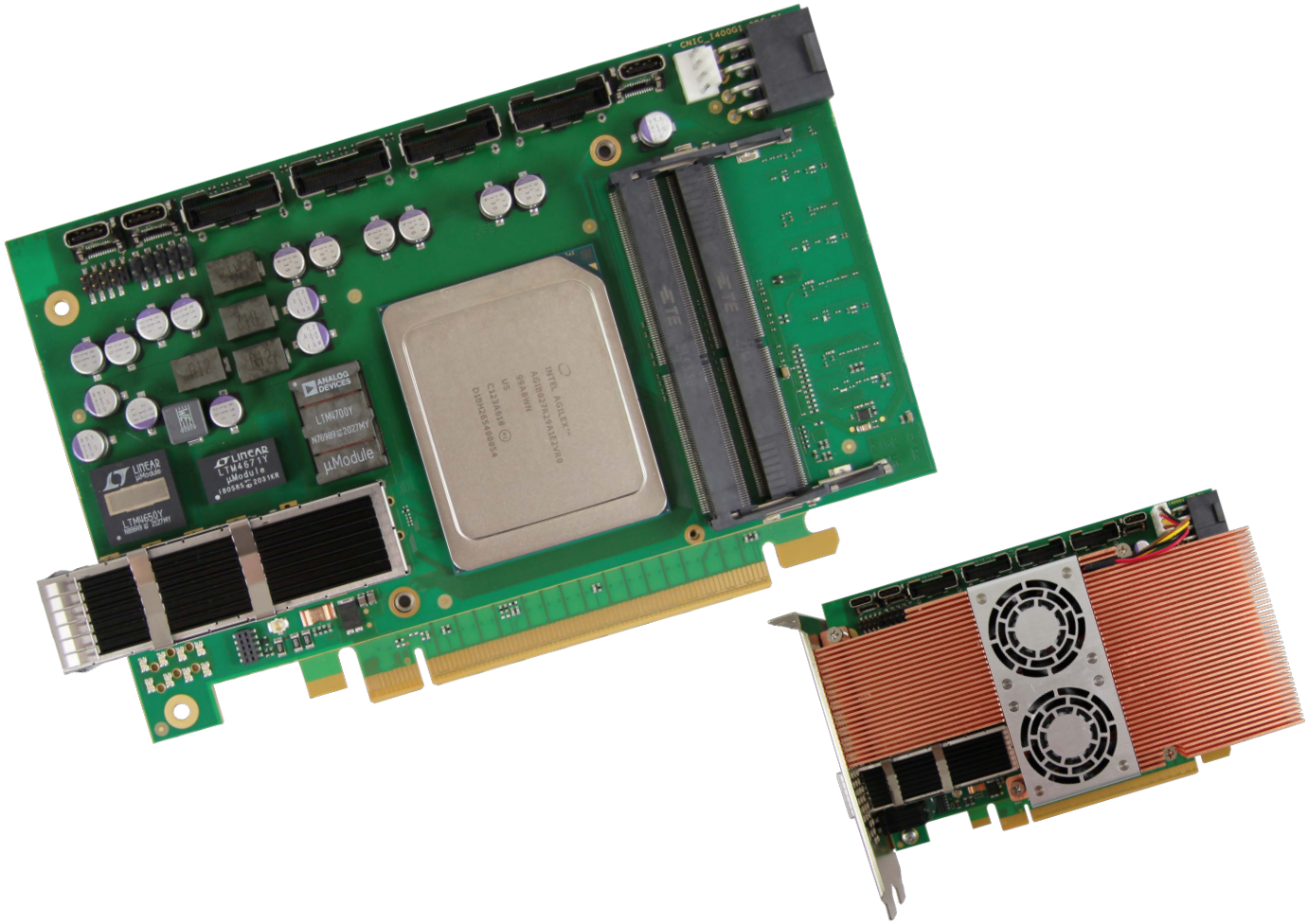
reflex ces high tech for innovators

XpressSX AGI-FH400G

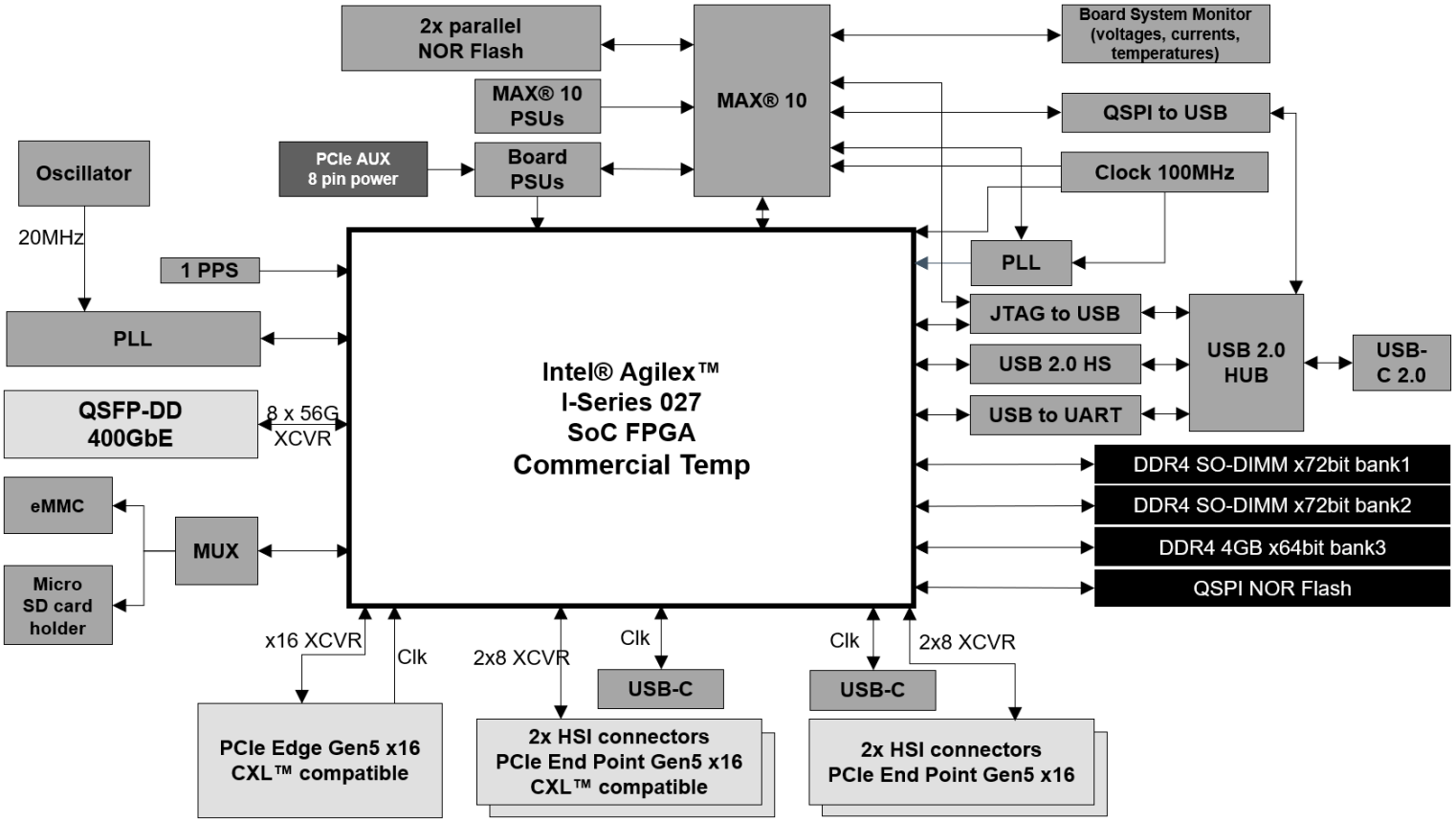
Full height, half length PCIe Gen5 Network Processing board



- Intel® Agilex™ I-Series SoC
- Quad Core ARM® Cortex® A53
- 2700 KLE
- PCIe Edge Gen5 x16, CXL™

- 400GbE (8 x 56)
- 3x DDR4
- 4x HSI connectors (PCIe Gen5 x16 EP)

- Security
- SmartNIC
- Networking Acceleration



Full Specifications

FPGA Configuration

- Intel® Agilex™ I-Series : AGIB027R29A1E2V including SoC: Quad Core ARM® Cortex® A53

SoC support for the Production Silicon version 400GT only

- Flash configuration
- USB 2.0 Hub for JTAG, UART, BMC, USB2

Memory

- 1x on-board DDR4 (mutual SoC / FPGA), x64 bit bus, 4GBytes up to 2666 MT/s
- 2x DDR4 SO-DIMM sockets, each capable up to 32GBytes SO-DIMM, with ECC
- eMMC or SD Card holder (if used) for SoC

Power

- 200W max, delivered with 2-slot active heatsink
- Powered by the PCIe slot and an 8 pin PCIe Aux ATX external connector (additional power)

Operating Range

- 0°C to 35°C

Storage Range

- 0°C to 70°C

Board Dimensions

- Full height half length: 167.7mm x 111.15mm

Communication Interfaces

- PCIe Edge Gen5 x16
- CXL™ standard compatible*:
  - Open standard interconnection for high-speed CPU-to-device and CPU-to-memory
  - Built on the PCIe physical and electrical interface
- 8x QSFP56-DD (8x 56G: 400G total)
- 2x HSI connectors (ARF6-16-L-RA): Total of 16 transceivers for PCIe Gen5 EP, CXL™ standard compatible
- 2x HSI connectors (ARF6-16-L-RA): Total of 16 transceivers for PCIe Gen5 EP
- 2x USB-C connectors for HSI Clocks & control signals

Other Resources

- Board Management Controller (MAX®10 device)
- Programmable PLL

Standards and Compliance

- RoHS/REACH compliant
- UL certified
- ISO9001 certified

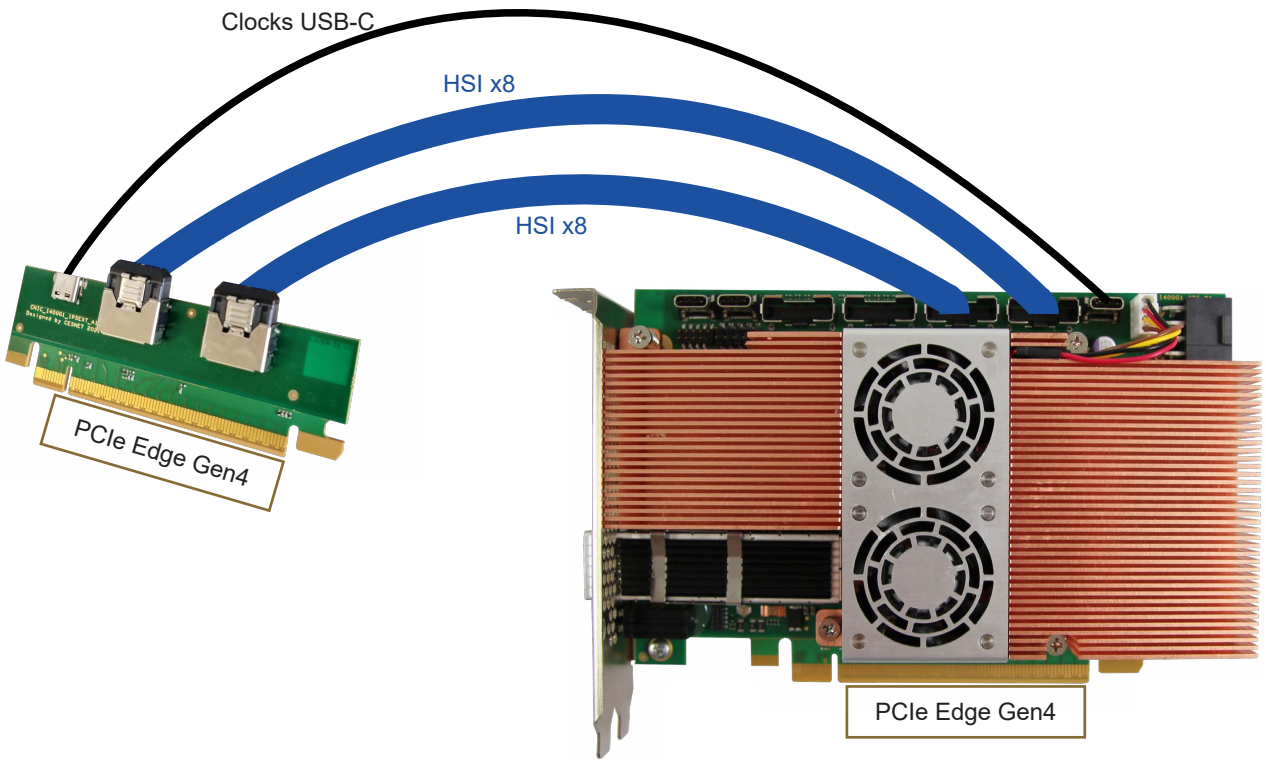
*Use of CXL™ features might require separate CXL™ IP license purchase. Please contact Intel® for details.

Additional PCIe Gen4 x16 daughter

The XpressSX AGI-FH400G board needs to be inserted in a PCIe Gen5 compatible server in order to deliver the full PCIe Gen5 x16 performances.

In case the user is only using a PCIe Gen4 compatible server, the XpressSX AGI-FH400G is delivered with this PCIe Gen4 x16 daughter card. This way, the system will achieve 2x Gen4 x16 performances similar to PCIe Gen5 x16, using two R-Tile PCIe Hard IPs inside the FPGA.

The daughter card also supports x8x8 bifurcation mode.



Deliverables

- Full height half length 2-slot PCIe board with active heatsink and PCIe bracket
- 2x DDR4 SO-DIMM 32GByte each
- Board Support Package: Manuals, 2D drawing, HDL reference designs (Contact REFLEX CES for PCIe Gen5 CXL™ interface validation)
- DWF/STEP models (upon request)
- Online support at support.reflexces.com
- NDK package (including DPDK NIC application) provided separately by BrnoLogic
- 2x HSI cables (ARC6-16-10.0-LU-LD-2-1) and 1x USB-C to USB-C cables (0.72ft), 3.1 Gen2 to connect the PCIe Gen4 x16 daughter card
- PCIe Gen4 x16 daughter card

Ordering information

XpressSXAGI-FH400GT-ES	=	Intel® Agilex™ SoC I-Series ES Silicon (AGIB027R29A1E2VR3), 3 banks DDR4 - No SoC support
XpressSXAGI-FH400GT	=	Intel® Agilex™ SoC I-Series Production Silicon (AGIB027R29A1E2V), 3 banks DDR4

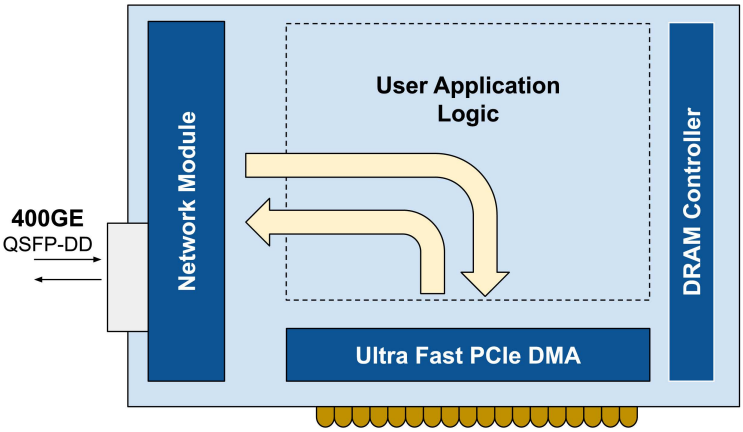
Contact sales for availability and pricing

Development Framework for High-speed Packet Processing

Start your design from standard NIC

- Provided as a free demo application
- Network module based on F-Tile 400G Ethernet Hard IP
- Ultra fast DMA with 400 Gbps throughput based on PCIe Gen5 x16 interface (R-Tile)
- Easy to use memory interface for single read/write data from/to card
- Preconfigured DDR4 controller for memory access from the user logic
- Precise timestamps with 2.5 ns resolution for 400G Ethernet

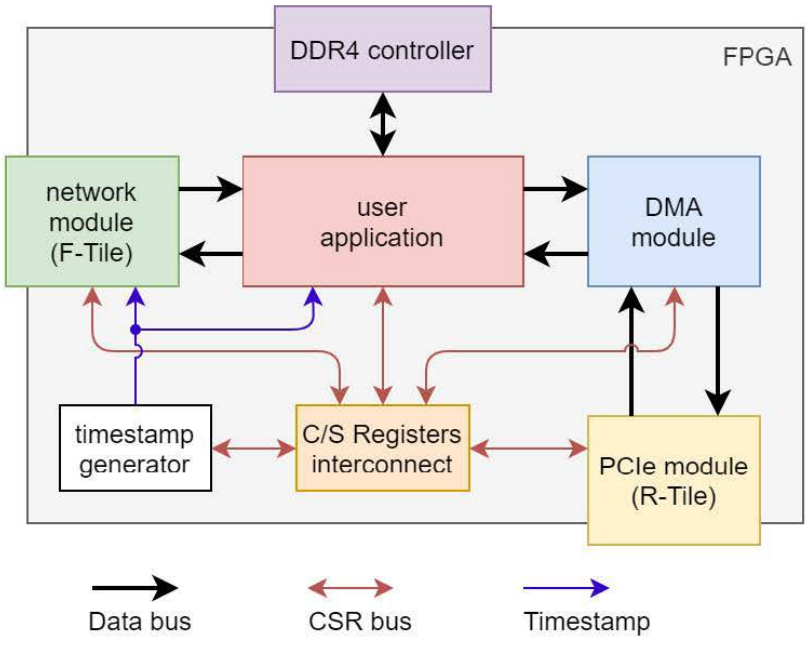
Standard NIC with high-speed packet capture
1x400GE, 2x200GE, 4x100GE, 8x50GE, 2x40GE, 8x25GE, 8x10GE



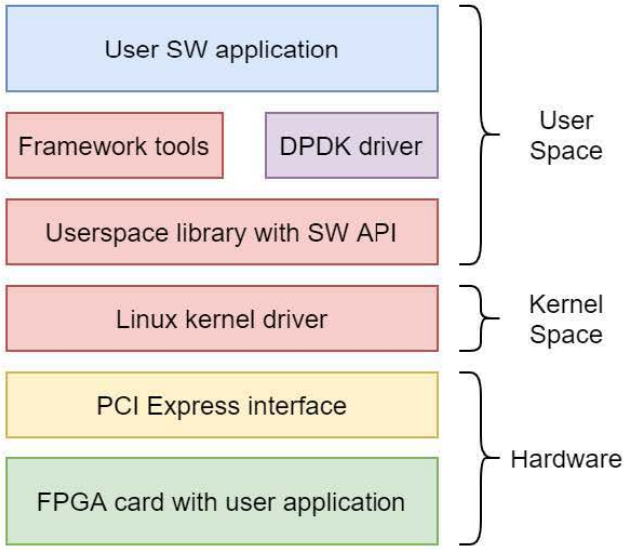
Easy to use NDK Development Framework

- Set of open-source IP cores for data manipulation
- Automatic scripts for complete design synthesis
- Single make command to create complete FPGA bitstream
- Bitstream identification through DeviceTree ROM
- Easy to use software stack in a single RPM package
- Linux kernel driver, DPDK support, user space library, tools for the configuration of components
- Easy creation of custom application by user-friendly API for component access and DMA transfers
- Fully parameterizable and modular hardware and software architecture

FPGA design architecture



Software stack



Part number: NDK-PROF-SUPPORT

BRNO LOGIC
sales@brnologic.cz
www.brnologic.cz

cesnet
Open source IP core library
www.liberouter.org/ndk