

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- · Direct interfacing to logic level ICs
- · Direct interfacing to low power gate drive circuits
- · High blocking voltage capability
- · Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- · Home appliances
- · Industrial process control
- Low power AC Fan controllers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage			-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{lead} \le 45$ °C; $\overline{Fig. 1}$; $\overline{Fig. 2}$; $\overline{Fig. 3}$		-	-	1	A
I _{TSM}	non-repetitive peak on-	full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms		-	-	8	Α
	state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms; Fig. 4; Fig. 5		-	-	8.5	А
T _j	junction temperature			-	-	125	°C
Static chara	acteristics		'				
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$		-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; Fig. 7$		-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \overline{\text{Fig. } 7}$		-	-	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2-\text{ G+;} $ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	-	7	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V _T	on-state voltage	I _T = 1 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
Dynamic cha	racteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	20	-	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; dI_{com}/dt = 0.44 A/ms; I_T = 1 A; gate open circuit	1	-	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		T2
2	G	gate		G sym051
3	T1	main terminal 1	TO-92 (SOT54)	Symosi

6. Ordering information

Table 3. Ordering information

Type number		Package					
		Name	Description	Version			
	Z0107NA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

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7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{lead} ≤ 45 °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	1	Α
I _{TSM}	non-repetitive peak on-	full sine wave; $T_{j(init)} = 25 ^{\circ}C$; $t_p = 20 \text{ms}$	-	8	Α
sta	state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms; Fig. 4; Fig. 5	-	8.5	Α
I ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.32	A²s
dI _T /dt	rate of rise of on-state	I _G = 20 mA; T2+ G+	-	50	A/µs
	current	I _G = 20 mA; T2+ G-	-	50	A/µs
		I _G = 20 mA; T2- G-	-	50	A/µs
		I _G = 20 mA; T2- G+	-	20	A/µs
I _{GM}	peak gate current		-	1	Α
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

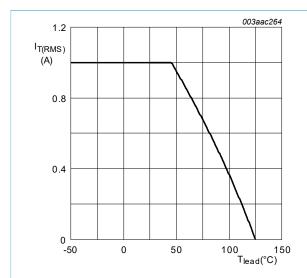
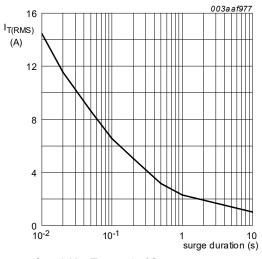


Fig. 1. RMS on-state current as a function of lead temperature; maximum values



 $f = 50 \text{ Hz}; T_{lead} = 45 ^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

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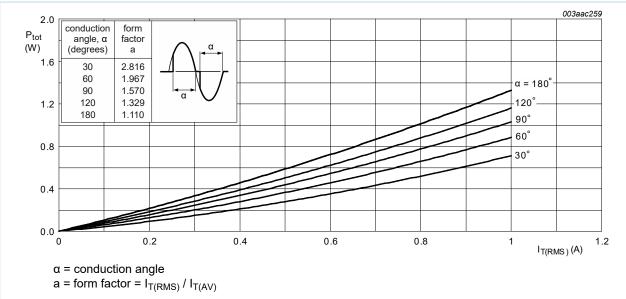


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

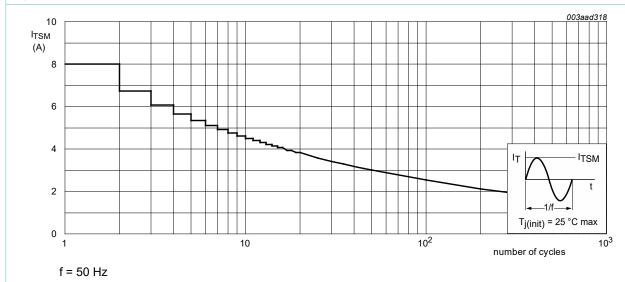
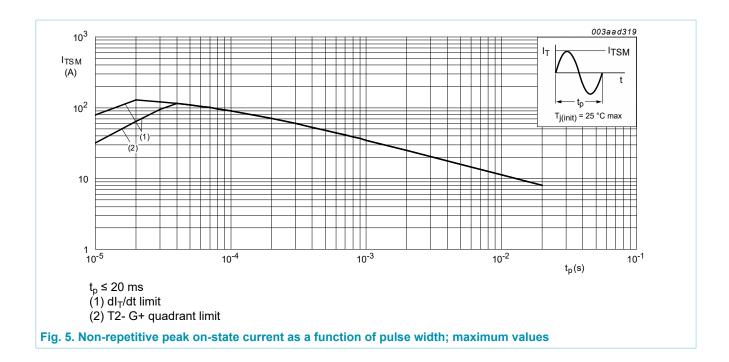


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-lead)}	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	full cycle; printed circuit board; lead length = 4 mm	-	150	-	K/W

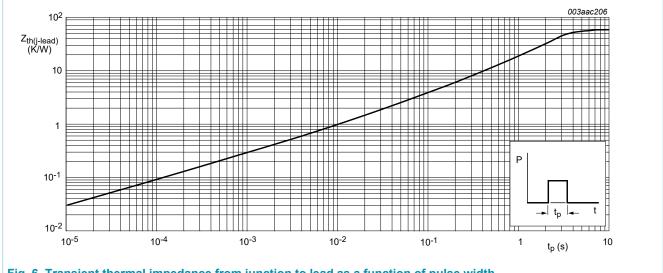


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

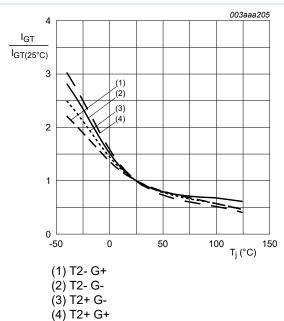
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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{G-};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 7}}$	-	-	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	7	mA
L	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	20	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	10	mA
l _н	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	10	mA
V _T	on-state voltage	I _T = 1 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
V_{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	-	1	V
		V _D = 800 V; I _T = 0.1 A; T _j = 125 °C	0.2	-	-	V
l _D	off-state current	V _D = 800 V; T _j = 125 °C	-	-	0.5	mA
Dynamic ch	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 110 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	20	-	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T_j = 110 °C; $dI_{com}/$ dt = 0.44 A/ms; I_T = 1 A; gate open circuit	1	-	-	V/µs

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junction temperature

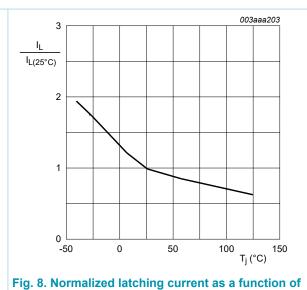


Fig. 7. Normalized gate trigger current as a function of junction temperature 003aaa204

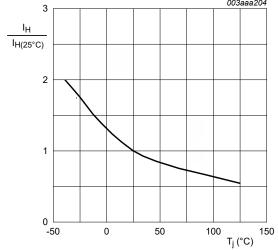
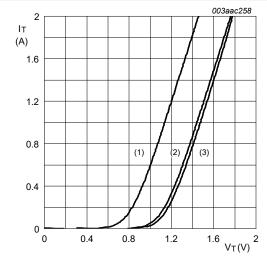


Fig. 9. Normalized holding current as a function of junction temperature



 $V_0 = 1.13 \text{ V}$ $R_s = 0.31 \Omega$

(1) T_j = 125 °C; typical values (2) T_j = 125 °C; maximum values

(3) T_i = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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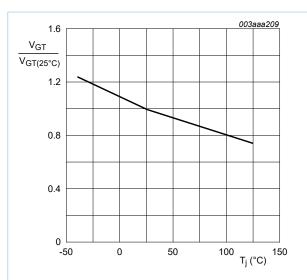


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

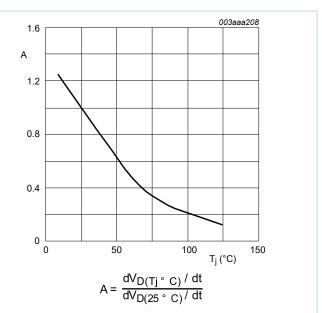
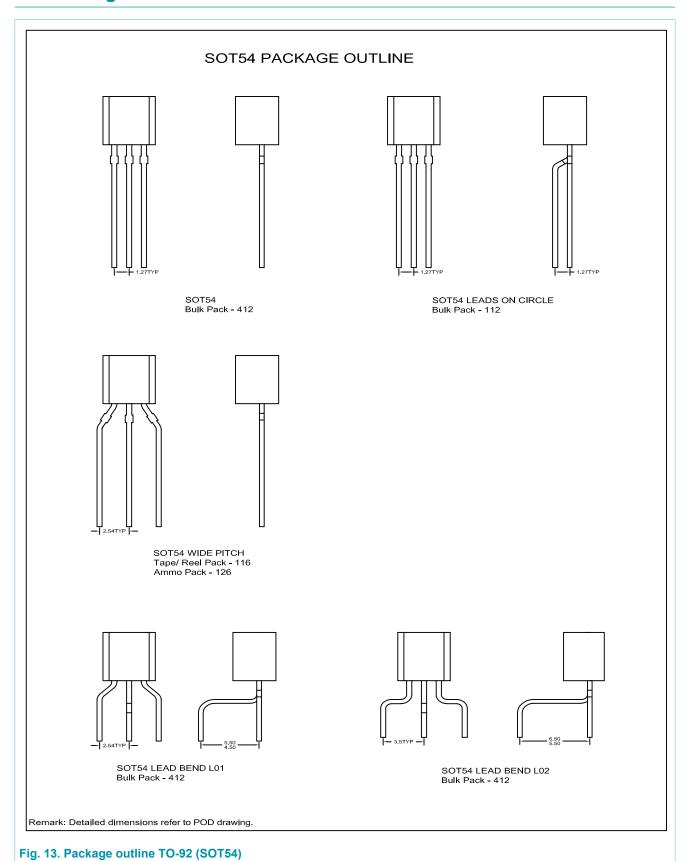


Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

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10. Package outline



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11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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