



Z02201

V.22bis Data Pump with Integrated AFE

PB008501-1201

Product Brief

Simple Block Diagram

Parallel I/F	DSP	ADC
	512 W RAM	DAC
8 KW ROM V.22bis/V.23V.22/V.21 Bell 212A/103		OSC
	Serial Interface	Eye Pattern I/F

Features

Device	Data Pump AFE	Speed (MHz)
Z02922	16-Bit Integrated	12.228

- Combined data pump and Analog Front-End (AFE)
- Full duplex data modem throughput to 2400 bps
 - ITU V.22bis, V.23, V.22, V.21
 - Bell 212A and Bell 103
- FSK (V.23 1200/75 bps, V.21/Bell 103 300 bps), DPSK (V.22/Bell 212A 1200 bps), or QAM encoding (V.22bis 2400 bps)
- Automatic handshake plus full manual control over handshake timings
- Scrambler/descrambler functions plus selectable control over internal data pump functions
- Programmable Bi-Quad tone detectors for call-progress tone detection
- Adaptive equalization to compensate for a wide variety of line conditions
- Programmable transmit attenuation and selectable receive threshold

- Fully programmable call-progress detectors, signal quality detectors, tone detectors, tone generators, and transmit signal levels which aid in rapid country qualifications
- Simultaneous tone generation and detection
- Host port allows direct parallel interface to standard 8-bit microprocessors
- HDLC framing at all speeds
- On-chip peripherals
 - Full-duplex voice band AFE with 12-bit resolution
 - Synchronous Serial Interface port
 - Eye pattern interface
- Low power consumption: 50 mA typical
- 44-Pin PLCC package
- Single +5 VDC power supply
- 0°C to +70°C commercial temperature range

Note: International Telecommunications Union (ITU), formerly CCITT.

General Description

The Z02201 is a synchronous single-chip modem solution that provides a means to construct a V.22bis modem capable of 2400 bps full duplex over dial-up lines. The Z02201 is specifically designed for use in embedded modem applications where space, performance, and low power consumption are key requirements.

Operating over the Public Switched Telephone Network (PSTN), the Z02201 meets the modem standards for V.22bis, V.22, V.23, V.21, Bell 212A, and Bell 103.



A typical modem application can be made by simply adding a control microprocessor (host), phone-line interface, and DTE interface.

The Z02201 performs HDLC framing at all speeds. This capability eliminates the requirement for an external Serial Input/Output (SIO) device for Data Terminal Equipment (DTE) in products incorporating error control.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip. Automatic and selectable compromise equalizers are included to optimize performance over a wide range of line types.

The Z02201 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers.

The Z02201 provides comprehensive selectable and programmable tone generation and detection.

All digital I/O signals are TTL compatible. The parallel interface is compatible with standard 8-bit microprocessors, allowing direct access to eight I/O registers and indirect access to the modem RAM.

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control data, and set programmable coefficients. The serial interface is used for data transfers. All control and status information is transferred by means of the parallel interface.

The Z02201 transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer. Completing this connection reduces the external circuits to a minimum.

In addition, the Z02201 offers further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the need for external filtering components.

The Z02201 device operates on a single +5 VDC power supply. During periods of no traffic, the host can place the modem into SLEEP mode, reducing power consumption to less than 1 percent of full load power.

Note: All signals with an overline, are active Low. For example, B/\overline{W} , in which WORD is active Low; or \overline{E}/W , in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Block Diagram

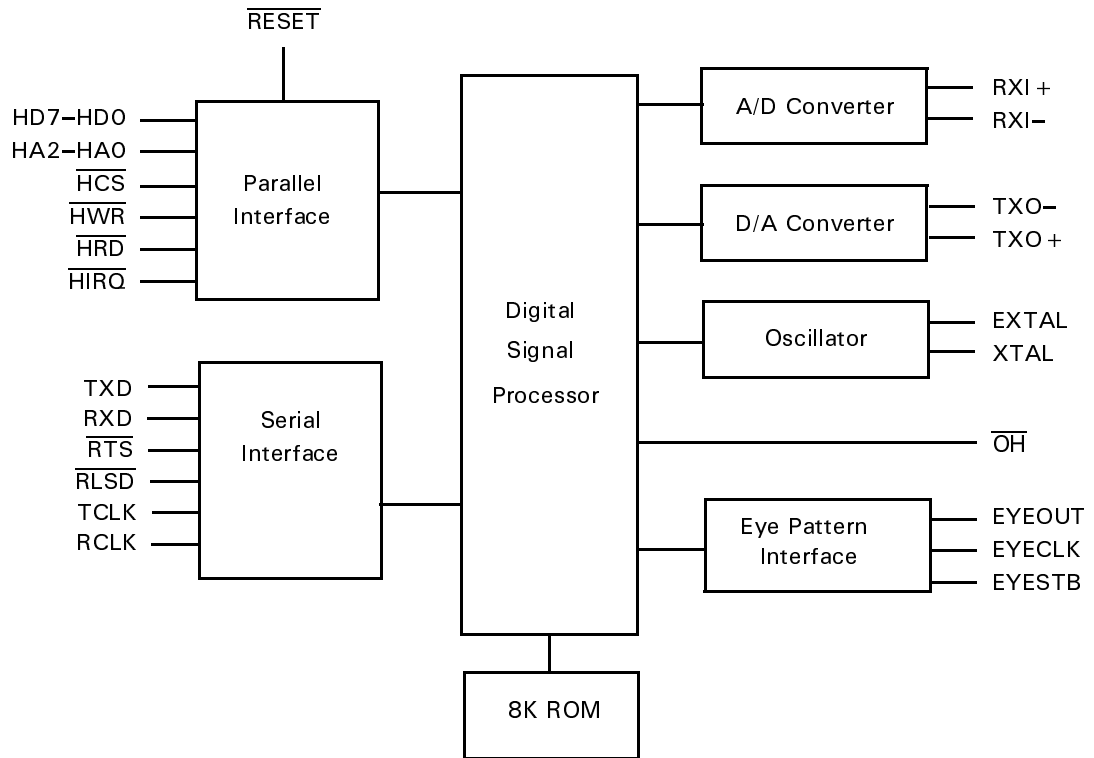


Figure 1. Z02201 Block Diagram

Pin-Outs and Pin Direction

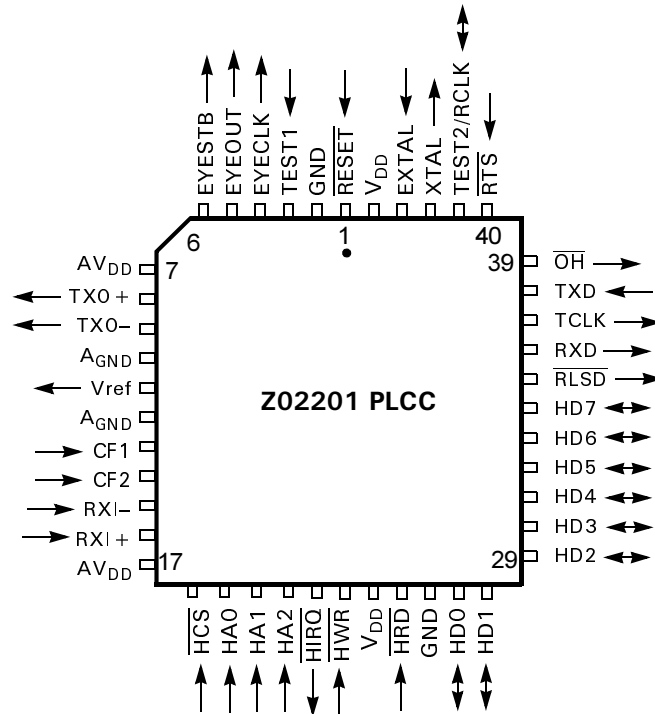


Figure 2. Z02201 44-Pin PLCC Identification

Ordering Information

Z02201 12.288 MHz 44-Pin PLCC

ROM code Version 0x48 Z0220112VSCR4078

ROM code Version 0x31 Z0220112VSCR3470

Refer to the Z02201 Product Update (<http://www.zilog.com/docs/modem/z02201update.pdf>) for the software differences between the two ROM code versions. The Product Update also lists the workarounds for Version 0x31 of the ROM code.

For fast results, contact your local ZiLOG sales office for assistance in ordering this part.