

Zilog

Z08470 Customer
Procurement Spec (CPS)

GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel, multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial, converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.

0	1	40	D ₈
0 ₁	2	36	D ₇
0 ₂	3	32	D ₆
0 ₃	4	28	D ₅
0 ₄	5	24	D ₄
0 ₅	6	20	D ₃
0 ₆	7	16	D ₂
0 ₇	8	12	D ₁
0 ₈	9	8	D ₀
0 ₉	10	4	D ₀
10	11	38	RD/STB
11	12	34	RD/STB
12	13	30	RD/STB
13	14	26	RD/STB
14	15	22	RD/STB
15	16	18	RD/STB
16	17	14	RD/STB
17	18	10	RD/STB
18	19	6	RD/STB
19	20	2	RD/STB
20	21	38	RD/STB
21	22	34	RD/STB
22	23	30	RD/STB
23	24	26	RD/STB
24	25	22	RD/STB
25	26	18	RD/STB
26	27	14	RD/STB
27	28	10	RD/STB
28	29	6	RD/STB
29	30	2	RD/STB
30	31	38	RD/STB
31	32	34	RD/STB
32	33	30	RD/STB
33	34	26	RD/STB
34	35	22	RD/STB
35	36	18	RD/STB
36	37	14	RD/STB
37	38	10	RD/STB
38	39	6	RD/STB
39	40	2	RD/STB

40-Pin Dual-In-Line Package (DIP),
Pin Assignments

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(MARCOM) DC2847 DOCUMENT CONTROL
MASTER

DC CHARACTERISTICS

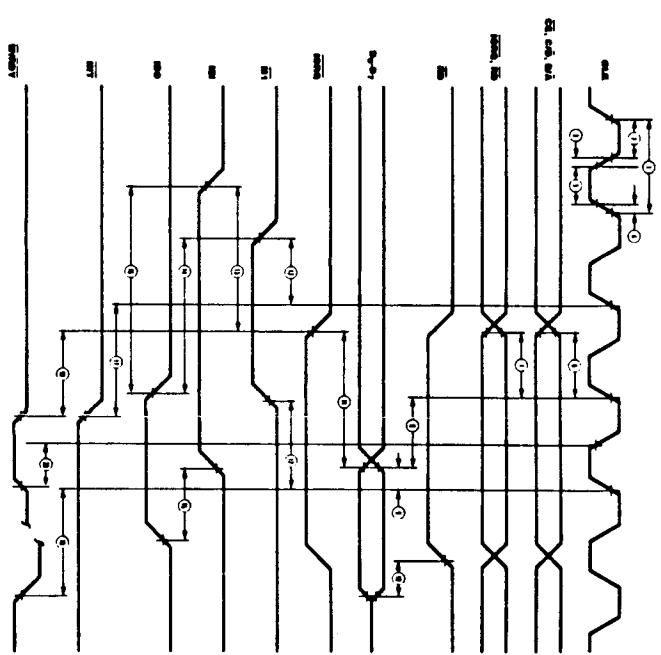
Symbol	Parameter	Min	Max	Units	Test Conditions
V _{CC}	Clock Input Low Voltage	-0.2 ^a	+0.45 ^b	V	V _{CC} = 2.0 mA 0.4 < V _{IN} < 2.0 V 0.4 < V _{OUT} < 2.0 V P _{AV} < 100 mW
V _{CC}	Clock Input High Voltage	V _{CC} - 0.8 ^a	+0.85 ^b	V	
V _{IN}	Input Low Voltage	-0.2 ^a	+0.18 ^b	V	
V _{IN}	Input High Voltage	+2.0 ^a	+0.85 ^b	V	
V _{OH}	Output Low Voltage	+0.4 ^a	+0.4 ^b	V	
V _{OH}	Output High Voltage	+2.4 ^a	+0.4 ^b	V	
I _{OL}	Input/3-Slew Output Leakage Current	-10 ^a	+10 ^b	μA	
I _{OH}	Input/3-Slew Output Leakage Current	-40 ^a	+10 ^b	μA	
I _{CC}	Power Supply Current		100 ^a	mA	
V _{CC}	V _{CC} - 0.2V to V _{CC} + 0.2V, 2.0V				

^a Tested
^b Guaranteed by Design
^c Guaranteed by Characterization

AC CHARACTERISTICS*

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T _{DC}	Clock Cycle Time	250 ^a	4000 ^a	185 ^a	4000 ^a
2	T _{HCH}	Clock Width (High)	105 ^a	2000 ^a	70 ^a	2000 ^a
3	T _{TC}	Clock Fall Time		30 ^a		15 ^a
4	T _{CC}	Clock Rise Time		30 ^a		15 ^a
5	T _{HCL}	Clock Width (Low)	105 ^a	2000 ^a	70 ^a	2000 ^a
6	T _{ANDQ}	CE, C _{EN} Setup to Clock Setup Time	145 ^a		80 ^a	
7	T _{ANDQ}	RE, RD Setup to Clock Setup Time	115 ^a		80 ^a	
8	T _{ANDQ}	Clock 1 to Data Out Delay		220 ^a		150 ^a
9	T _{ANDQ}	Data In to Clock Setup (Write or Hit Cycle)	50 ^a		30 ^a	
10	T _{ANDQ}	RD to Data Out Read Delay		110 ^a		80 ^a
11	T _{ANDQ}	RE, RD to Data Out Delay (TRACK Cycle)		180 ^a		100 ^a
12	T _{ANDQ}	RT to Clock Setup Time	80 ^a		75 ^a	
13	T _{ANDQ}	RT to RE, RD Setup Time (TRACK Cycle)	140 ^a		120 ^a	
14	T _{ANDQ}	RT to RE, RD Delay (format before hit)	180 ^a		180 ^a	
15	T _{ANDQ}	RT to RE, RD Delay (after ED decode)	100 ^a		70 ^a	
16	T _{ANDQ}	RT to RE, RD Delay	100 ^a		70 ^a	
17	T _{ANDQ}	Clock 1 to RT Delay	200 ^a		150 ^a	
18	T _{ANDQ}	RE, RD or CE 1 to W/RDY Delay (Ready Mode)	210 ^a		175 ^a	
19	T _{ANDQ}	Clock 1 to W/RDY Delay (Ready Mode)	120 ^a		100 ^a	
20	T _{ANDQ}	Clock 1 to W/RDY Read Delay (Ready Mode)	130 ^a		110 ^a	

* Units in microseconds (μs)
^a Tested
^b Guaranteed by Design
^c Guaranteed by Characterization



AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T _{WH}	Pulse Width (High)	200 ^a	200 ^a		
2	T _{WL}	Pulse Width (Low)	200 ^a	200 ^a		
3	T _{CHC}	CE Cycle Time	400 ^a	300 ^a	300 ^a	300 ^a
4	T _{HCL}	CE Width (Low)	180 ^a	100 ^a	100 ^a	100 ^a
5	T _{HCH}	CE Width (High)	180 ^a	100 ^a	100 ^a	100 ^a
6	T _{ANDQ}	CE 1 to RD Delay	300 ^a		220 ^a	
7	T _{ANDQ}	CE 1 to W/RDY Delay (Ready Mode)	5 ^a	9 ^a	5 ^a	9 ^a
8	T _{ANDQ}	CE 1 to RT Delay	5 ^a	9 ^a	5 ^a	9 ^a
9	T _{ANDQ}	RE Cycle Time	400 ^a	300 ^a	300 ^a	300 ^a
10	T _{ANDQ}	RE Width (Low)	180 ^a	100 ^a	100 ^a	100 ^a
11	T _{ANDQ}	RE Width (High)	180 ^a	100 ^a	100 ^a	100 ^a
12	T _{ANDQ}	RD to RE, RD Setup Time (Hit Mode)	0 ^a	0 ^a	0 ^a	0 ^a
13	T _{ANDQ}	RD Hold Time (Hit Mode)	140 ^a	100 ^a		
14	T _{ANDQ}	RE 1 to W/RDY Delay (Ready Mode)	10 ^a	13 ^a	10 ^a	13 ^a
15	T _{ANDQ}	RE 1 to RT Delay	10 ^a	13 ^a	10 ^a	13 ^a

* In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.
¹ Units equal to System Clock Period.
² Units in microseconds (μs)
^a Tested
^b Guaranteed by Design
^c Guaranteed by Characterization